TEXAS INSTRUMENTS

CD74HCT356

High-Speed CMOS Logic 8-Input Multiplexer/Register, Three-State

SCLS459A - June 2001 - Revised May 2003

Features

- Edge-Triggered Data Flip-Flops
  - Transparent Select Latches
- Buffered Inputs
- 3-State Complementary Outputs
- Bus Line Driving Capability
- Typical Propagation Delay: V_{CC} = 5V, C_L = 15pF, T_A = 25°C
  - Clock to Output = 22ns
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 4.5V to 5.5V Operation
- Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)
- CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The CD74HCT356 consists of data selectors/multiplexers that select one of eight sources. The data select bits (S0, S1, and S2) are stored in transparent latches that are enabled by a low latch enable input ($\overline{LE}$).

The data is stored in edge-triggered flip-flops that are triggered by a low-to-high clock transition.

In both types the 3-state outputs are controlled by three output-enable inputs ($\overline{OE1}$, $\overline{OE2}$, and OE3).

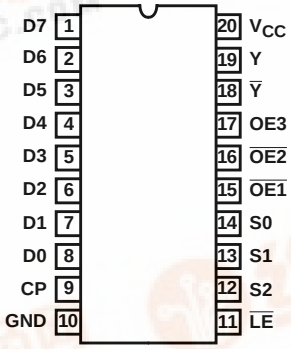
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HCT356E	-55 to 125	20 Ld PDIP
CD74HCT356M96	-55 to 125	20 Ld SOIC

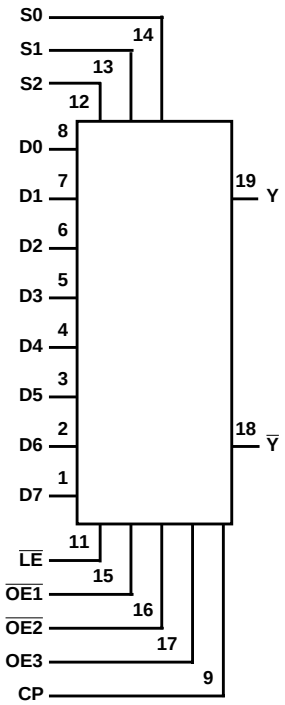
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Pinout

CD74HCT356
(PDIP or SOIC)
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS							OUTPUTS	
SELECT (NOTE 1)			CLOCK	OUTPUT ENABLES				
S2	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H or L	L	L	H	$\overline{D6}_n$	$D6_n$

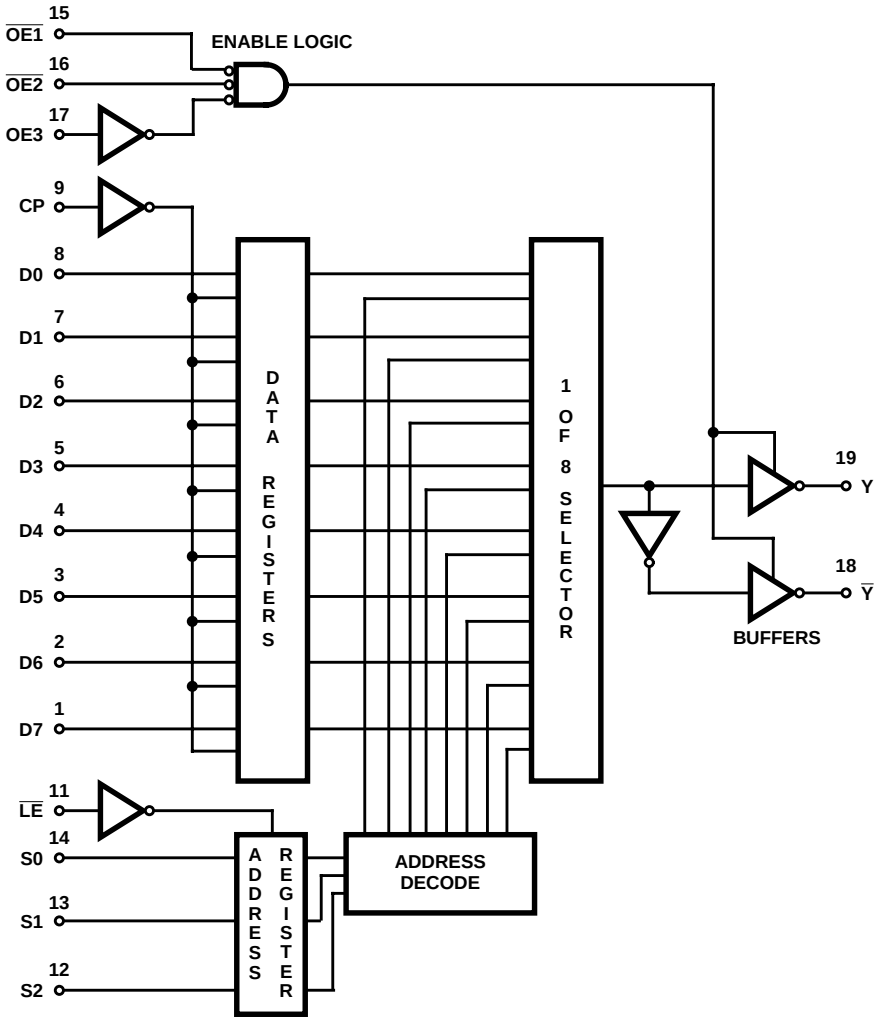
TRUTH TABLE (Continued)

INPUTS							OUTPUTS	
SELECT (NOTE 1)			CLOCK	OUTPUT ENABLES				
S2	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	OE3	$\overline{Y}$	Y
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

H = High Voltage Level (Steady State); L = Low Voltage Level (Steady State); ↑ = Transition from Low to High Level;
X = Don't Care; Z = High-Impedance State (Off State); $D0_n$...$D7_n$ = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.
NOTE:

1. This column shows the input address setup with $\overline{LE}$ low.

Block Diagram



Logic Diagram

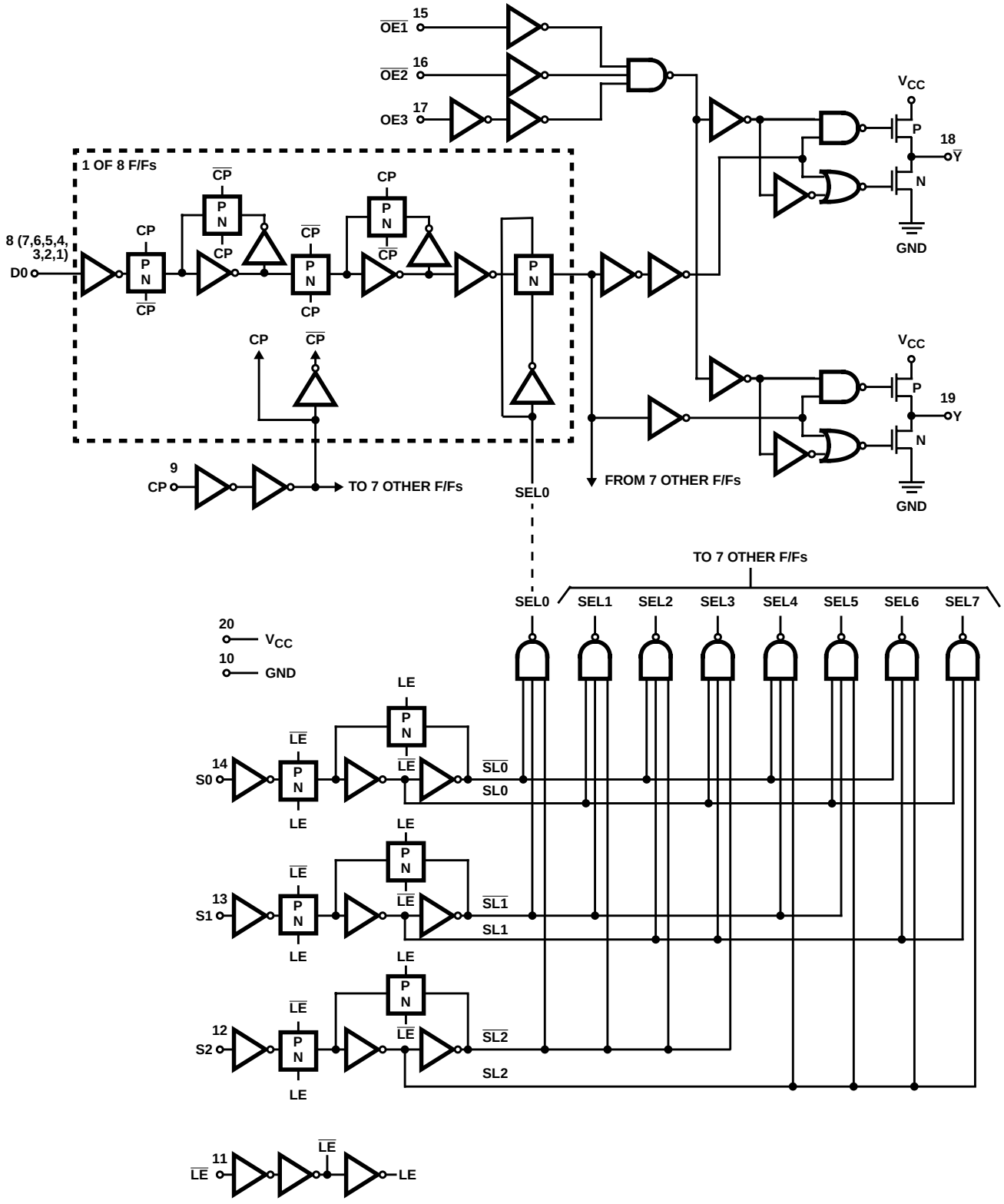


FIGURE 1. LOGIC DIAGRAM

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . . . ±35mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC} . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V . . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)
E (PDIP) Package	69
M (SOIC) Package	58

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25^oC			-40^oC TO 85^oC		-55^oC TO 125^oC		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
3-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	V_O = V_{CC} or GND	5.5	-	-	±0.5	-	±5	-	±10	µA

NOTE:

3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

Input Loading Table

INPUT	UNIT LOADS
D0-D7	0.50
S0, S1, S3	0.70
$\overline{OE1}$, $\overline{OE2}$	0.80
OE3	0.25
$\overline{LE}$	0.25
CP	0.60

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CP Pulse Width	t_{PLH}, t_{PHL}	-	4.5	16	20	-	25	-	30	-	ns
$\overline{LE}$ Pulse Width	t_{PLH}, t_{PHL}	-	4.5	16	20	-	25	-	30	-	ns
Setup Times Dn → $\overline{E}$	t_{SU}	-	4.5	5	7	-	9	-	11	-	ns
Setup Times Sn → $\overline{LE}$	t_{SU}	-	4.5	5	7	-	9	-	11	-	ns
Hold Times Dn → $\overline{E}$	t_H	-	4.5	9	9	-	11	-	14	-	ns
Hold Times Sn → $\overline{LE}$	t_H	-	4.5	12	12	-	15	-	18	-	ns

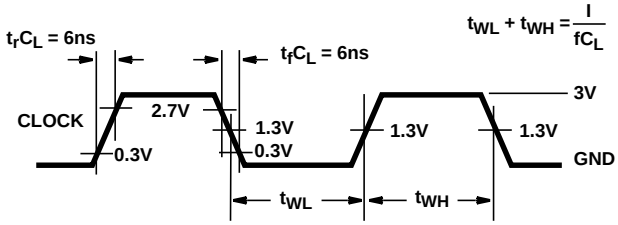
Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Propagation Delay, CP→ Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	51	64	77	ns
		C_L = 15pF	5	22	-	-	-	ns
Propagation Delay, Sn → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	59	74	89	ns
		C_L = 15pF	5	25	-	-	-	ns
Propagation Delay, $\overline{LE}$ → Y, $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	63	79	94	ns
		C_L = 15pF	5	25	-	-	-	ns
Output Disabling Time	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	33	41	50	ns
	t_{PLZ}	C_L = 15pF	5	13	-	-	-	ns
	t_{PHZ}	C_L = 15pF	5	15	-	-	-	ns
Output Enabling Time	t_{PLZ}, t_{PHZ}	C_L = 50pF	4.5	-	34	43	51	ns
		C_L = 15pF	5	14	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
3-State Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	52	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per device.
5. $P_D = V_{CC}^2 (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX}, input duty cycle = 50%.

FIGURE 2. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

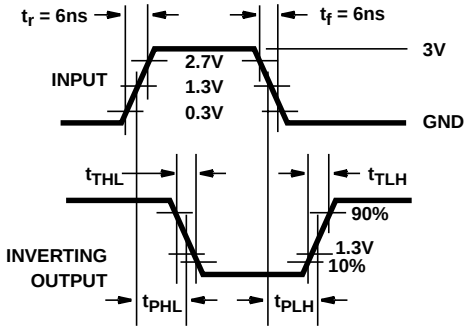


FIGURE 3. TRANSITION TIMES AND PROPAGATION-DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

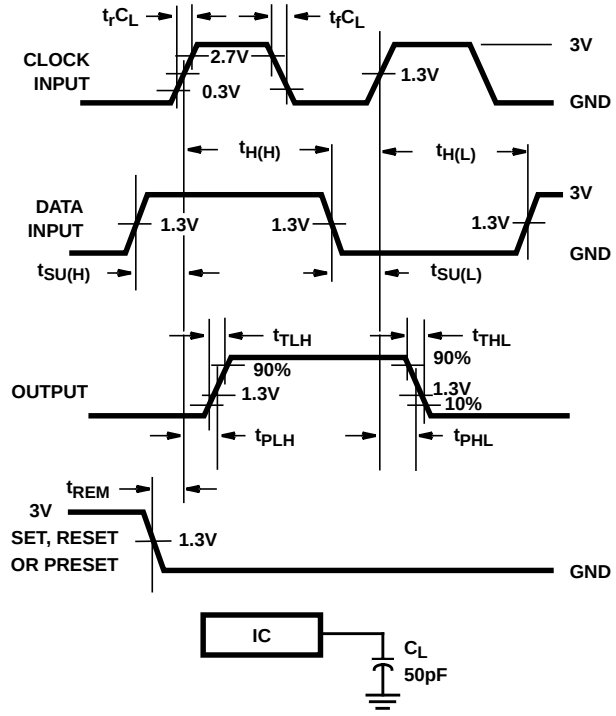


FIGURE 4. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION-DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

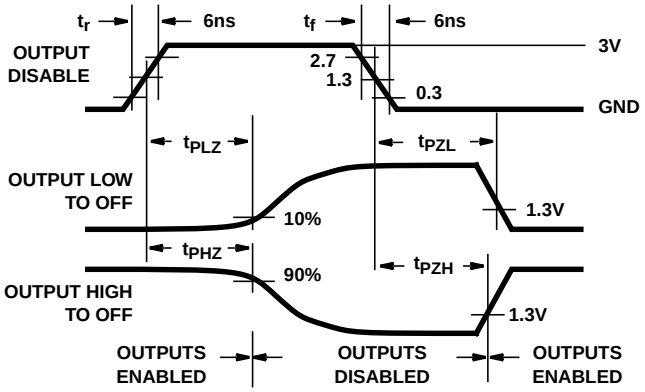
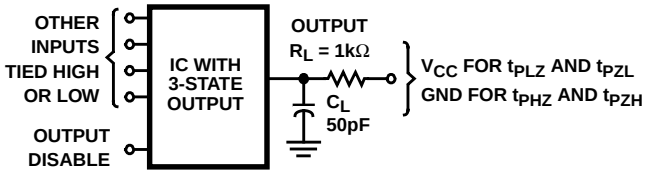


FIGURE 5. 3-STATE PROPAGATION-DELAY WAVEFORM



NOTE: Open-drain waveforms t_{PLZ} and t_{PZL} are the same as those for 3-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 6. 3-STATE PROPAGATION-DELAY TEST CIRCUIT

PACKAGE OPTION ADDENDUM

25-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HCT356E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT356M96	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

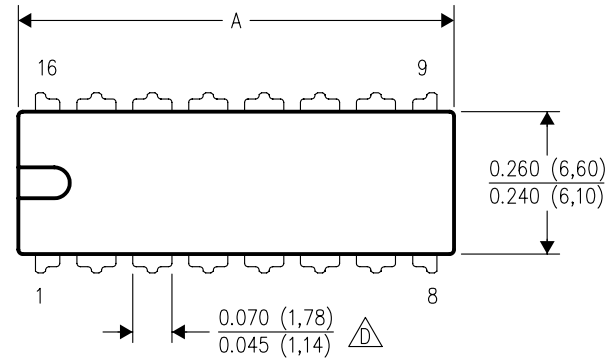
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

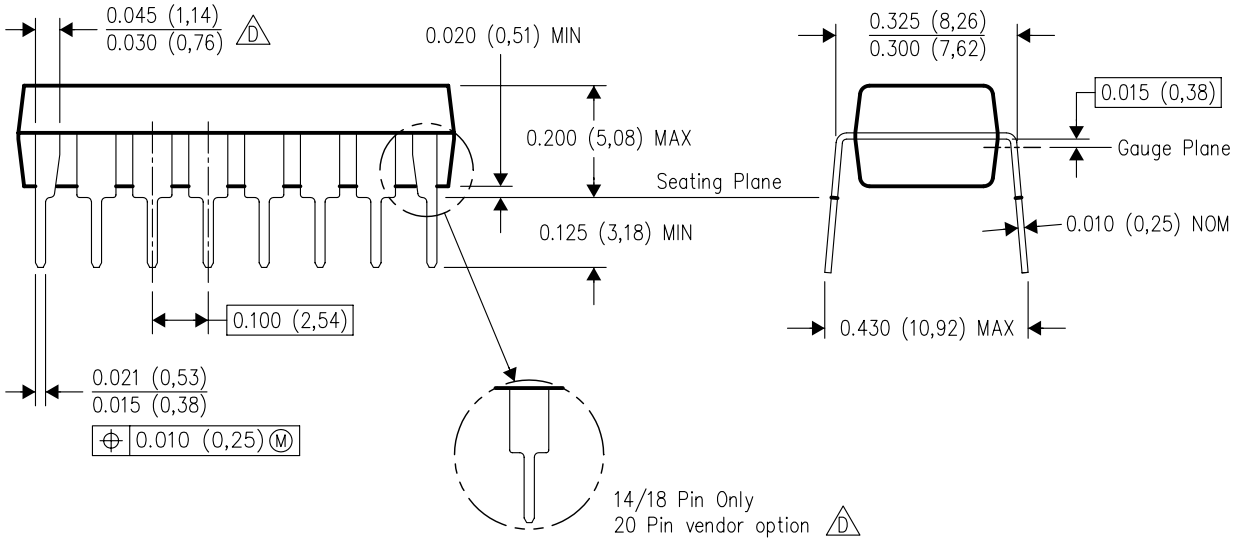
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



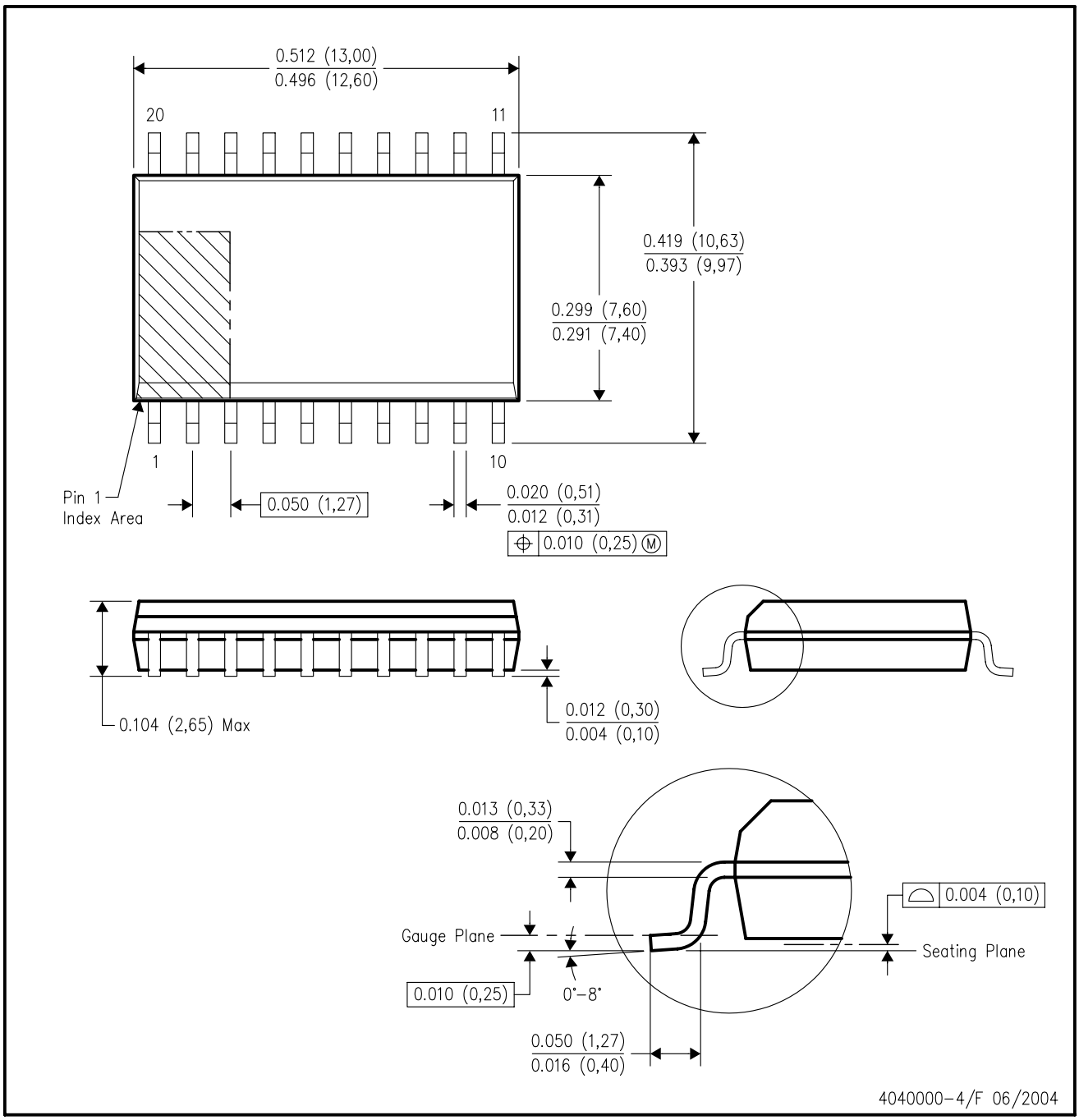
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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