

MC10EP16T, MC100EP16T

3.3V / 5V ECL Differential Receiver/Driver with Internal Termination

The EP16T is a world-class differential receiver/driver. The device is functionally equivalent to the EP16 with internal termination resistors. A 50 Ω resistor is connected from the D input to the VT pin and from the \bar{D} input to the \bar{VT} pin. Tie the VT and \bar{VT} pins to VTT supply ($V_{CC} - 2\text{ V}$) for parallel termination or connect VT and \bar{VT} pins for 100 Ω input series termination.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

The 100 Series contains temperature compensation.

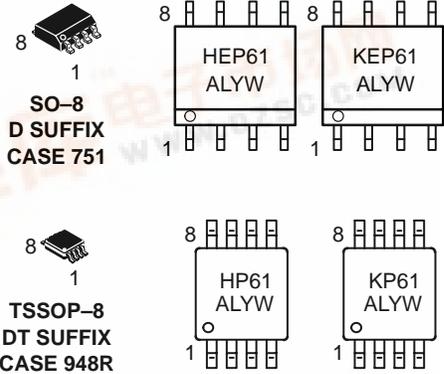
- 220 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V}$ to 5.5 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V}$ to -5.5 V
- Internal 50 Ω Termination Resistors



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MARKING DIAGRAMS*



H = MC10 L = Wafer Lot
 K = MC100 Y = Year
 A = Assembly Location W = Work Week

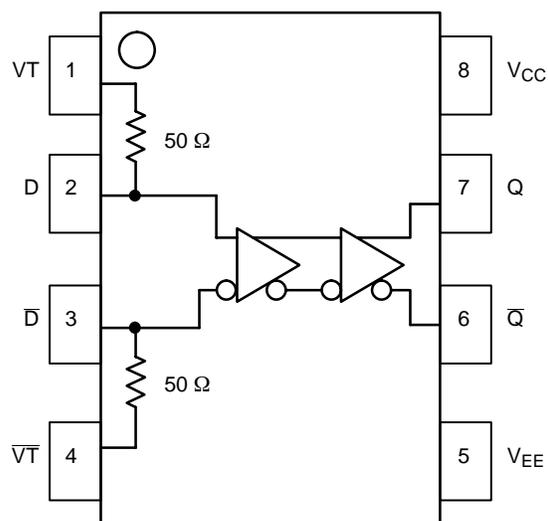
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP16TD	SO-8	98 Units/Rail
MC10EP16TDR2	SO-8	2500 Tape & Reel
MC100EP16TD	SO-8	98 Units/Rail
MC100EP16TDR2	SO-8	2500 Tape & Reel
MC10EP16TDT	TSSOP-8	100 Units/Rail
MC10EP16TDR2	TSSOP-8	2500 Tape & Reel
MC100EP16TDT	TSSOP-8	100 Units/Rail
MC100EP16TDR2	TSSOP-8	2500 Tape & Reel



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PIN DESCRIPTION

PIN	FUNCTION
D, \bar{D}	ECL Data Inputs
Q, \bar{Q}	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
VT	50 Ω Termination Resistor to D
$\bar{V}T$	50 Ω Termination Resistor to \bar{D}

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL-94 V-0 @ 0.125 in
Transistor Count	167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which device damage may occur.

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10EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	16	23	31	16	23	31	16	23	31	mA
V_{OH}	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

3. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

4. All loading with 50 Ω to V_{CC} -2.0 volts.

5. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	16	23	31	16	23	31	16	23	31	mA
V_{OH}	Output HIGH Voltage (Note 7)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 7)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.0		5.0	2.0		5.0	2.0		5.0	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.

7. All loading with 50 Ω to V_{CC} -2.0 volts.

8. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	16	23	31	16	23	31	16	23	31	mA
V_{OH}	Output HIGH Voltage (Note 10)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 10)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

9. Input and output parameters vary 1:1 with V_{CC} .

10. All loading with 50 Ω to V_{CC} -2.0 volts.

11. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 12)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	25	35	20	27	37	22	29	39	mA
V_{OH}	Output HIGH Voltage (Note 13)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 13)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	2.0		3.3	2.0		3.3	2.0		3.3	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

12. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

13. All loading with 50 Ω to V_{CC} -2.0 volts.

14. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 15)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	25	35	20	27	37	22	29	39	mA
V_{OH}	Output HIGH Voltage (Note 16)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 16)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 17)	2.0		5.0	2.0		5.0	2.0		5.0	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

15. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +2.0 V to -0.5 V.

16. All loading with 50 Ω to V_{CC} -2.0 volts.

17. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 18)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	25	35	20	27	37	22	29	39	mA
V_{OH}	Output HIGH Voltage (Note 19)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 19)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
R_T	Internal Termination Resistor	43		57	43	50	57	43		57	Ω
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	-150			-150			-150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

18. Input and output parameters vary 1:1 with V_{CC} .

19. All loading with 50 Ω to V_{CC} -2.0 volts.

20. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 21)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Frequency (See Figure 2 F_{\max}/JITTER)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	150	230	300	150	240	300	200	275	350	ps
t_{SKEW}	Duty Cycle Skew (Note 22)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2 F_{\max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, \bar{Q}	70	120	170	80	130	180	100	140	200	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC}-2.0\text{ V}$.

22. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

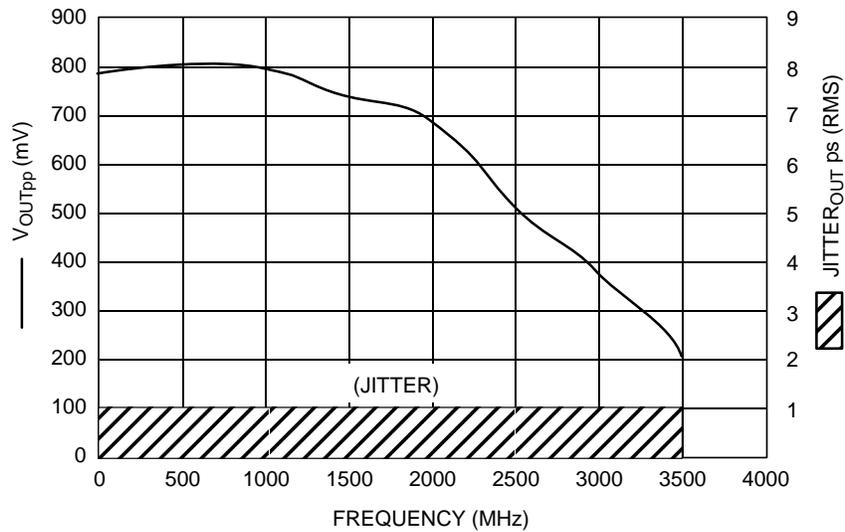
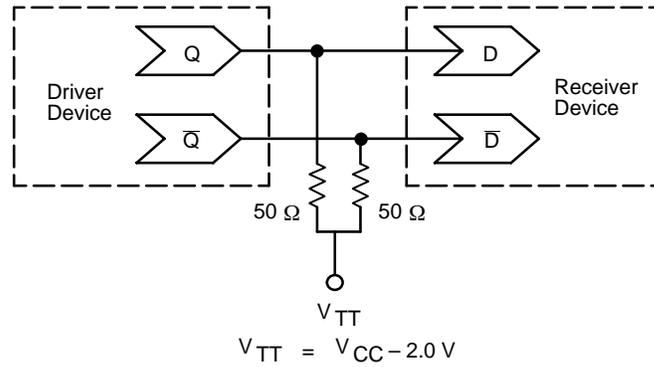


Figure 2. F_{\max}/Jitter

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**Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)**

Resource Reference of Application Notes

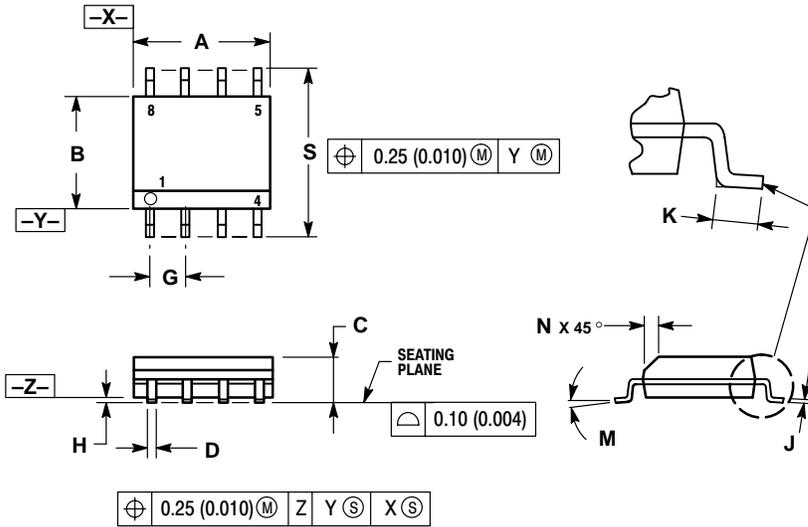
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

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PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA

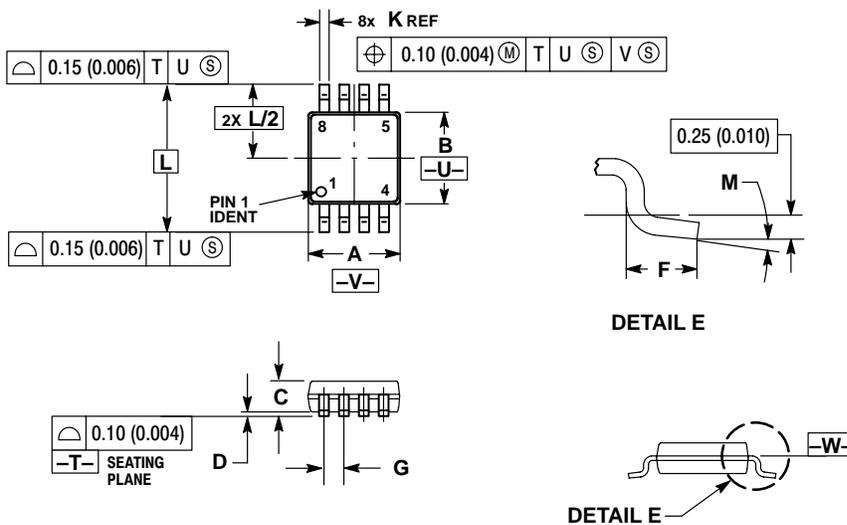


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0° - 8°		0° - 8°	
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0° - 6°		0° - 6°	

MC10EP16T, MC100EP16T

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