



SCCS031 - July 1994 - Revised March 2000

CY54/74FCT646T

8-Bit Registered Transceiver

Features

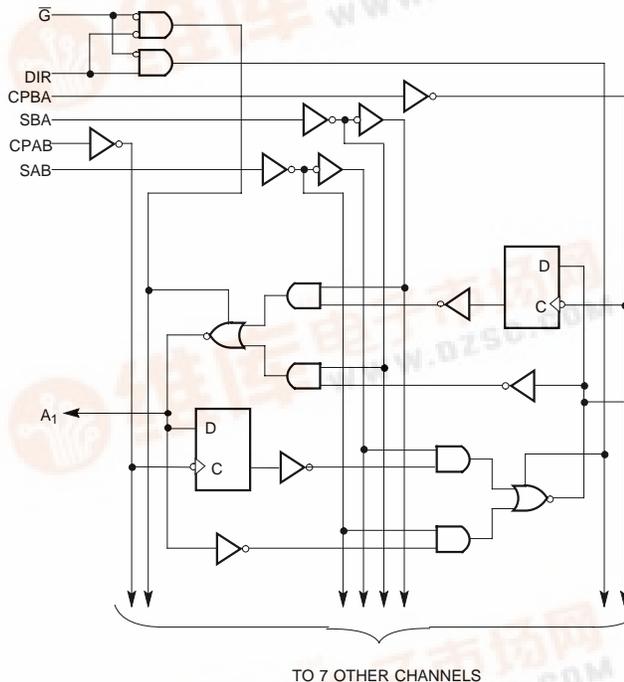
- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.4 ns max. (Com'l)
FCT-A speed at 6.3 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature permits live insertion
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Sink current 64 mA (Com'l), 48 mA (Mil)
Source current 32 mA (Com'l), 12 mA (Mil)
- Independent register for A and B buses
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$

Functional Description

The FCT646T consists of a bus transceiver circuit with three-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Enable Control \bar{G} and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control \bar{G} is Active LOW. In the isolation mode (enable Control \bar{G} HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

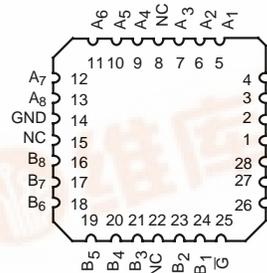
The outputs of the FCT646T are designed with a power-off disable feature to allow for live insertion of boards.

Function Block Diagrams



Pin Configurations

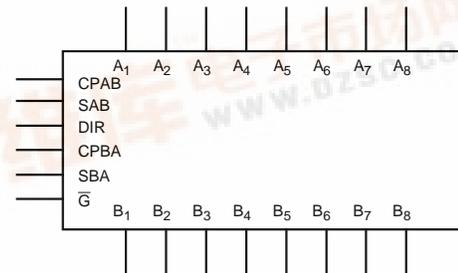
LCC Top View



QSOP, SOIC Top View



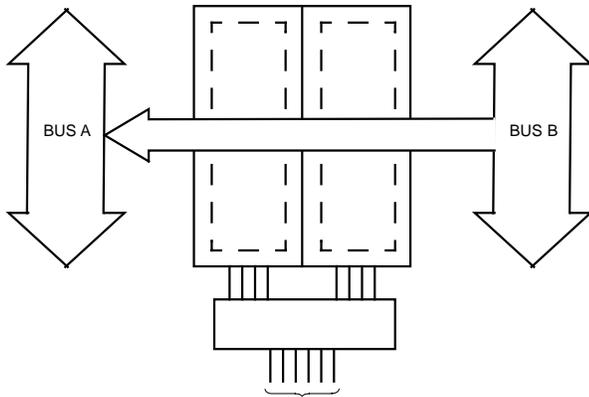
Logic Block Diagram



Pin Description

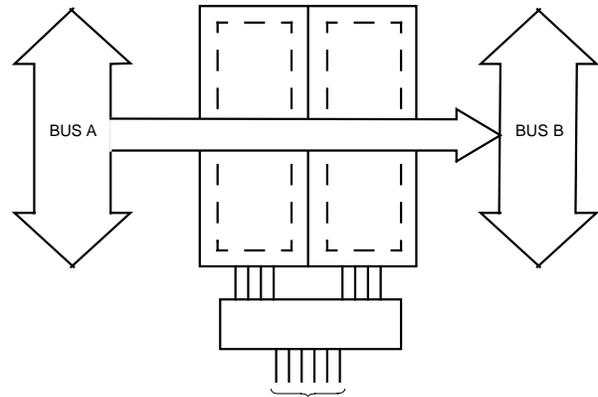
Name	Description
A	Data Register A Inputs, Data Register B Outputs
B	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, \bar{G}	Output Enable Inputs





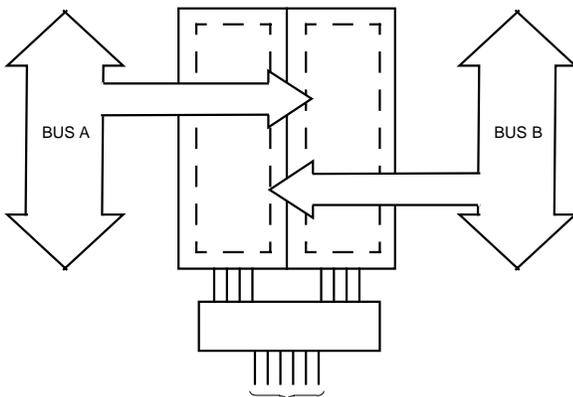
DIR L \bar{G} L CPAB X CPBA X SAB X SBA L

Real-Time Transfer
Bus B to Bus A



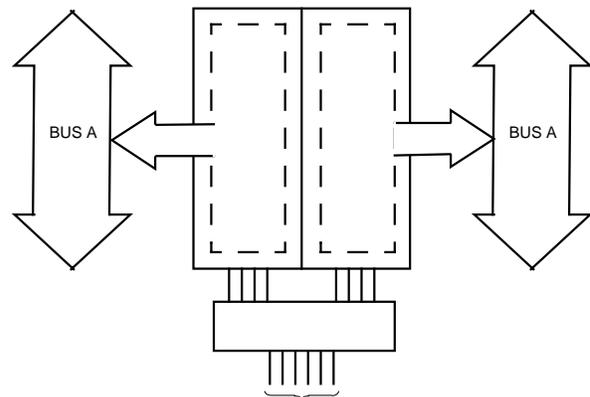
DIR H \bar{G} L CPAB X CPBA X SAB L SBA X

Real-Time Transfer
Bus A to Bus B



DIR H L X \bar{G} L L H CPAB \lceil X \lceil CPBA X \lceil \lceil SAB X X X SBA X X X

Storage from
A and/or B



DIR^[1] L H \bar{G} L L CPAB X H or L CPBA H or L X SAB X H SBA H X

Transfer Stored Data
to A and/or B

Function Table^[2]

Inputs						Data I/O ^[3]		Operation or Function
\bar{G}	DIR	CPAB	CPBA	SAB	SBA	A ₁ thru A ₈	B ₁ thru B ₈	FCT646T
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	\lceil	\lceil	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

Notes:

1. Cannot transfer data to A bus and B bus simultaneously.
2. H = HIGH Voltage Level, L = LOW Voltage Level, \lceil = LOW-to-HIGH Transition, X = Don't Care.
3. The data output functions may be enabled or disabled by various signals at the \bar{G} or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

Maximum Ratings^[4, 5]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -65°C to +135°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) 120 mA

Power Dissipation 0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	All	-40°C to +85°C	5V ± 5%
Military ^[6]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[7]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	Com'l	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	Mil	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA	Com'l		0.3	0.55	V
		V _{CC} =Min., I _{OL} =48 mA	Mil		0.3	0.55	V
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[8]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current ^[8]	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current ^[8]	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OS}	Output Short Circuit Current ^[9]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Capacitance^[8]

Parameter	Description	Typ. ^[7]	Max.	Unit
C _{IN}	Input Capacitance	6	10	pF
C _{OUT}	Output Capacitance	8	12	pF

Notes:

- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[7]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$, $V_{IN}\leq 0.2\text{V}$, $V_{IN}\geq V_{CC}-0.2\text{V}$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$, $V_{IN}=3.4\text{V}$, $f_1=0$, Outputs Open ^[10]	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[11]	$V_{CC}=\text{Max.}$, One Input Toggling, 50% Duty Cycle, Outputs Open, $\bar{G}=\text{DIR}=\text{GND}$, $\text{GAB}=\text{GBA}=\text{GND}$, $V_{IN}\leq 0.2\text{V}$ or $V_{IN}\geq V_{CC}-0.2\text{V}$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current ^[12]	$V_{CC}=\text{Max.}$, $f_0=10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz}$, $\bar{G}=\text{DIR}=\text{GND}$, $\text{GAB}=\text{GBA}=\text{GND}$, $V_{IN}\leq 0.2\text{V}$ or $V_{IN}\geq V_{CC}-0.2\text{V}$	0.7	1.4	mA
		$V_{CC}=\text{Max.}$, $f_0=10\text{ MHz}$, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5\text{ MHz}$, $\bar{G}=\text{DIR}=\text{GND}$, $\text{GAB}=\text{GBA}=\text{GND}$, $V_{IN}=3.4\text{V}$ or $V_{IN}=\text{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}$, $f_0=10\text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz}$, $\bar{G}=\text{DIR}=\text{GND}$, $\text{GAB}=\text{GBA}=\text{GND}$, $V_{IN}\leq 0.2\text{V}$ or $V_{IN}\geq V_{CC}-0.2\text{V}$	2.8	5.6 ^[13]	mA
		$V_{CC}=\text{Max.}$, $f_0=10\text{ MHz}$, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=5\text{ MHz}$, $\bar{G}=\text{DIR}=\text{GND}$, $\text{GAB}=\text{GBA}=\text{GND}$, $V_{IN}=3.4\text{V}$ or $V_{IN}=\text{GND}$	5.1	14.6 ^[13]	mA

Notes:

10. Per TTL driven input ($V_{IN}=3.4\text{V}$); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4\text{V}$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamperes and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[14]

Parameter	Description	FCT646T				FCT646AT		Unit	Fig. No. ^[15]
		Military		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	2.0	11.0	1.5	9.0	1.5	6.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	2.0	15.0	1.5	14.0	1.5	9.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time \bar{G} to Bus and DIR to Bus	2.0	11.0	1.5	9.0	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	2.0	10.0	1.5	9.0	1.5	6.3	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	1.5	11.0	1.5	7.7	ns	1, 5
t _S	Set-Up Time HIGH or LOW, Bus to Clock	4.5		4.0		2.0		ns	4
t _H	Hold Time HIGH or LOW, Bus to Clock	2.0		2.0		1.5		ns	4
t _W	Pulse Width, HIGH or LOW ^[8]	6.0		6.0		5.0		ns	5

Parameter	Description	FCT646CT				Unit	Fig. No. ^[15]
		Military		Commercial			
		Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Bus to Bus	1.5	6.0	1.5	5.4	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time Enable to Bus and DIR to A _n or B _n	1.5	8.9	1.5	7.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time \bar{G} to Bus and DIR to Bus	1.5	7.7	1.5	6.3	ns	1, 7, 8
t _{PLH} t _{PHL}	Propagation Delay Clock to Bus	1.5	6.3	1.5	5.7	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay SBA or SAB to A or B	1.5	7.0	1.5	6.2	ns	1, 5
t _S	Set-Up Time, HIGH or LOW, Bus to Clock	2.0		2.0		ns	4
t _H	Hold Time, HIGH or LOW, Bus to Clock	1.5		1.5		ns	4
t _W	Pulse Width, ^[8] HIGH or LOW	5.0		5.0		ns	5

Notes:

14. Minimum limits are specified but not tested on Propagation Delays.
15. See "Parameter Measurement Information" in the General Information Section.

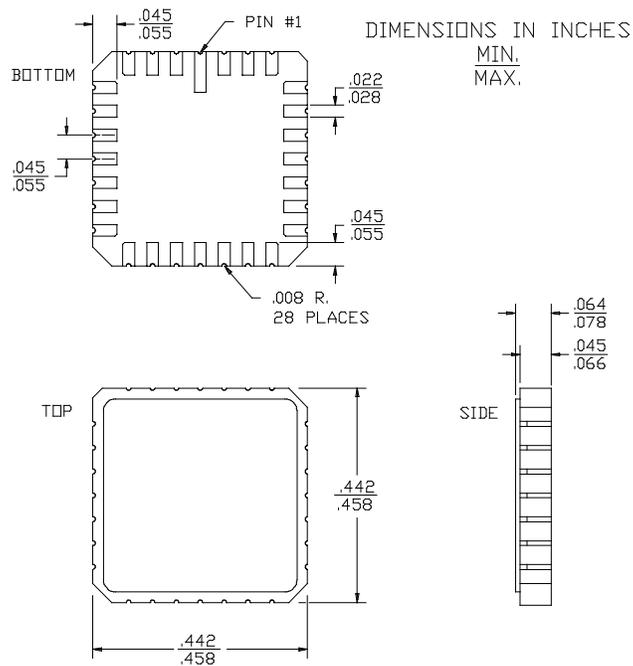
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT646CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT646CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT646CTLMB	L64	28-Square Leadless Chip Carrier	Military
6.3	CY74FCT646ATQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT646ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY74FCT646TQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT646TSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT646TLMB	L64	28-Square Leadless Chip Carrier	Military

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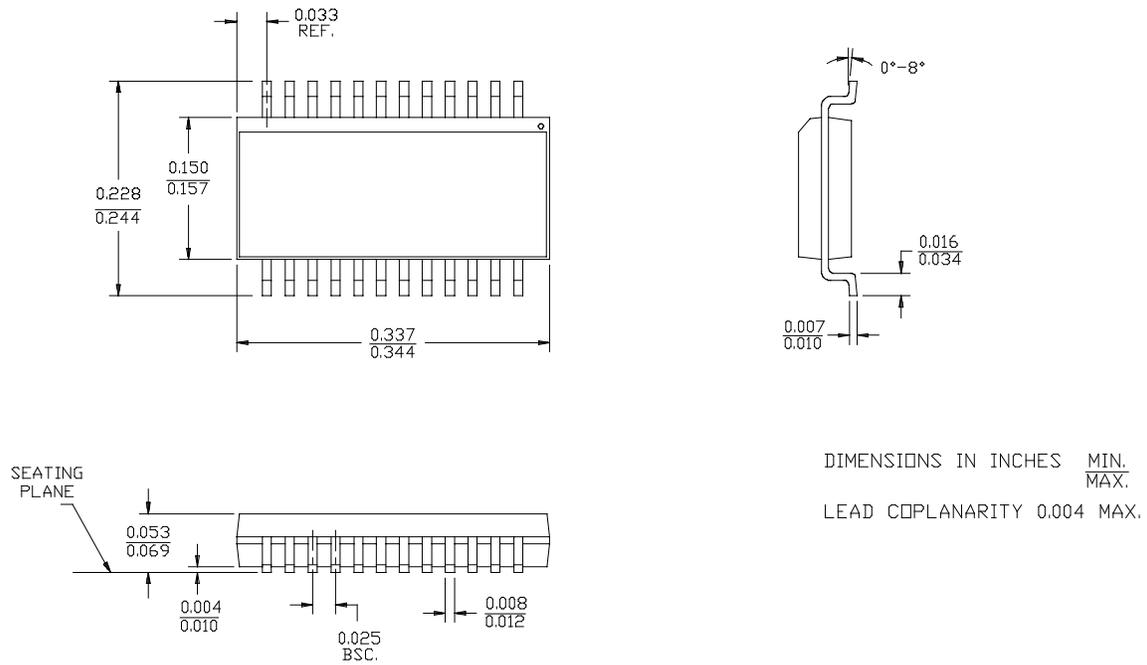
Package Diagrams
28-Square Leadless Chip Carrier L64

MIL-STD-1835 C-4

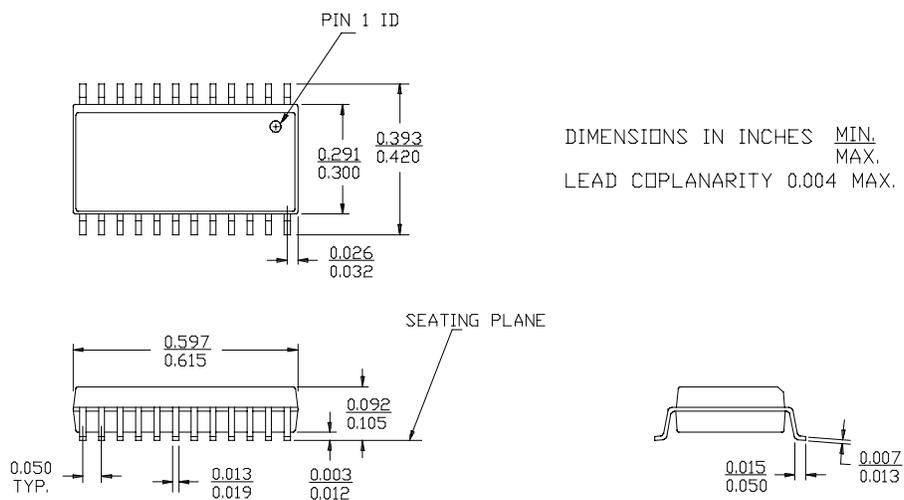


Package Diagrams (continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13



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