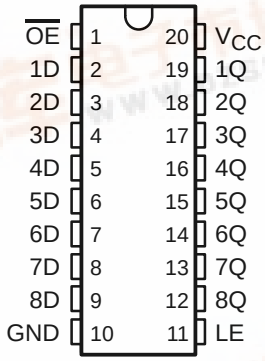
# SN54HCT573, SN74HCT573
# OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

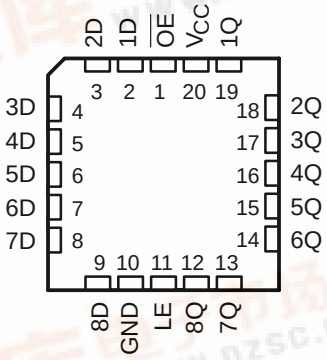
SCLS176E – MARCH 1984 – REVISED JULY 2003

- **Operating Voltage Range of 4.5 V to 5.5 V**
- **High-Current 3-State Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads**
- **Low Power Consumption, 80-μA Max $I_{CC}$**
- **Typical $t_{pd}$ = 21 ns**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **Bus-Structured Pinout**

**SN54HCT573 . . . J OR W PACKAGE**
**SN74HCT573 . . . DB, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54HCT573 . . . FK PACKAGE**
**(TOP VIEW)**




## description/ordering information

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The ’HCT573 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

### ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74HCT573N | SN74HCT573N |
| | SOIC – DW | Tube | SN74HCT573DW | HCT573 |
| | | Tape and reel | SN74HCT573DWR | |
| | SOP – NS | Tape and reel | SN74HCT573NSR | HCT573 |
| | SSOP – DB | Tape and reel | SN74HCT573DBR | HT573 |
| | TSSOP – PW | Tube | SN74HCT573PW | HT573 |
| | | Tape and reel | SN74HCT573PWR | |
| –55°C to 125°C | CDIP – J | Tube | SNJ54HCT573J | SNJ54HCT573J |
| | CFP – W | Tube | SNJ54HCT573W | SNJ54HCT573W |
| | LCCC – FK | Tube | SNJ54HCT573FK | SNJ54HCT573FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

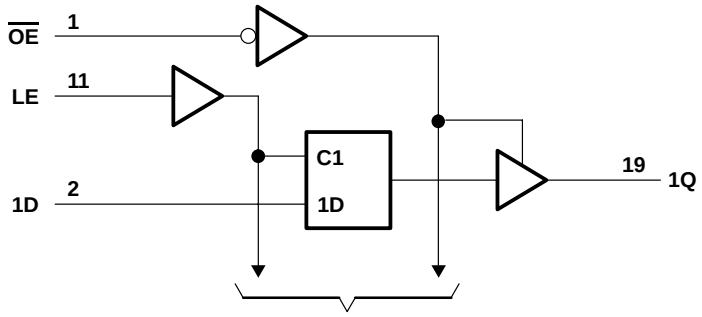
## description/ordering information (continued)

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±35 mA
Continuous current through $V_{CC}$ or GND . . . . . ±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54HCT573 | | | SN74HCT573 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | | | 0.8 | | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | | | | 500 | | | 500 | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT573 | | SN74HCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 μA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | $I_{OH}$ = –6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | | 5.5 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or 0 | | 5.5 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | | 5.5 V | | | 8 | | 160 | | 80 | μA |
| $\Delta I_{CC}$† | One input at 0.5 V or 2.4 V, Other inputs at 0 or $V_{CC}$ | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| $C_i$ | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | $V_{CC}$ | $T_A$ = 25°C | | SN54HCT573 | | SN74HCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 4.5 V | 20 | | 30 | | 25 | | ns |
| | | 5.5 V | 17 | | 27 | | 23 | | |
| $t_{su}$ | Setup time, data before LE↓ | 4.5 V | 10 | | 15 | | 13 | | ns |
| | | 5.5 V | 9 | | 14 | | 12 | | |
| $t_h$ | Hold time, data after LE↓ | 4.5 V | 5 | | 5 | | 5 | | ns |
| | | 5.5 V | 5 | | 5 | | 5 | | |

### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT573 | | SN74HCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | 4.5 V | | 25 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 21 | 32 | | 48 | | 40 | |
| | LE | Any Q | 4.5 V | | 28 | 35 | | 53 | | 44 | |
| | | | 5.5 V | | 25 | 32 | | 48 | | 40 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 4.5 V | | 26 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 23 | 32 | | 48 | | 40 | |
| $t_{dis}$ | $\overline{OE}$ | Any Q | 4.5 V | | 23 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 22 | 32 | | 48 | | 40 | |
| $t_t$ | | Any Q | 4.5 V | | 9 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |



### switching characteristics over recommended operating free-air temperature range, $C_L$ = 150 pF (unless otherwise noted) (see Figure 1)

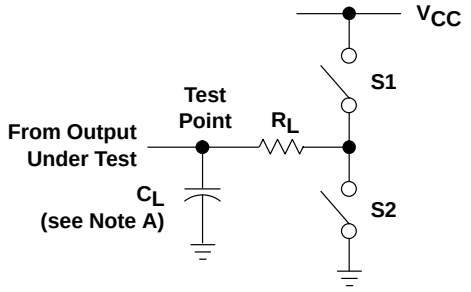
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C | | | SN54HCT573 | | SN74HCT573 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | 4.5 V | | 32 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 27 | 47 | | 71 | | 59 | |
| | LE | Any Q | 4.5 V | | 38 | 52 | | 79 | | 65 | |
| | | | 5.5 V | | 36 | 47 | | 71 | | 59 | |
| $t_{en}$ | $\overline{OE}$ | Any Q | 4.5 V | | 33 | 52 | | 79 | | 65 | ns |
| | | | 5.5 V | | 28 | 47 | | 71 | | 59 | |
| $t_t$ | | Any Q | 4.5 V | | 18 | 42 | | 63 | | 53 | ns |
| | | | 5.5 V | | 16 | 38 | | 57 | | 48 | |



### operating characteristics, $T_A$ = 25°C

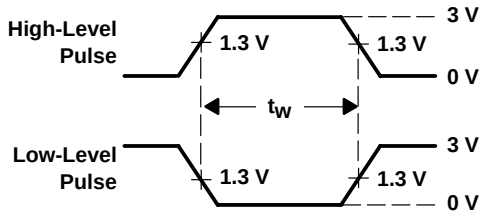
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per latch | No load | 50 | pF |

## PARAMETER MEASUREMENT INFORMATION

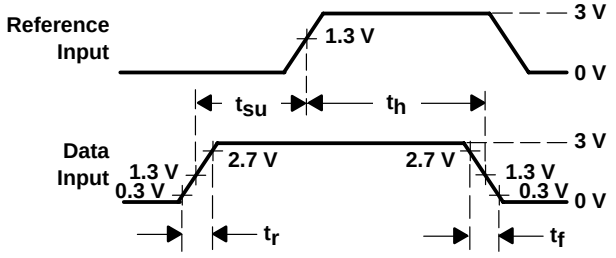



LOAD CIRCUIT

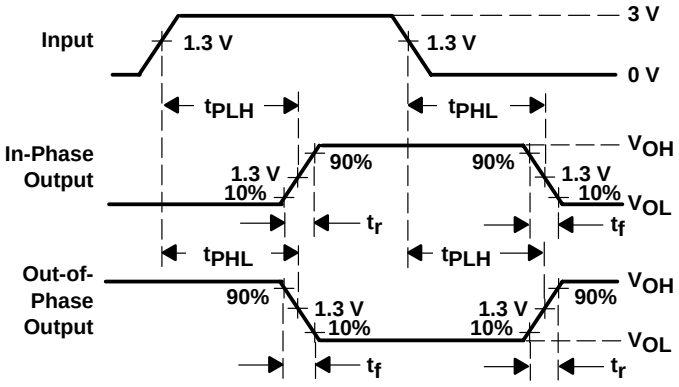
| PARAMETER | | $R_L$ | $C_L$ | S1 | S2 |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 1 kΩ | 50 pF or 150 pF | Open | Closed |
| | $t_{PZL}$ | | | Closed | Open |
| $t_{dis}$ | $t_{PHZ}$ | 1 kΩ | 50 pF | Open | Closed |
| | $t_{PLZ}$ | | | Closed | Open |
| $t_{pd}$ or $t_t$ | | –– | 50 pF or 150 pF | Open | Open |



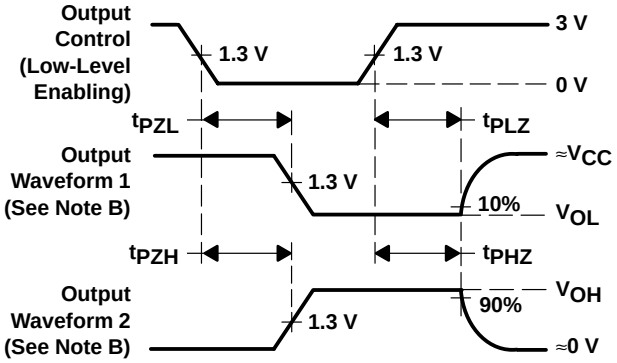

VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

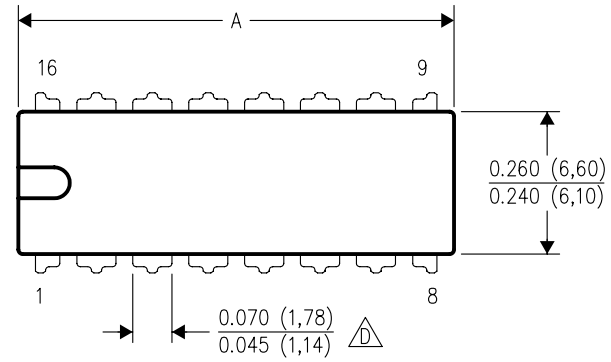
NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

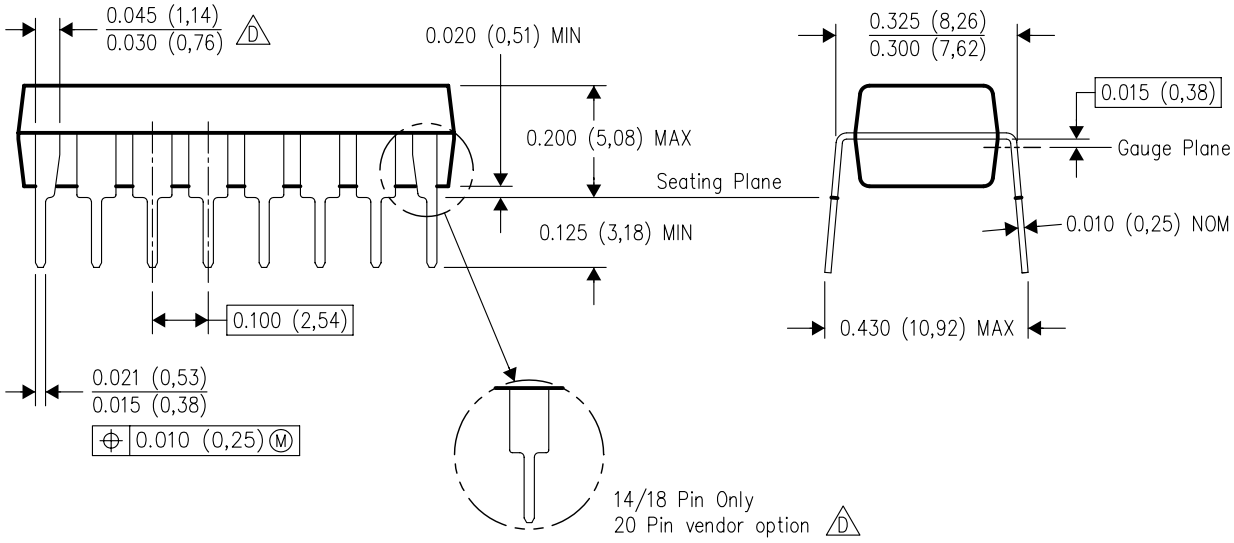
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



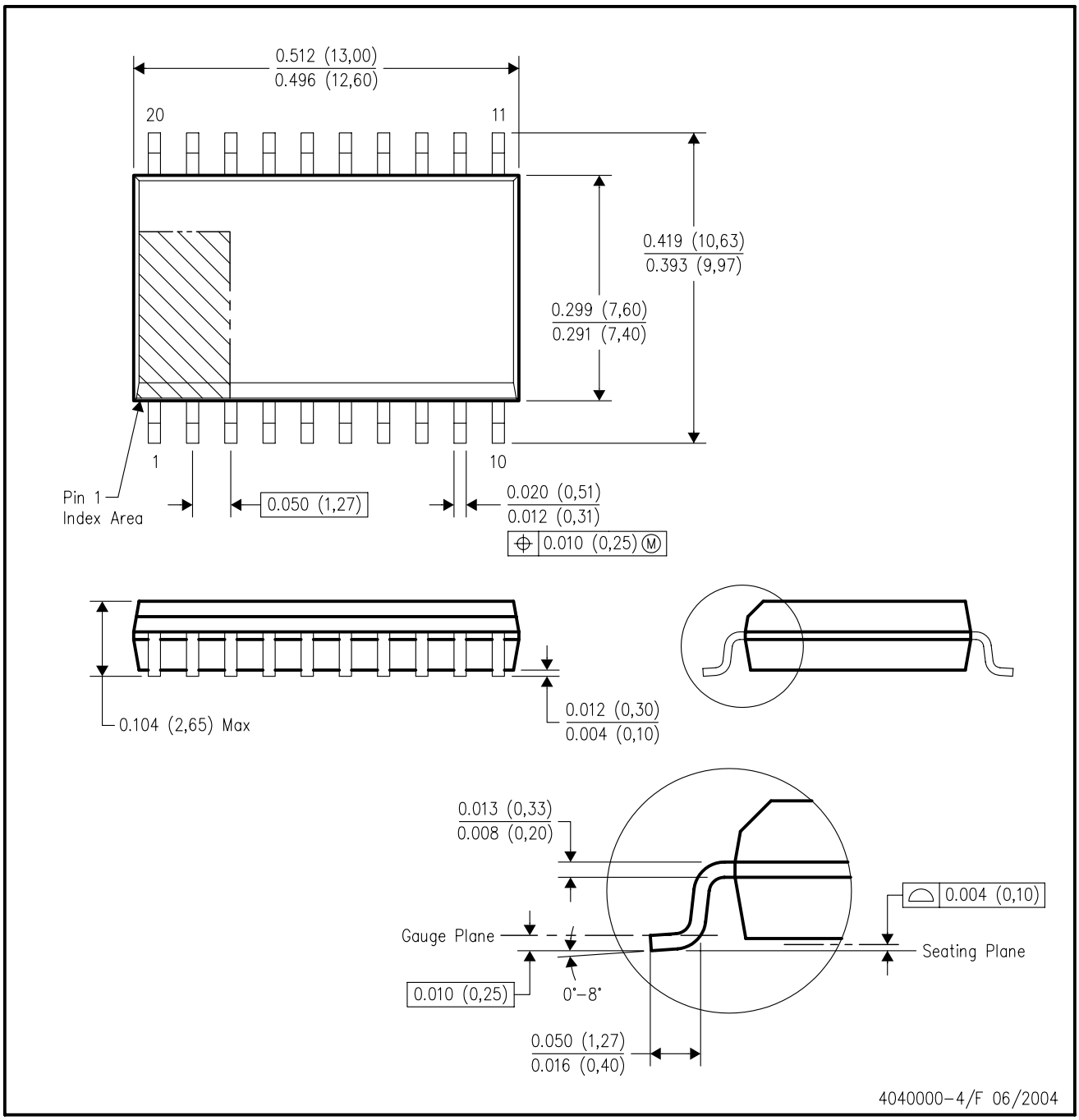

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

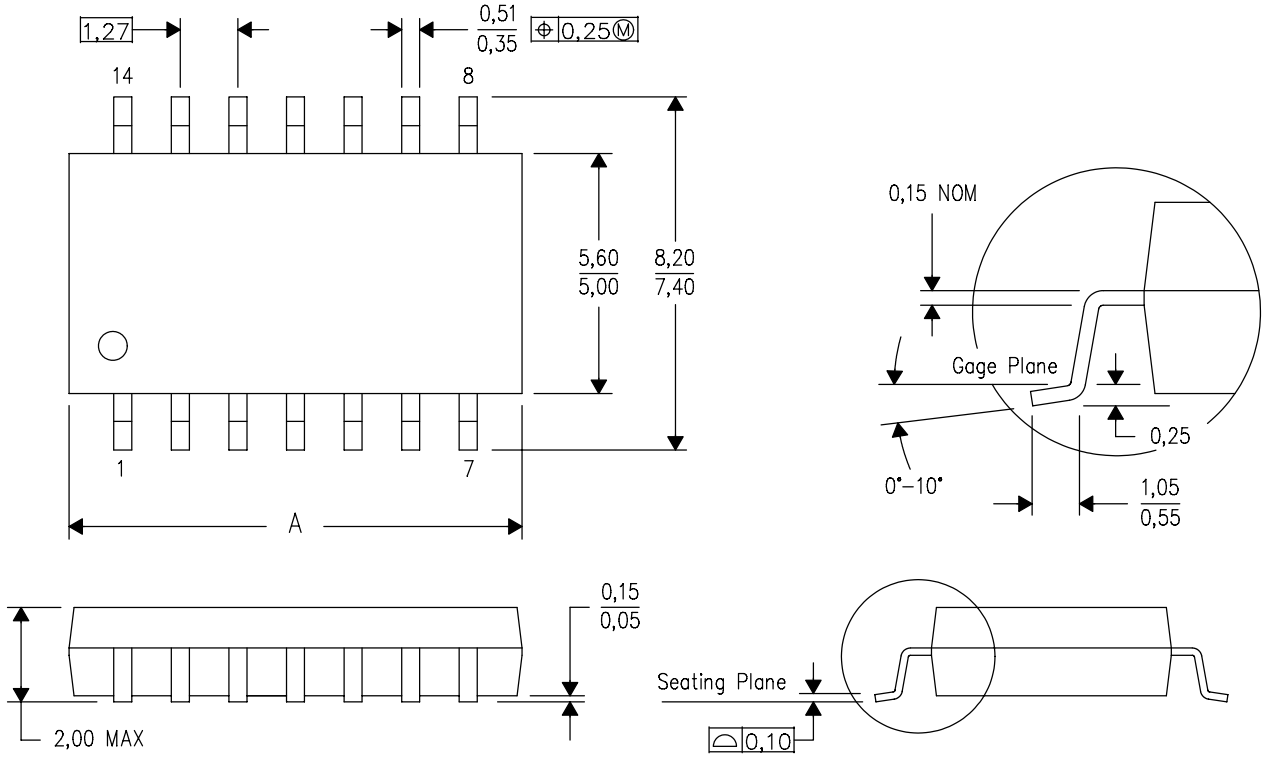



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

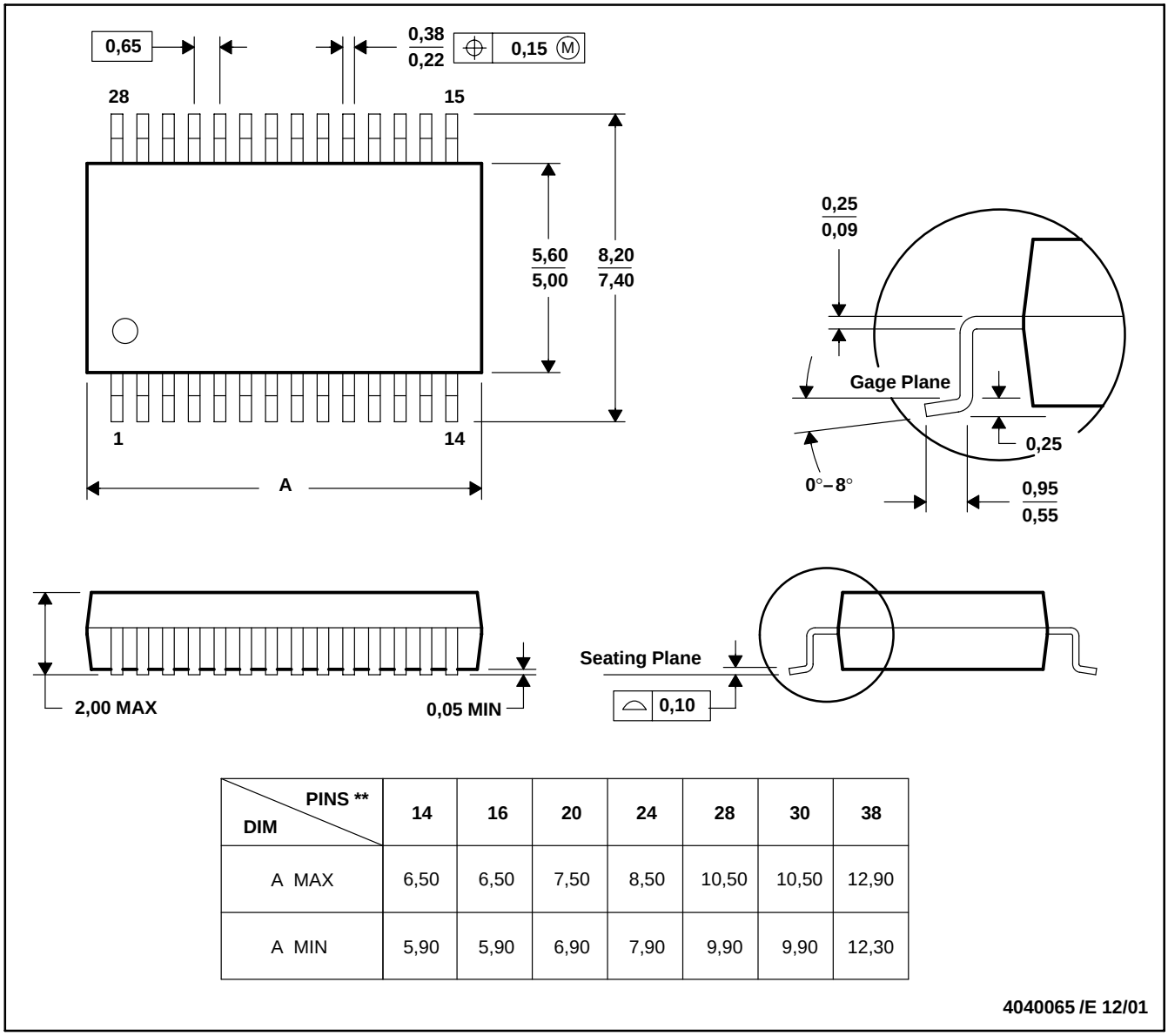
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**



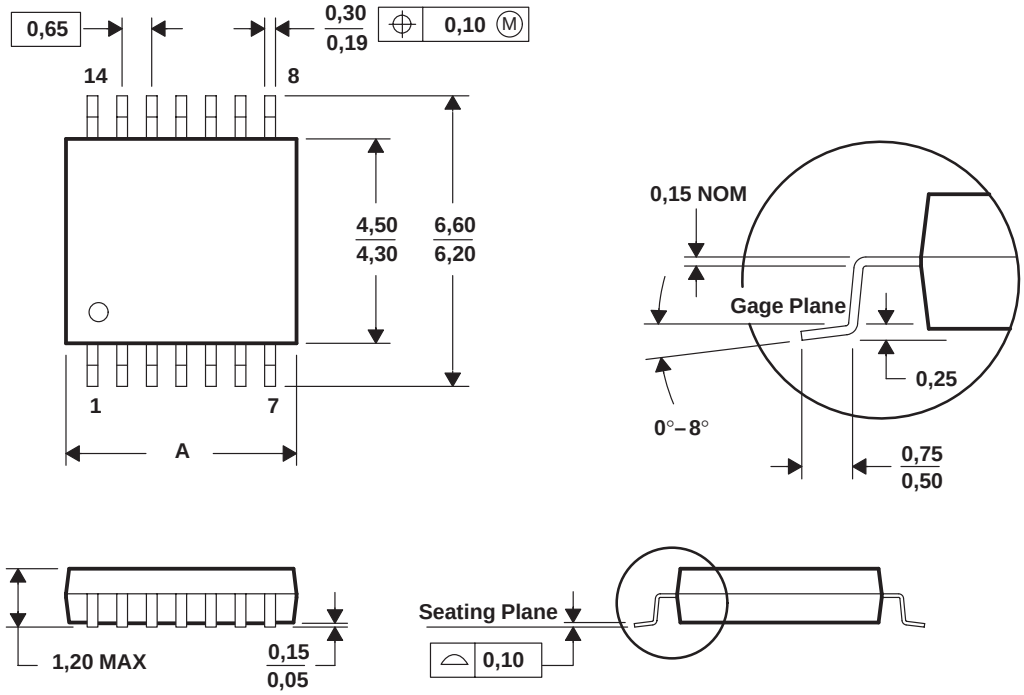

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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