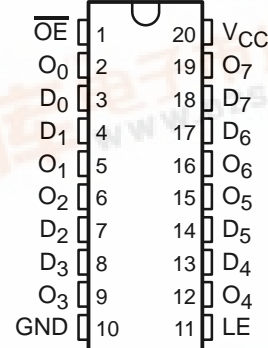# CY74FCT2373T
8-BIT LATCH
WITH 3-STATE OUTPUTS

SCCS039B – SEPTEMBER 1994 – REVISED OCTOBER 2001

- **Function and Pinout Compatible With the Fastest Bipolar Logic**
- **25-Ω Output Series Resistors Reduce Transmission-Line Reflection Noise**
- **Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **3-State Outputs**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **12-mA Output Sink Current**
  15-mA Output Source Current

Q OR SO PACKAGE
(TOP VIEW)

```
          ___
   OE [ 1     20 ] V_CC
   O0 [ 2     19 ] O7
   D0 [ 3     18 ] D7
   D1 [ 4     17 ] D6
   O1 [ 5     16 ] O6
   O2 [ 6     15 ] O5
   D2 [ 7     14 ] D5
   D3 [ 8     13 ] D4
   O3 [ 9     12 ] O4
  GND [ 10    11 ] LE
```

description

The CY74FCT2373T is an 8-bit, high-speed CMOS, TTL-compatible buffered latch with 3-state outputs that is ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25-Ω termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2373T can replace the CY74FCT373T to reduce noise in an existing design.

When the latch-enable (LE) input is high, the flip-flops appear transparent to the data. Data that meets the required setup times are latched when LE transitions from high to low. Data appears on the bus when the output-enable ($\overline{OE}$) input is low. When $\overline{OE}$ is high, the bus output is in the high-impedance state. In this mode, data can be entered into the latches.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QSOP – Q	Tape and reel	4.7	CY74FCT2373CTQCT	FCT2373C
	SOIC – SO	Tube	4.7	CY74FCT2373CTSOC	FCT2373C
		Tape and reel	4.7	CY74FCT2373CTSOCT	
	QSOP – Q	Tape and reel	5.2	CY74FCT2373ATQCT	FCT2373A
	QSOP – Q	Tape and reel	8	CY74FCT2373TQCT	FCT2373

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state, Q_0 = Previous state of flip flops (Q_{0-1})

logic diagram

To Seven Other Channels
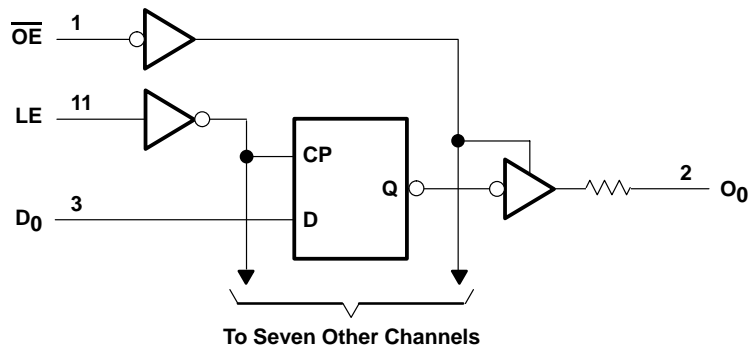
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . –0.5 V to 7 V
DC input voltage range . . . . –0.5 V to 7 V
DC output voltage range . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): Q package . . . . 68°C/W
SO package . . . . 58°C/W
Ambient temperature range with power applied, T_A . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 2:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_{IN} = −18 mA			−0.7	−1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −15 mA		2.4	3.3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 12 mA			0.3	0.55	V
R_{OUT}	V_{CC} = 4.75 V,	I_{OL} = 12 mA		20	28	40	Ω
V_{hys}	All inputs				0.2		V
I_I	V_{CC} = 5.25 V,	V_{IN} = V_{CC}				5	µA
I_{IH}	V_{CC} = 5.25 V,	V_{IN} = 2.7 V				±1	µA
I_{IL}	V_{CC} = 5.25 V,	V_{IN} = 0.5 V				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V				10	µA
I_{OZL}	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V				−10	µA
I_{OS}[‡]	V_{CC} = 5.25 V,	V_{OUT} = 0 V		−60	−120	−225	mA
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1	µA
I_{CC}	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} − 0.2 V		0.1	0.2	mA
ΔI_{CC}	V_{CC} = 5.25 V, V_{IN} = 3.4 V[§], f_1 = 0, Outputs open				0.5	2	mA
I_{CCD}[¶]	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}$ = GND, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V				0.06	0.12	mA/MHz
I_C[#]	V_{CC} = 5.25 V, Outputs open, $\overline{OE}$ = GND, LE = V_{CC}	One input switching at f_1 = 10 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V		0.7	1.4	mA
			V_{IN} = 3.4 V or GND		1	2.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V		1.3	2.6‖	
			V_{IN} = 3.4 V or GND		3.3	10.6‖	
C_i					6	10	pF
C_o					8	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

\# I_C = I_{CC} + $\Delta I_{CC} \times D_H \times N_T$ + $I_{CCD}(f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			CY74FCT2373T		CY74FCT2373AT		CY74FCT2373CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		6		5		5		ns
t_{su}	Setup time, D to LE	High to low	2		2		2		ns
t_h	Hold time, D to LE	High to low	1.5		1.5		1.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2373T		CY74FCT2373AT		CY74FCT2373CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	O	1.5	8	1.5	5.2	1.5	4.7	ns
t_{PHL}			1.5	8	1.5	5.2	1.5	4.7	
t_{PLH}	LE	O	2	13	2	8.5	2	5.5	ns
t_{PHL}			2	13	2	8.5	2	5.5	
t_{PZH}	$\overline{OE}$	O	1.5	11	1.5	6.5	1.5	5.5	ns
t_{PZL}			1.5	11	1.5	6.5	1.5	5.5	
t_{PHZ}	$\overline{OE}$	O	1.5	7	1.5	5.5	1.5	5	ns
t_{PLZ}			1.5	7	1.5	5.5	1.5	5	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR
3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**
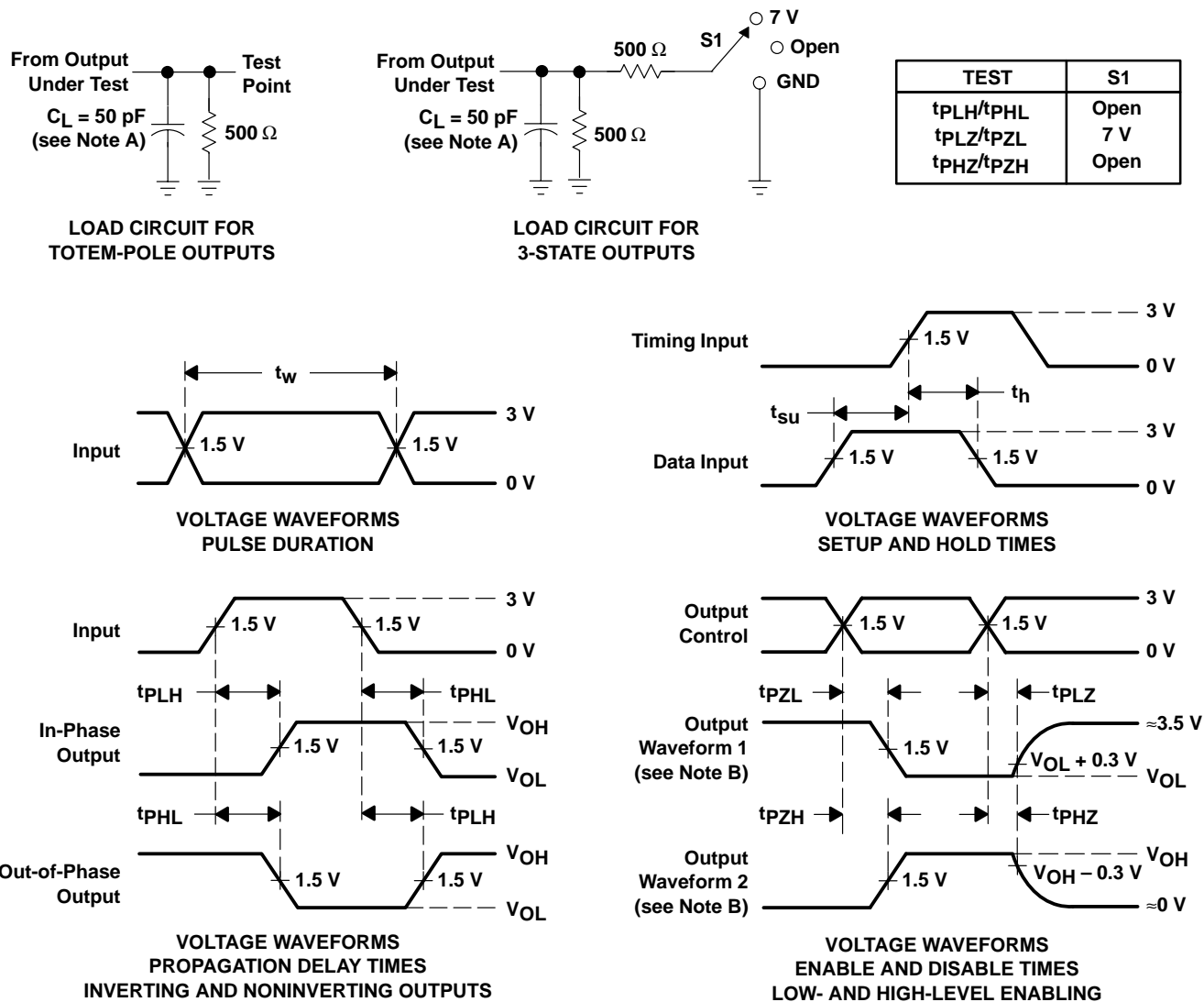
NOTES: A. C_L includes probe and jig capacitance.
       B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
          Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
       C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**TEXAS
INSTRUMENTS**

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