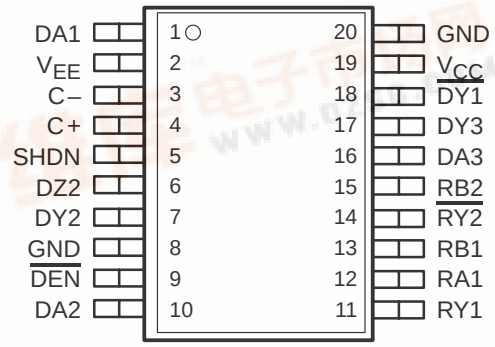
SN75LBC777
SINGLE CHIP GEOPORT™/AppleTalk™ TRANSCEIVER

SLLS227 – SEPTEMBER 1996

- **Single-Chip Interface Solution for the 9-Pin GeoPort™ Peripheral Data Circuit-Terminating Equipment (DCE) for the Intelligent Network Port**
- **Designed to Operate up to 4-Mbits/s Full Duplex**
- **Single 5-V Supply Operation**
- **10-kV ESD Protection on Bus Terminals**
- **Backward Compatible with AppleTalk™ and LocalTalk™ LANs**
- **Combines Multiple Components into a Single Chip Solution**
- **Complements the SN75LBC776 9-Terminal GeoPort Host Data Terminal Equipment (DTE) Interface Device**
- **LinBiCMOS™ Process Technology**

DW PACKAGE
(TOP VIEW)

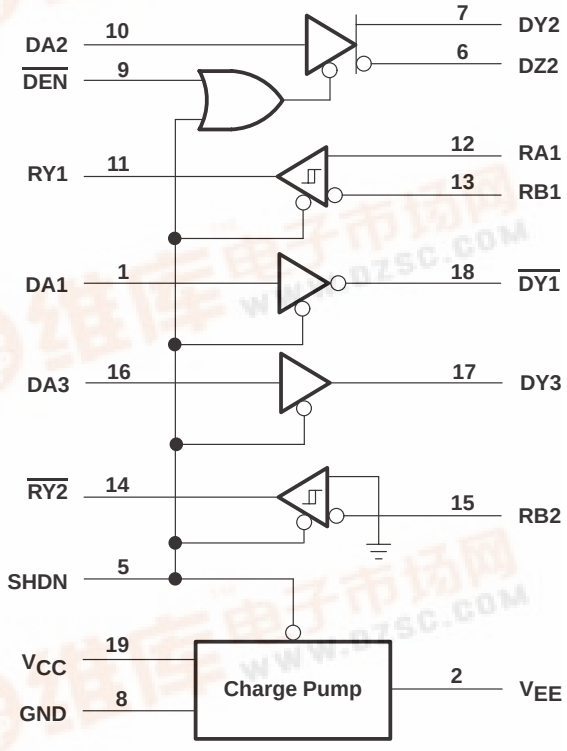


description

The SN75LBC777 is a low-power LinBiCMOS device that incorporate the drivers and receivers for a 9-pin GeoPort peripheral interface. GeoPort combines hybrid EIA/TIA-422-B and EIA/TIA-423-B drivers and receivers to transmit data up to four-Mbit/s full duplex. GeoPort is a serial communications standard that is intended to replace the RS-232, AppleTalk, and printer ports all in one connector in addition to providing real-time data transfer capability. The SN75LBC777 provides point-to-point connections between GeoPort-compatible devices with data transmission rates up to 4-Mbit/s full duplex over a 4-foot cable. Applications include connection to telephone, integrated services digital network (ISDN), digital sound and imaging, fax-data modems, and other traditional serial and parallel connections. The GeoPort is backwardly compatible to both LocalTalk and AppleTalk LANs.

While the SN75LBC777 is powered off (V_{CC} = 0) the outputs are in a high-impedance state. When the shutdown (SHDN) terminal is high, the charge pump is powered down and the outputs are in a high-impedance state. When high, the driver enable ($\overline{DEN}$) terminal puts the outputs of the differential driver into a high-impedance state.

logic diagram (positive logic)



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description (continued)

A switched-capacitor voltage converter generates the negative voltage required from a single 5-V supply using two 0.33-µF capacitors. One capacitor is between the C+ and C– terminals and the other is between V_{EE} and ground.

The SN75LBC777 is characterized for operation over the 0°C to 70°C temperature range.

DRIVER FUNCTION TABLE

INPUTS			ENABLE		OUTPUTS			
DA1	DA2	DA3	SHDN	$\overline{DEN}$	$\overline{DY1}$	DY2	DZ2	DY3
H	X	H	L	X	L	X	X	H
L	X	L	L	X	H	X	X	L
X	H	X	L	L	X	H	L	X
X	L	X	L	L	X	L	H	X
OPEN	OPEN	OPEN	L	L	L	H	L	H
X	X	X	H	X	Z	Z	Z	Z
X	X	X	X	H	X	Z	Z	X
X	X	X	OPEN	OPEN	Z	Z	Z	Z

H = high level, L= low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

RECEIVER FUNCTION TABLE

INPUTS			ENABLE	OUTPUTS	
RA1	RB1	RB2	SHDN	RY1	$\overline{RY2}$
H	L	H	L	H	L
L	H	L	L	L	H
OPEN		OPEN	L	H	H
SHORT†		SHORT†	L	?	?
X	X	X	H	Z	Z
X	X	X	OPEN	Z	Z

† $-0.2\ V < V_{ID} < 0.2\ V$

H = high level, L= low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage range, $V_{CC,}$ (see Note 1) . . . . . –0.5 to 7 V
Negative supply voltage range, $V_{EE,}$ (see Note 1) . . . . . –7 to 0.5 V
Receiver input voltage range (RA1, RB1, RB2) . . . . . –15 V to 15 V
Receiver differential input voltage range, V_{ID} . . . . . –12 V to 12 V
Receiver output voltage range (RY1, $\overline{RY2}$) . . . . . –0.5 V to 5.5 V
Driver output voltage range (Power Off)($\overline{DY1}$, DY2, DZ2, DY3) . . . . . –15 V to 15 V
Driver output voltage range (Power On)($\overline{DY1}$, DY2, DZ2, DY3) . . . . . –11 V to 11 V
Driver input voltage range (DA, SHDN, $\overline{DEN}$) . . . . . –0.5 V to V_{CC} +0.4 V
Electrostatic discharge (see Note 2)
Bus Pins (Class 3 A) . . . . . 10 kV
Bus Pins (Class 3 B) . . . . . 600 V
All Pins (Class 3, A) . . . . . 2 kV
All Pins (Class 3 B) . . . . . 200 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages values are with respect to the network ground terminal unless otherwise noted.
2. This rating is measured using MIL-STD-883C Method, 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATE FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0°C	720 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH} (DA, SHDN, $\overline{DEN}$)	2		5.25	V
Low-level input voltage, V_{IL} (DA, SHDN, $\overline{DEN}$)			0.8	V
Receiver common-mode input voltage, V_{IC}	–7		7	V
Receiver differential input voltage, V_{ID}	–12		12	V
Voltage converter filter capacitance	0.33			µF
Voltage converter filter capacitor equivalent series resistance (ESR)	0		0.2	Ω
Operating free-air temperature, T_A			70	°C

driver electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Single ended, See Figure 1	R_L = 12 kΩ		3.6	4.5		V
			R_L = 120 Ω		2	3.6		V
V_{OL}	Low-level output voltage		R_L = 12 kΩ			–4.5	–3.6	V
			R_L = 120 Ω			–2.7	–1.8	V
$\lvert V_{OD}\rvert$	Magnitude of differential output voltage $\lvert V_{DY} - V_{DZ}\rvert$		R_L = 120 Ω,	See Figure 2	4			V
$\Delta\lvert V_{OD}\rvert$	Change in differential voltage magnitude						250	mV
V_{OC}	Common-mode output voltage		See Figure 3		–1		3	V
$\lvert\Delta V_{OC(SS)}\rvert$	Magnitude of change, common-mode steady-state output voltage						200	mV
$\lvert\Delta V_{OC(PP)}\rvert$	Magnitude of change, common-mode peak-to-peak output voltage					700		mV
I_{CC}	Supply current		SHDN = $\overline{DEN}$ = 0 V,	No Load		7	15	mA
			SHDN = $\overline{DEN}$ = 5 V,	No Load			100	µA
I_{OZ}	High-impedance output current		V_{CC} = 0 or 5 V,	$-10 \le V_O \le 10$ V			±100	µA
I_{OS}	Short-circuit output current		V_{CC} = 5.25 V, See Note 3	-5 V $\le V_O \le 5$ V,		±170	±450	mA

NOTE 3: Not more than one output should be shorted at one time.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output		Single-ended, R_L = 120 Ω, See Figure 4		40	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				40	75	ns
t_{PZL}	Driver output enable time to low-level output	SHDN			25	100	µs
t_{PZH}	Driver output enable time to high-level output	SHDN			25	100	µs
t_{PLZ}	Driver output disable time from low-level output	SHDN			30	100	ns
t_{PHZ}	Driver output disable time from high-level output	SHDN			30	100	ns
t_r	Rise time			10	25	75	ns
t_f	Fall time			10	25	75	ns
t_{PHL}	Propagation delay time, high-to-low level output		Differential, R_L = 120 Ω, See Figure 5		40	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				40	75	ns
t_{PZL}	Driver output enable time to low-level output	SHDN			25	100	µs
		$\overline{DEN}$			35	100	ns
t_{PZH}	Driver output enable time to high-level output	SHDN			25	100	µs
		$\overline{DEN}$			35	150	ns
t_{PLZ}	Driver output disable time from low-level output	SHDN			30	100	ns
		$\overline{DEN}$			30	100	ns
t_{PHZ}	Driver output disable time from high-level output	SHDN			35	100	ns
		$\overline{DEN}$			35	100	ns
t_r	Rise time			10	25	75	ns
t_f	Fall time			10	25	75	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PLH} - t_{PHL} \rvert$					22	ns

receiver electrical characteristics over free-air temperature range (unless otherwise noted)

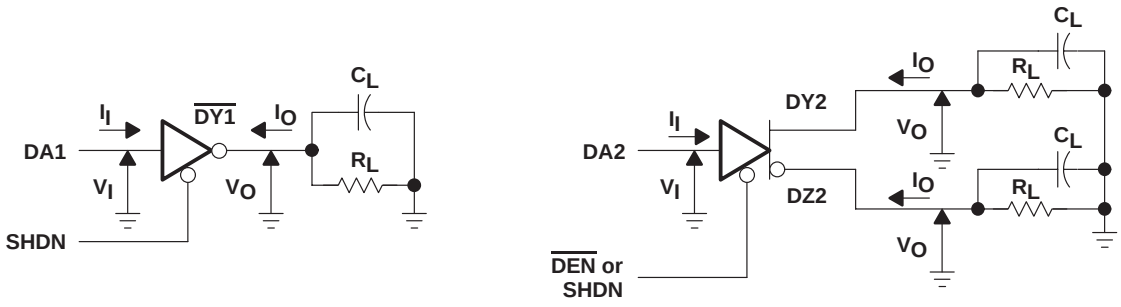
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			–200			mV
V_{hys}	Differential input voltage hysteresis ($V_{IT+} - V_{IT-}$)				50		mV
V_{OH}	High-level output voltage (see Note 4)	I_{OH} = 2 mA,	V_{IC} = 0	2	4.9		V
V_{OL}	Low-level output voltage	I_{OL} = –2 mA,	V_{IC} = 0		0.2	0.8	V
I_{OS}	Short-circuit output current	V_O = 0		–85	–45		mA
		V_O = 5.25 V			45	85	mA
R_I	Input resistance	V_{CC} = 0 or 5.25 V,	–12 V ≤ V_I ≤ 12 V	6	30		kΩ

NOTE 4: If the inputs are left unconnected, RA1 interprets this as a high-level input and RB1 and RB2 interpret this as a low-level input so that all outputs are at the high level.

receiver switching characteristics over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output	R_L = 2 kΩ, See Figure 6	C_L = 15 pF,		30	75	ns
t_{PLH}	Propagation delay time, low-to-high level output				30	75	ns
t_r	Rise time				15	30	ns
t_f	Fall time				15	30	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH}-t_{PHL}\rvert$					20	ns
t_{PZL}	Receiver output enable time to low-level output	Differential, See Figure 7	C_L = 50 pF,		35	100	ns
t_{PZH}	Receiver output enable time to high-level output				35	100	ns
t_{PLZ}	Receiver output disable time from low-level output				21	100	ns
t_{PHZ}	Receiver output disable time from high-level output				21	100	ns
t_{PZL}	Receiver output enable time to low-level output	Single-ended, See Figure 7	C_L = 50 pF,		12	25	µs
t_{PZH}	Receiver output enable time to high-level output				12	25	µs
t_{PLZ}	Receiver output disable time from low-level output				25	100	ns
t_{PHZ}	Receiver output disable time from high-level output				125	400	ns

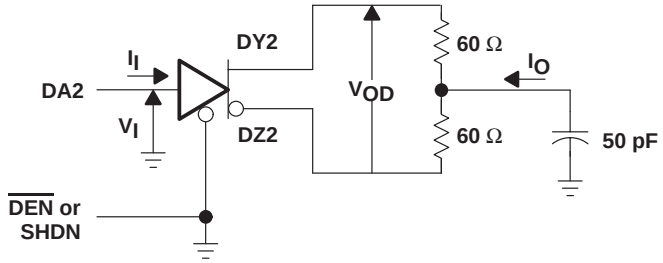
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

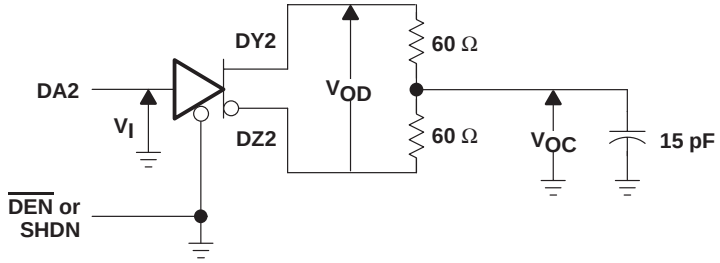
NOTES: A. C_L = 50 pF
B. Driver 3 is a noninverting version of driver 1.

Figure 1. Single-Ended Driver DC Parameter Test Circuits

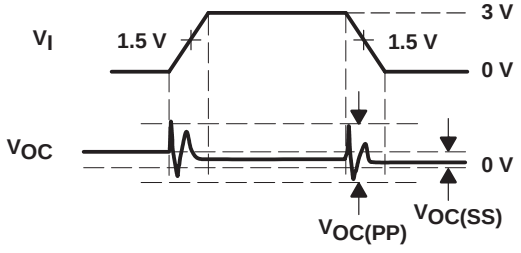


TEST CIRCUIT

Figure 2. Differential Driver DC Parameter Test Circuit



TEST CIRCUIT (see Note A)

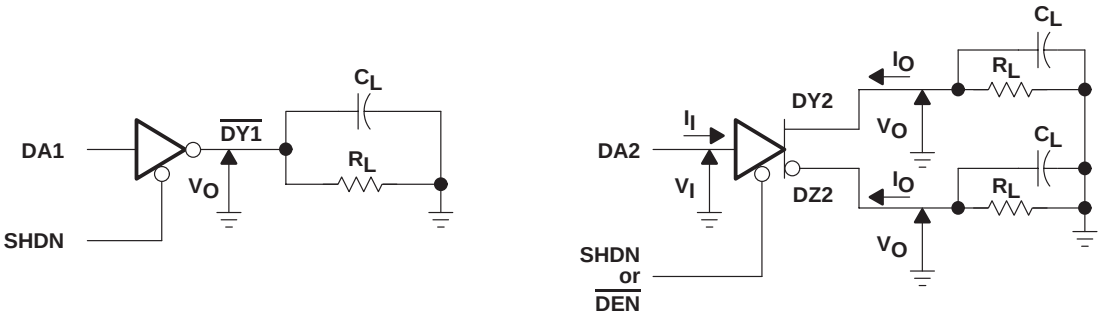


VOLTAGE WAVEFORM

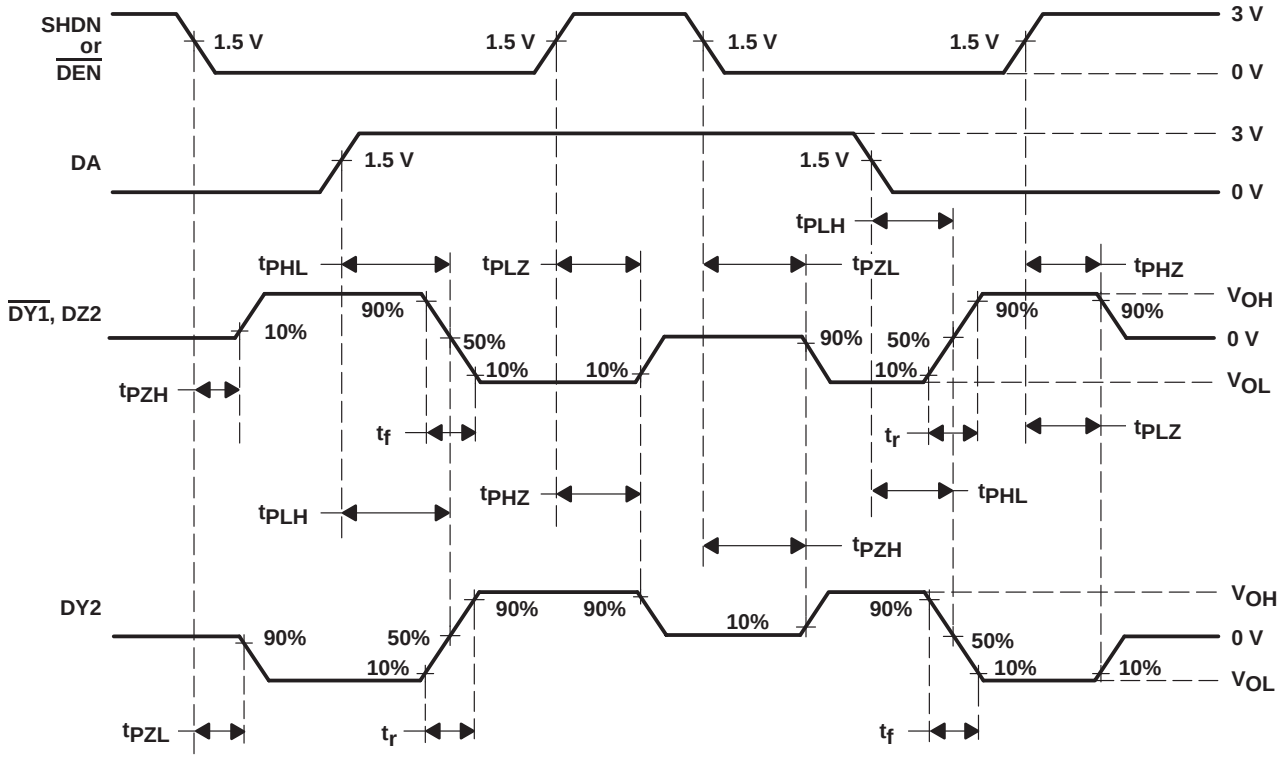
NOTE A. Measured 3dB Bandwidth = 300 MHz

Figure 3. Differential Driver Common-Mode Output Voltage Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT
(see Note A)

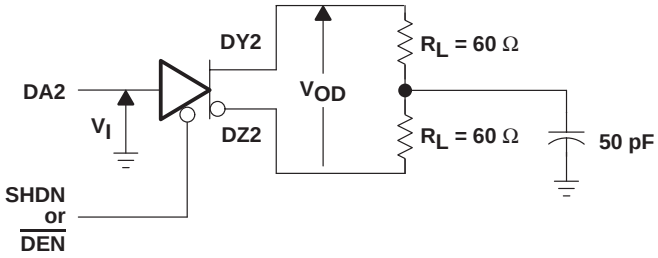


VOLTAGE WAVEFORM
(see Note B)

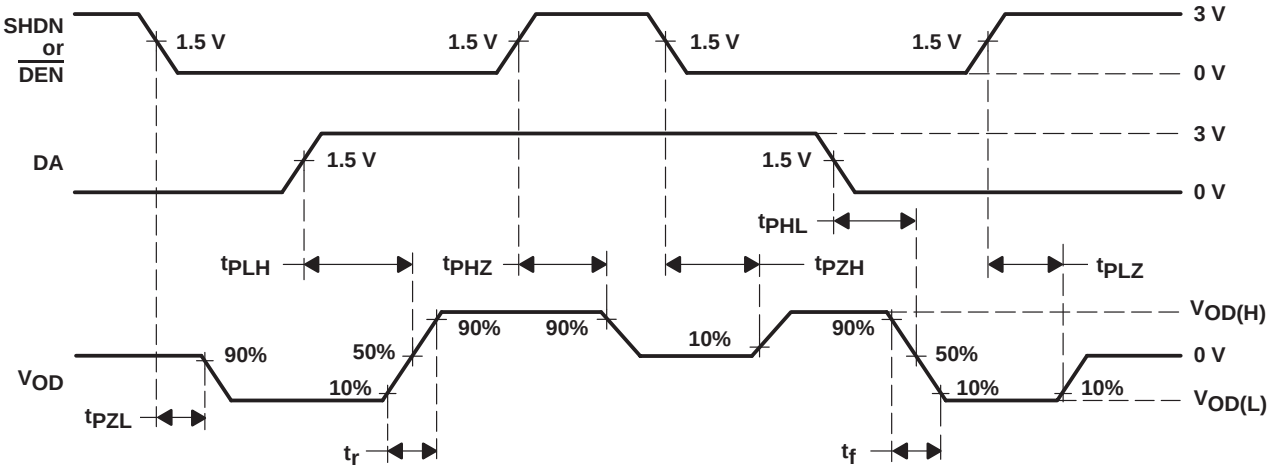
NOTES: A. C_L = 50 pF, R_L = 120 Ω
B. The input waveform t_r, $t_f \leq$ 10 ns.
C. Driver 3 is a noninverting version of driver 1.

Figure 4. Single-Ended Driver Propagation and Transition Times Test Circuits and Waveform

PARAMETER MEASUREMENT INFORMATION



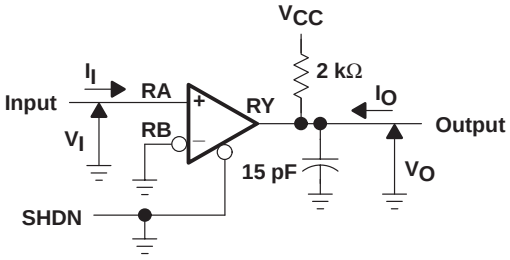
TEST CIRCUIT



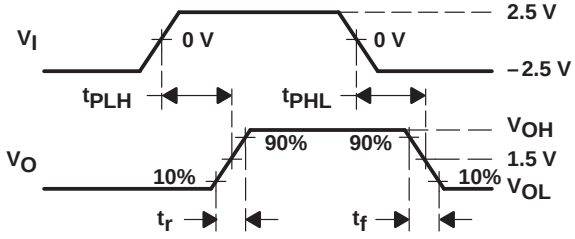
VOLTAGE WAVEFORM

NOTE A: For the input waveform t_r, t_f < = 10 ns

Figure 5. Differential Driver Propagation and Transition Times Test Circuit and Waveforms



TEST CIRCUIT

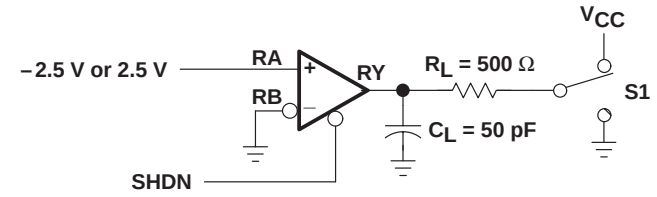


VOLTAGE WAVEFORM

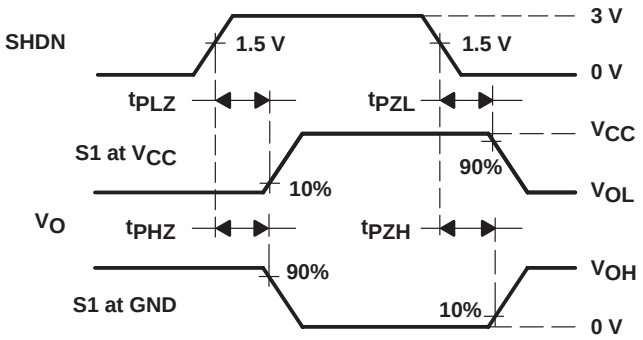
NOTE A: For the input waveform t_r, t_f < = 10 ns

Figure 6. Receiver Propagation and Transition Times Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

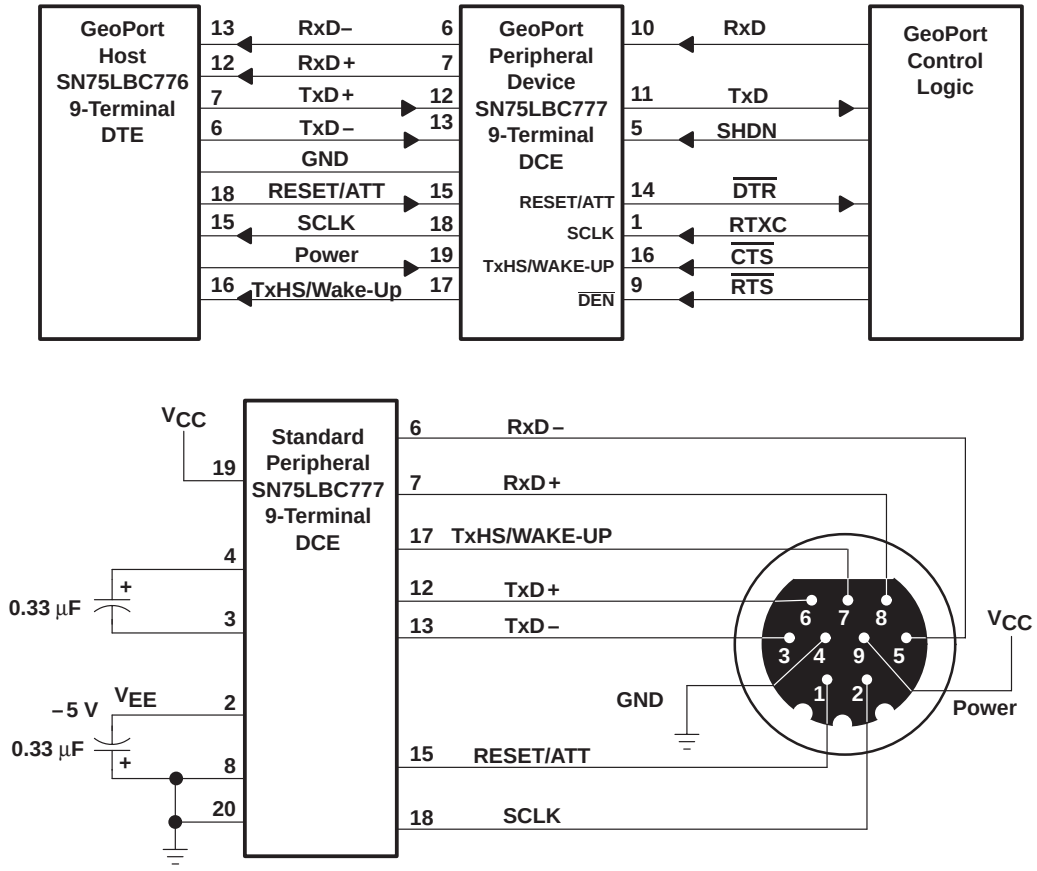


VOLTAGE WAVEFORM

NOTE A: For the input waveform t_r, t_f < = 10 ns

Figure 7. Receiver Enable and Disable Test Circuit and Waveforms

APPLICATION INFORMATION



NOTE A: A potential charge pump capacitor is the AVX 0805YC334MATXA or an equivalent.

Figure 8. GeoPort 9-terminal DCE Connection Application

generator characteristics

PARAMETER		TEST CONDITIONS	232/V.28		423/V.10		562		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$\|V_O\|$	Output voltage magnitude	Open circuit		25	4	6		13.2	V
		3 kΩ ≤ R_L ≤ 7 kΩ	5	15	NA		3.7		V
		R_L = 450 Ω	NA		3.6		NA		V
I_{OS}	Short-circuit output current	V_O = 0		100		150		60	mA
$R_{O(OFF)}$	Power-off source resistance	V_{CC} = 0, $\|V_O\|$ < 2 V	300		NA		300		Ω
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0, $\|V_O\|$ < 6 V	NA			±100	NA		µA
SR	Output voltage slew rate			30	NA		4	30	V/µs
t_t	Output transition time	±3.3 V to ±3.3 V	NA		NA		0.22	2.1	µs
		±3 V to ±3 V		0.04	NA		NA		ui†
		10% to 90%	NA			0.3	NA		ui†
$V_{O(RING)}$	Output voltage ringing		NA			10%		5%	

† ui is the unit interval and is the inverse of the signaling rate (a.k.a. bit time).

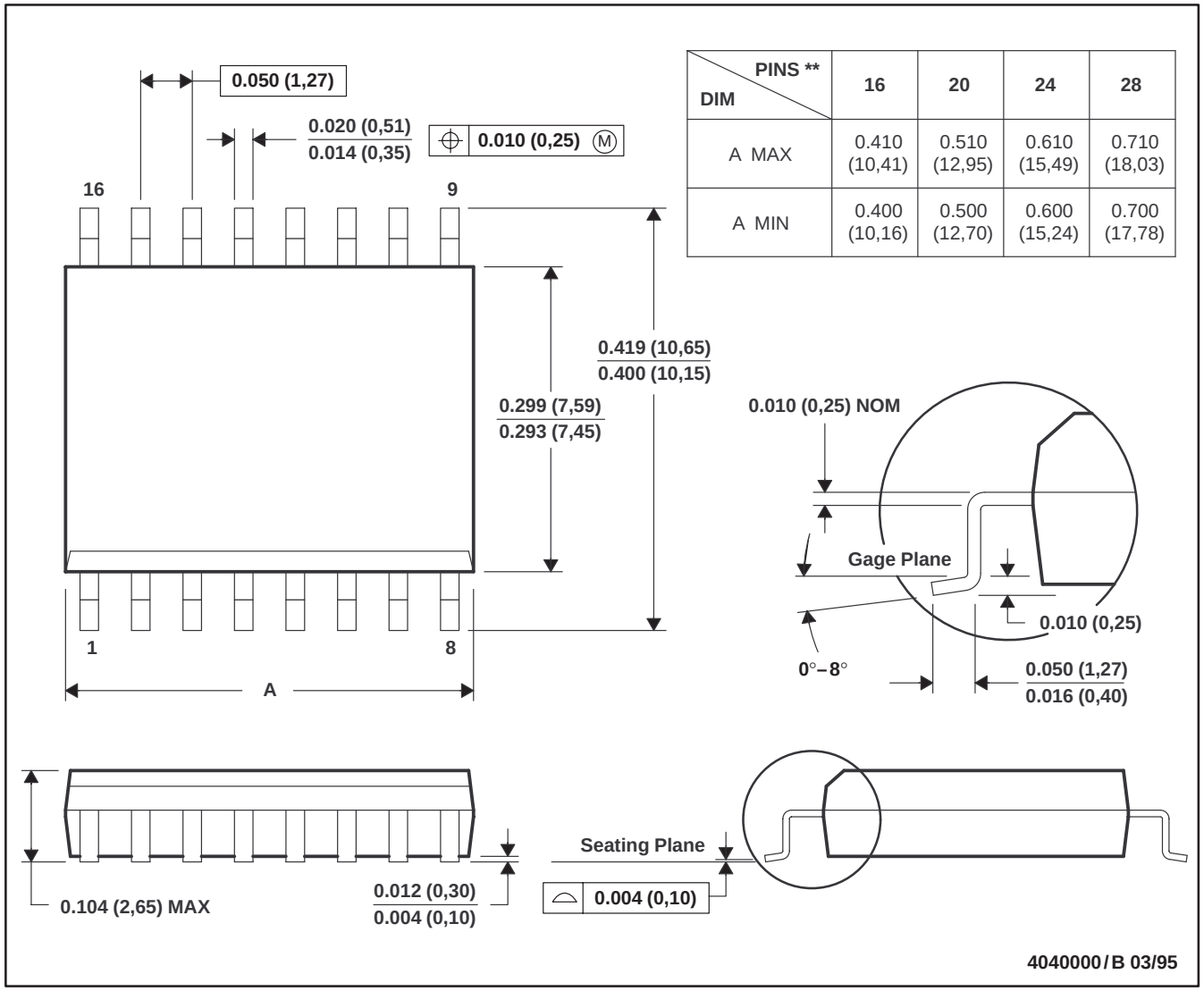
receiver characteristics

PARAMETER		TEST CONDITIONS	232/V.28		423/V.10		562		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$\|V_I\|$	Input voltage			25		10		25	V
V_{IT}	Input voltage threshold	$\|V_I\|$ < 15 V	–3	3	NA		–3	3	V
		$\|V_I\|$ < 10 V	NA		–0.2	0.2	NA		V
R_I	Input resistance	3 V < $\|V_I\|$ < 15 V	3	7	NA		3	7	kΩ
		$\|V_I\|$ < 10 V	NA		4		NA		kΩ

MECHANICAL INFORMATION

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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