

# MC14076B

## 4-Bit D-Type Register with Three-State Outputs

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master root is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 1.)

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}, V_{out}$	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient) per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package (Note 2.)	500	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$  From 65 $^{\circ}C$  To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

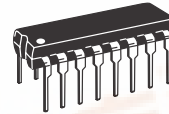
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



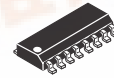
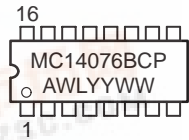
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### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

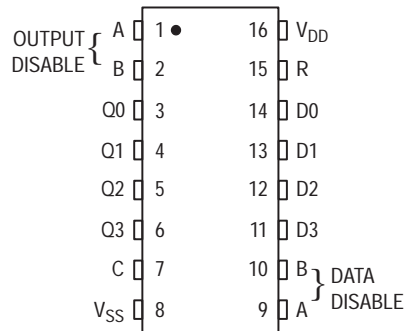
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Device	Package	Shipping
MC14076BCP	PDIP-16	2000/Box
MC14076BD	SOIC-16	2400/Box
MC14076BDR2	SOIC-16	2500/Tape & Reel

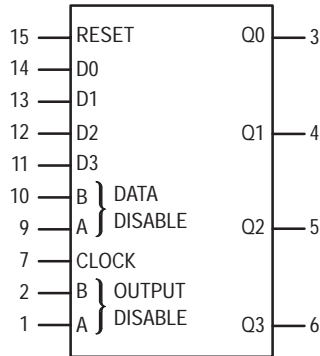


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## PIN ASSIGNMENT



## BLOCK DIAGRAM



$V_{DD}$  = PIN 16  
 $V_{SS}$  = PIN 8

## FUNCTION TABLE

Inputs					Output Q
Reset	Clock	Data Disable		Data D	
		A	B		
1	X	X	X	X	0
0	0	X	X	X	$Q_n$
0	$\nearrow$	1	X	X	$Q_n$
0	$\nearrow$	X	1	X	$Q_n$
0	$\nearrow$	0	0	0	0
0	$\nearrow$	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.  
 X = Don't Care.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0  $V_{in} = 0$ or $V_{DD}$	"0" Level  $V_{OL}$	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level  $V_{OH}$	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage $(V_O = 4.5$ or $0.5$ Vdc) $(V_O = 9.0$ or $1.0$ Vdc) $(V_O = 13.5$ or $1.5$ Vdc)  $(V_O = 0.5$ or $4.5$ Vdc) $(V_O = 1.0$ or $9.0$ Vdc) $(V_O = 1.5$ or $13.5$ Vdc)	"0" Level  $V_{IL}$	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level  $V_{IH}$	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current $(V_{OH} = 2.5$ Vdc) $(V_{OH} = 4.6$ Vdc) $(V_{OH} = 9.5$ Vdc) $(V_{OH} = 13.5$ Vdc)  $(V_{OL} = 0.4$ Vdc) $(V_{OL} = 0.5$ Vdc) $(V_{OL} = 1.5$ Vdc)	Source  $I_{OH}$	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink  $I_{OL}$	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	$I_{in}$	15	—	$\pm 0.1$	—	$\pm 0.00001$	$\pm 0.1$	—	$\pm 1.0$	$\mu$ Adc	
Input Capacitance $(V_{in} = 0)$	$C_{in}$	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	$I_{DD}$	5.0	—	5.0	—	0.005	5.0	—	150	$\mu$ Adc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current <sup>(4.)</sup> <sup>(5.)</sup> (Dynamic plus Quiescent, Per Package) $(C_L = 50$ pF on all outputs, all buffers switching)	$I_T$	5.0	$I_T = (0.75 \mu A/kHz) f + I_{DD}$							$\mu$ Adc	
		10	$I_T = (1.50 \mu A/kHz) f + I_{DD}$								
		15	$I_T = (2.25 \mu A/kHz) f + I_{DD}$								
Three-State Leakage Current	$I_{TL}$	15	—	$\pm 0.1$	—	$\pm 0.0001$	$\pm 0.1$	—	$\pm 3.0$	$\mu$ Adc	

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.002$ .

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### SWITCHING CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ <sup>(7.)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}$ , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}$ , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$  Reset to Q $t_{PLH}$ , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 92 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15  5.0 10 15	— — —  — — —	300 125 90  300 125 90	600 250 180  600 250 180	ns
3-State Propagation Delay, Output "1" or "0" to High Impedance	$t_{PHZ}$ , $t_{PLZ}$	5.0 10 15	— — —	150 60 45	300 120 90	ns
3-State Propagation Delay, High Impedance to "1" or "0" Level	$t_{PZH}$ , $t_{PZL}$	5.0 10 15	— — —	200 80 60	400 160 120	ns
Clock Pulse Width	$t_{WH}$	5.0 10 15	260 110 80	130 55 40	— — —	ns
Reset Pulse Width	$t_{WH}$	5.0 10 15	370 150 110	185 75 55	— — —	ns
Data Setup Time	$t_{su}$	5.0 10 15	30 10 4	15 5 2	— — —	ns
Data Hold Time	$t_h$	5.0 10 15	130 60 50	65 30 25	— — —	ns
Data Disable Setup Time	$t_{su}$	5.0 10 15	220 80 50	110 40 25	— — —	ns
Clock Pulse Rise and Fall Time	$t_{TLH}$ , $t_{THL}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	3.6 9.0 12	1.8 4.5 6.0	MHz

6. The formulas given are for the typical characteristics only at 25°C.

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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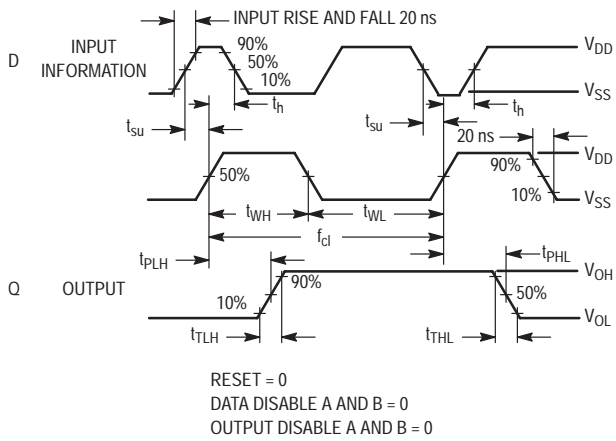


Figure 1. Timing Diagram

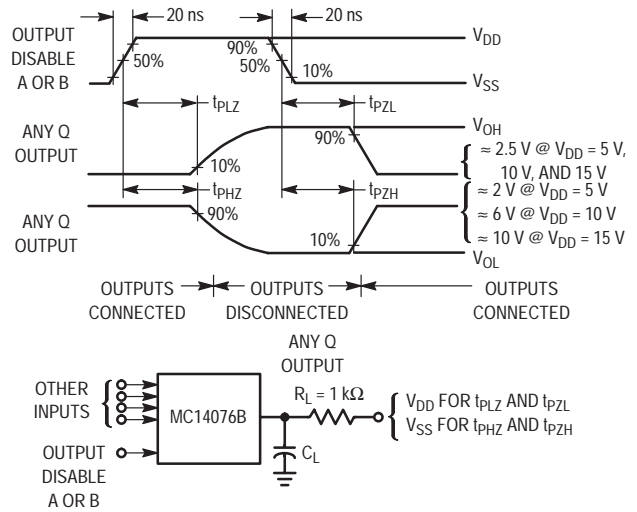
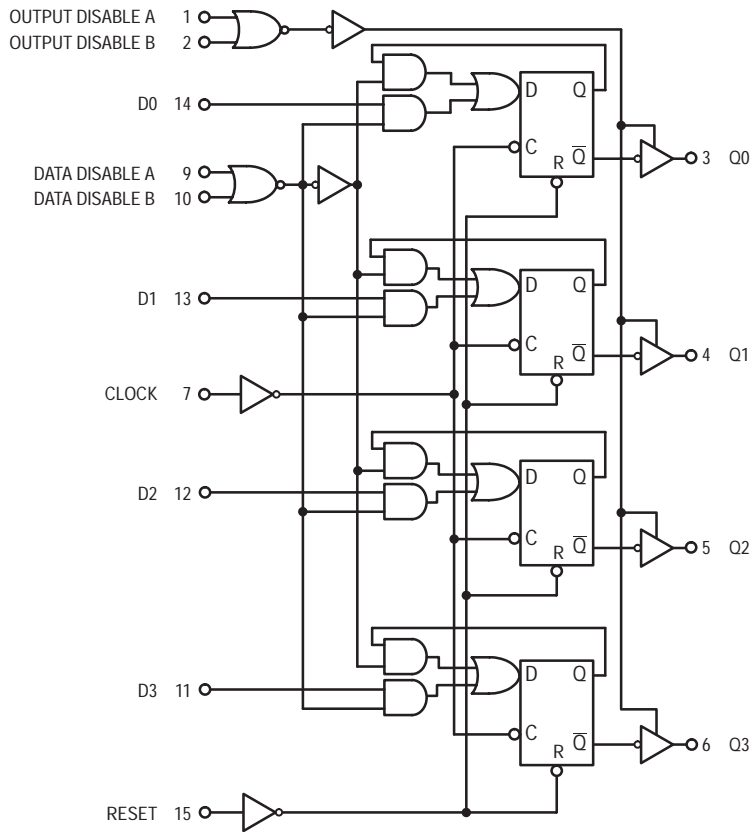


Figure 2. Three-State Propagation Delay Waveshape and Circuit

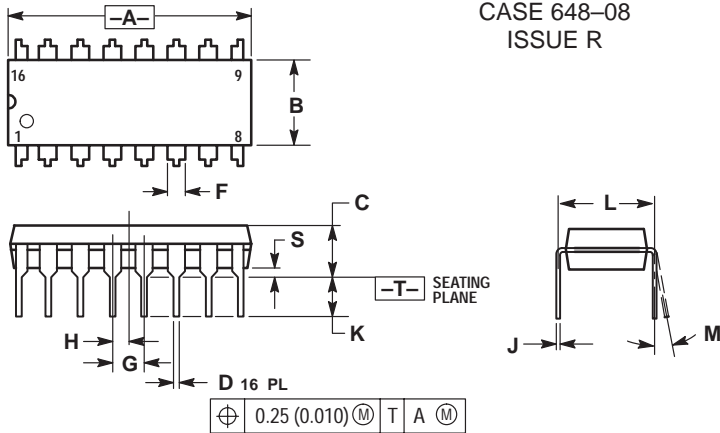
## EQUIVALENT FUNCTIONAL BLOCK DIAGRAM



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## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE R



NOTES:

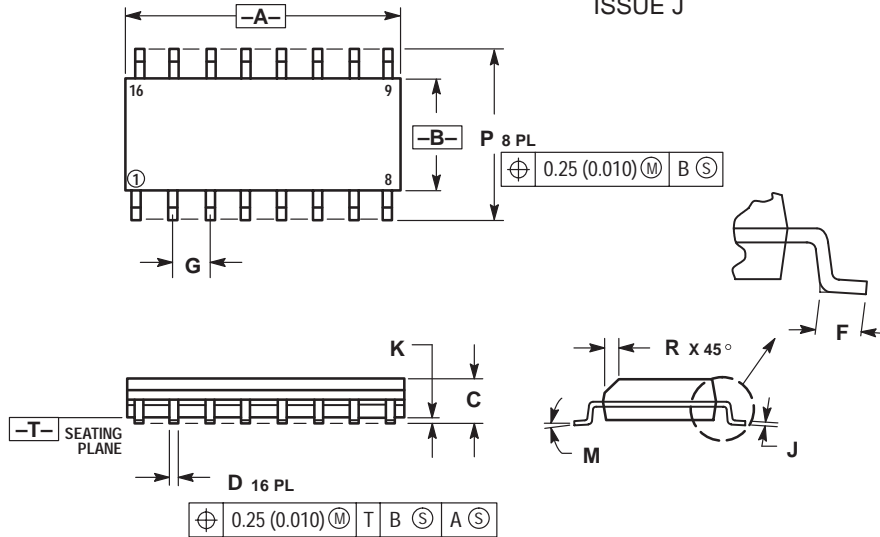
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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