LTC1591/LTC1597

14-Bit and 16-Bit Parallel Low Glitch Multiplying DACs with 4-Quadrant Resistors

FEATURES

- **True 16-Bit Performance Over Industrial Temperature Range**
- **DNL and INL: 1LSB Max**
- **On-Chip 4-Quadrant Resistors Allow Precise 0V to 10V, 0V to –10V or ±10V Outputs**
- **Pin Compatible 14- and 16-Bit Parts**
- Asynchronous Clear Pin
  - LTC1591/LTC1597: Reset to Zero Scale
  - LTC1591-1/LTC1597-1: Reset to Midscale
- **Glitch Impulse < 2nV-s**
- 28-Lead SSOP Package
- Low Power Consumption: 10μW Typ
- Power-On Reset

APPLICATIONS

- Process Control and Industrial Automation
- Direct Digital Waveform Generation
- Software-Controlled Gain Adjustment
- Automatic Test Equipment

DESCRIPTION

The LTC®1591/LTC1597 are pin compatible, parallel input 14-bit and 16-bit multiplying current output DACs that operate from a single 5V supply. INL and DNL are accurate to 1LSB over the industrial temperature range in both 2- and 4-quadrant multiplying modes. True 16-bit 4-quadrant multiplication is achieved with on-chip 4-quadrant multiplication resistors.

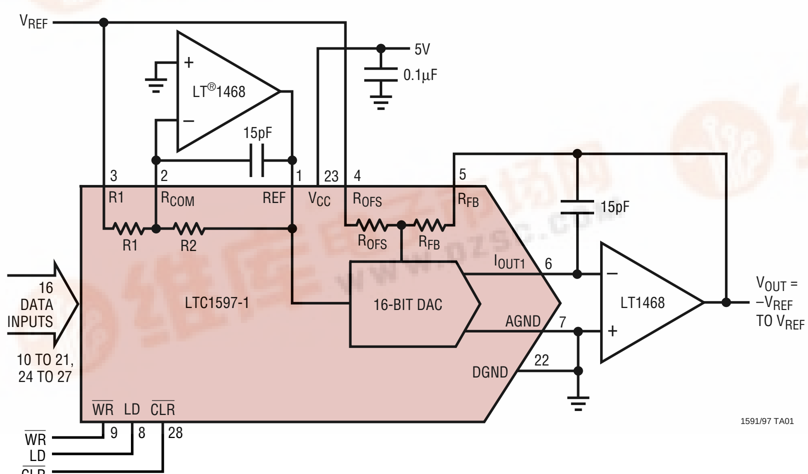
These DACs include an internal deglitcher circuit that reduces the glitch impulse to less than 2nV-s (typ). The asynchronous $\overline{\text{CLR}}$ pin resets the LTC1591/LTC1597 to zero scale and LTC1591-1/LTC1597-1 to midscale.

The LTC1591/LTC1597 are available in 28-pin SSOP and PDIP packages and are specified over the industrial temperature range.

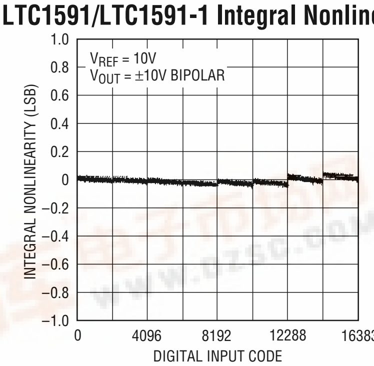
For serial interface 16-bit current output DACs refer to the LTC1595/LTC1596 data sheet.

TYPICAL APPLICATION

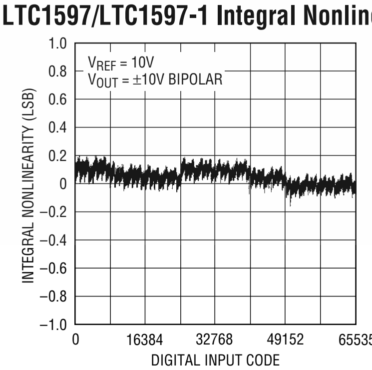
16-Bit, 4-Quadrant Multiplying DAC with a Minimum of External Components



LTC1591/LTC1591-1 Integral Nonlinearity



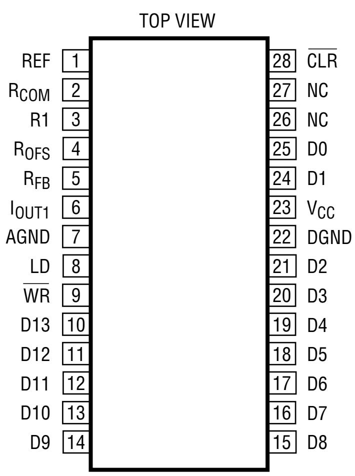
LTC1597/LTC1597-1 Integral Nonlinearity



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to AGND .... –0.5V to 7V
V_{CC} to DGND .... –0.5V to 7V
AGND to DGND .... V_{CC} + 0.5V
DGND to AGND .... V_{CC} + 0.5V
REF, R_{OFS}, R_{FB}, R1, R_{COM} to AGND, DGND .... ±25V
Digital Inputs to DGND .... –0.5V to (V_{CC} + 0.5V)
I_{OUT1} to AGND .... –0.5V to(V_{CC} + 0.5V)
Maximum Junction Temperature .... 125°C
Operating Temperature Range
LTC1591C/LTC1591-1C
LTC1597C/LTC1597-1C .... 0°C to 70°C
LTC1591I/LTC1591-1I
LTC1597I/LTC1597-1I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

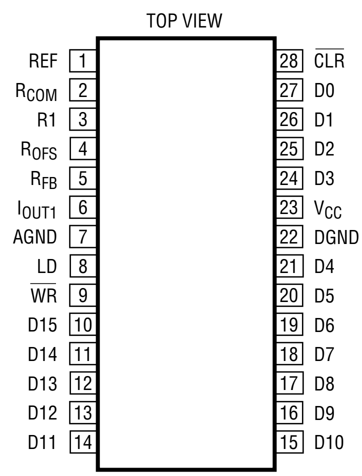
PACKAGE/ORDER INFORMATION



G PACKAGE 28-LEAD PLASTIC SSOP
N PACKAGE 28-LEAD NARROW PDIP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)

ORDER PART NUMBER

LTC1591CG
LTC1591CN
LTC1591IG
LTC1591IN
LTC1591-1CG
LTC1591-1CN
LTC1591-1IG
LTC1591-1IN



G PACKAGE 28-LEAD PLASTIC SSOP
N PACKAGE 28-LEAD NARROW PDIP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)

ORDER PART NUMBER

LTC1597ACG
LTC1597ACN
LTC1597BCG
LTC1597BCN
LTC1597-1ACG
LTC1597-1ACN
LTC1597-1BCG
LTC1597-1BCN
LTC1597AIG
LTC1597AIN
LTC1597BIG
LTC1597BIN
LTC1597-1AIG
LTC1597-1AIN
LTC1597-1BIG
LTC1597-1BIN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1591/-1 MIN	LTC1591/-1 TYP	LTC1591/-1 MAX	LTC1597B/-1B MIN	LTC1597B/-1B TYP	LTC1597B/-1B MAX	LTC1597A/-1A MIN	LTC1597A/-1A TYP	LTC1597A/-1A MAX	UNITS
Accuracy													
	Resolution		●	14			16			16			Bits
	Monotonicity		●	14			16			16			Bits
INL	Integral Nonlinearity	(Note 2) T_A = 25°C				±1			±2		±0.25	±1	LSB
		T_{MIN} to T_{MAX}	●			±1			±2		±0.35	±1	LSB
DNL	Differential Nonlinearity	T_A = 25°C				±1			±1		±0.2	±1	LSB
		T_{MIN} to T_{MAX}	●			±1			±1		±0.2	±1	LSB
GE	Gain Error	Unipolar Mode											
		(Note 3) T_A = 25°C				±4			±16		2	±16	LSB
		T_{MIN} to T_{MAX}	●			±6			±24		3	±16	LSB
		Bipolar Mode											
		(Note 3) T_A = 25°C				±4			±16		2	±16	LSB
		T_{MIN} to T_{MAX}	●			±6			±24		3	±16	LSB
	Gain Temperature Coefficient	(Note 4) ΔGain/ΔTemperature	●		1	2		1	2		1	2	ppm/°C
	Bipolar Zero-Scale Error	T_A = 25°C				±3			±10			±5	LSB
		T_{MIN} to T_{MAX}	●			±5			±16			±8	LSB
I_{LKG}	OUT1 Leakage Current	(Note 5) T_A = 25°C				±5			±5			±5	nA
		T_{MIN} to T_{MAX}	●			±15			±15			±15	nA
PSRR	Power Supply Rejection Ratio	V_{CC} = 5V ±10	●		±0.1	±1		±0.4	±2		±0.4	±2	LSB/V

V_{CC} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R_{REF}	DAC Input Resistance (Unipolar)	(Note 6)	●	4.5	6	10	kΩ
R1/R2	R1/R2 Resistance (Bipolar)	(Notes 6, 13)	●	9	12	20	kΩ
R_{OFS}, R_{FB}	Feedback and Offset Resistances	(Note 6)	●	9	12	20	kΩ
AC Performance (Note 4)							
	Output Current Settling Time	(Notes 7, 8)			1		µs
	Midscale Glitch Impulse	(Note 12)			2		nV-s
	Digital-to-Analog Glitch Impulse	(Note 9)			1		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 10)			108		dB
	Output Noise Voltage Density	(Note 11)			10		$nV/\sqrt{Hz}$
	Harmonic Distortion (Digital Waveform Generation)	Unipolar Mode (Note 14)					
		2nd Harmonic			94		dB
		3rd Harmonic			101		dB
		SFDR			94		dB
		Bipolar Mode (Note 14)					
		2nd Harmonic			94		dB
		3rd Harmonic			101		dB
		SFDR			94		dB

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, V_{REF} = 10V, I_{OUT1} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Outputs (Note 4)							
C_{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s: C_{OUT1} DAC Register Loaded to All 0s: C_{OUT1}	● ●		115 70	130 80	pF pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 4) V_{IN} = 0V	●			8	pF
Timing Characteristics							
t_{DS}	Data to $\overline{WR}$ Setup Time		●	60	20		ns
t_{DH}	Data to $\overline{WR}$ Hold Time		●	0	–12		ns
t_{WR}	$\overline{WR}$ Pulse Width		●	60	25		ns
t_{LD}	LD Pulse Width		●	110	55		ns
t_{CLR}	Clear Pulse Width		●	60	40		ns
t_{LWD}	$\overline{WR}$ to LD Delay Time		●	0			ns
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{CC}	●			10	µA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Absolute Maximum Values are those beyond which the life of a device may be impaired.

Note 2: ±1LSB = ±0.006% of full scale = ±61ppm of full scale for the LTC1591/LTC1591-1. ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale for the LTC1597/LTC1597-1.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: $I_{(OUT1)}$ with DAC register loaded to all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: I_{OUT1} load = 100Ω in parallel with 13pF.

Note 8: To 0.006% for a full-scale change, measured from the rising edge of LD for the LTC1591/LTC1591-1. To 0.0015% for a full-scale change, measured from the rising edge of LD for the LTC1597/LTC1597-1.

Note 9: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 10: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 11: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K), R = resistance (Ω), T = temperature (°K), B = bandwidth (Hz).

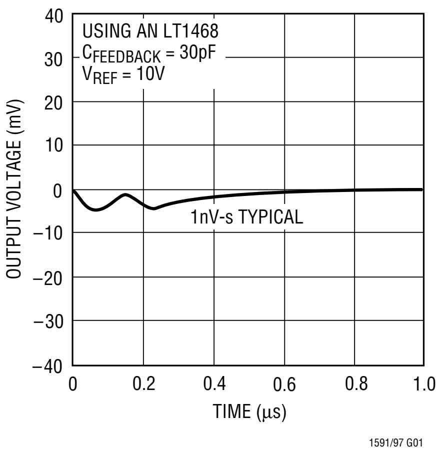
Note 12: Midscale transition code: 01 1111 1111 1111 to 10 0000 0000 0000 for the LTC1591/LTC1591-1 and 0111 1111 1111 1111 to 1000 0000 0000 0000 for the LTC1597/LTC1597-1.

Note 13: R1 and R2 are measured between R1 and R_{COM}, REF and R_{COM}.

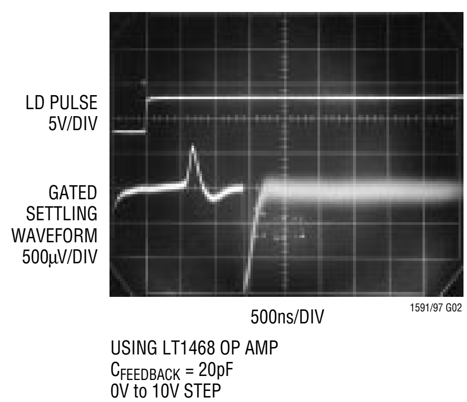
Note 14: Measured using the LT1468 op amp in unipolar mode for I/V converter and LT1468 I/V and LT1001 reference inverter in bipolar mode. Sample Rate = 50kHz, Signal Frequency = 1kHz, V_{REF} = 5V, T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591/LTC1597)

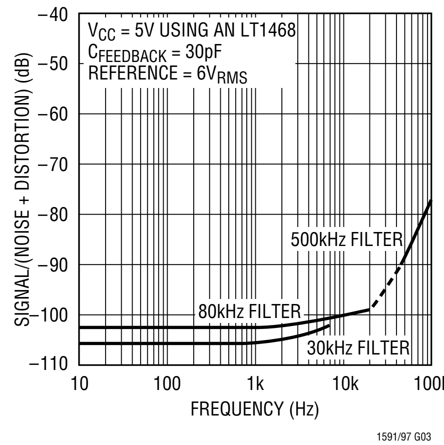
Midscale Glitch Impulse



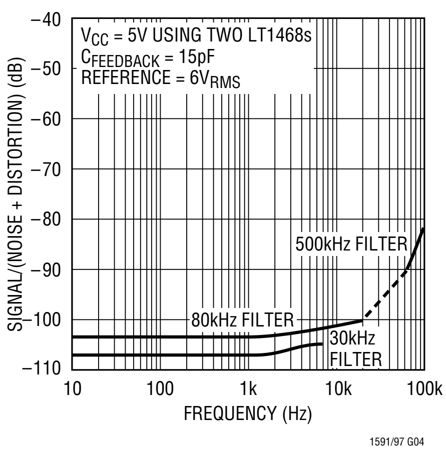
Full-Scale Settling Waveform



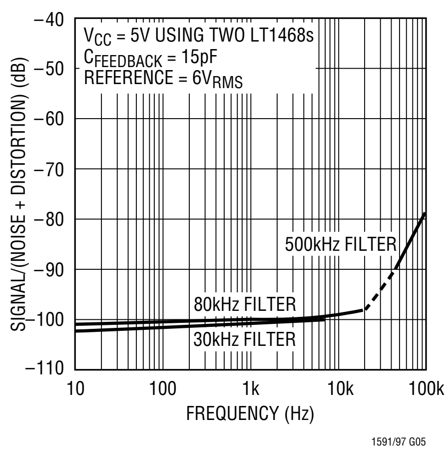
Unipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency



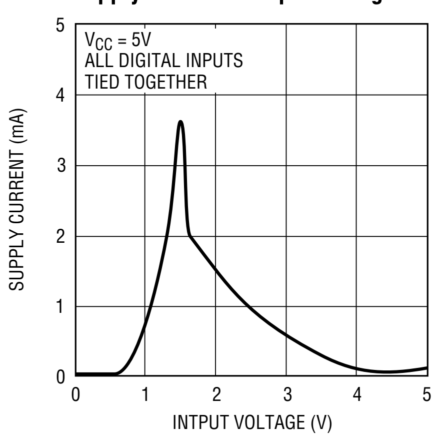
Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Zeros



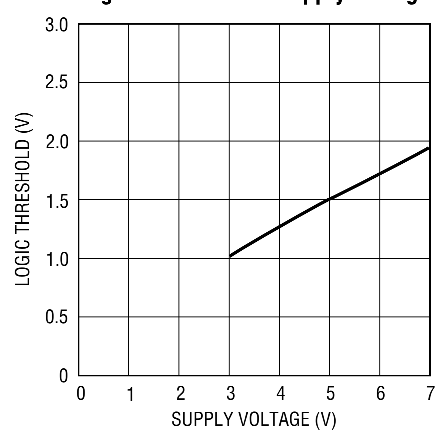
Bipolar Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency, Code = All Ones



Supply Current vs Input Voltage

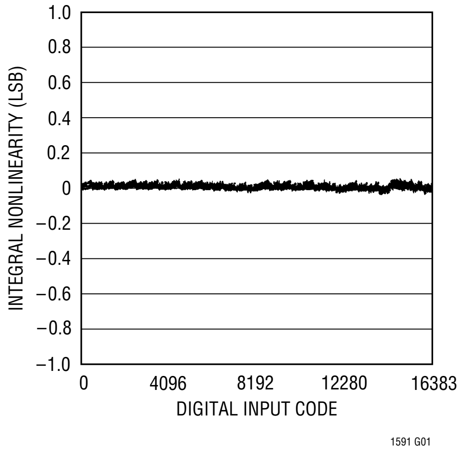


Logic Threshold vs Supply Voltage

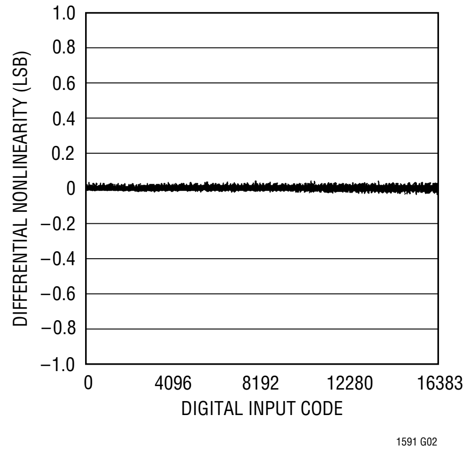


TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)

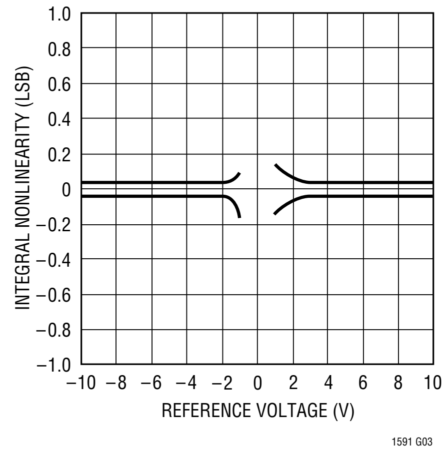
Integral Nonlinearity (INL)



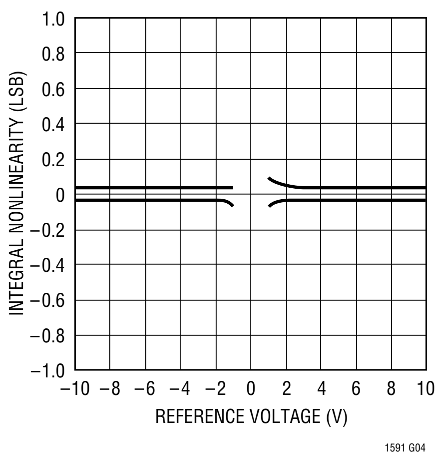
Differential Nonlinearity (DNL)



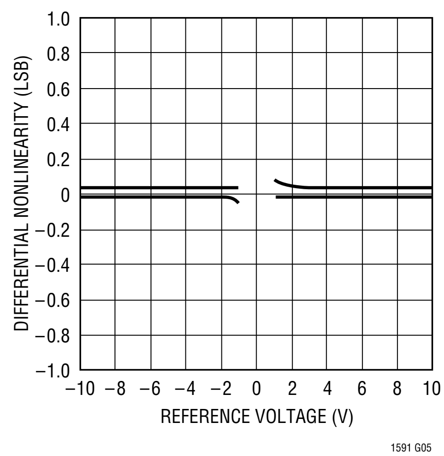
Integral Nonlinearity vs Reference Voltage in Unipolar Mode



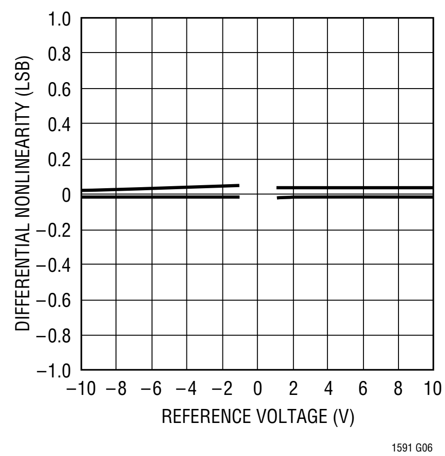
Integral Nonlinearity vs Reference Voltage in Bipolar Mode



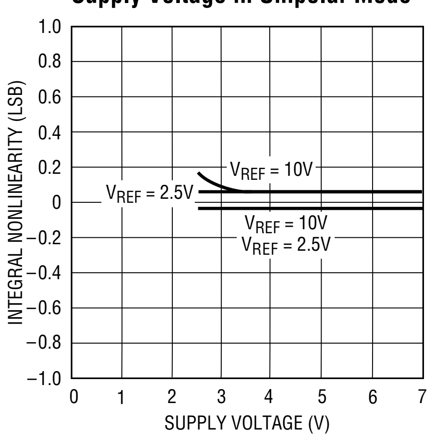
Differential Nonlinearity vs Reference Voltage in Unipolar Mode



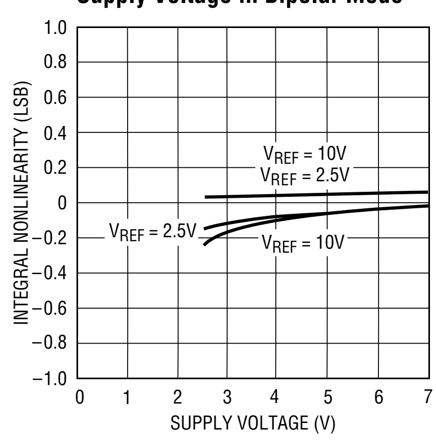
Differential Nonlinearity vs Reference Voltage in Bipolar Mode



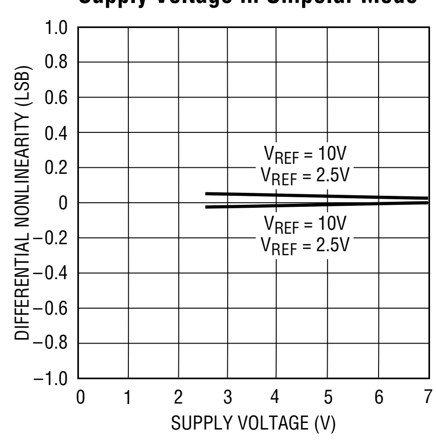
Integral Nonlinearity vs Supply Voltage in Unipolar Mode



Integral Nonlinearity vs Supply Voltage in Bipolar Mode

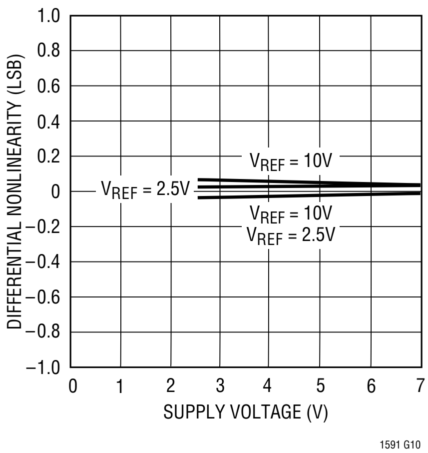


Differential Nonlinearity vs Supply Voltage in Unipolar Mode

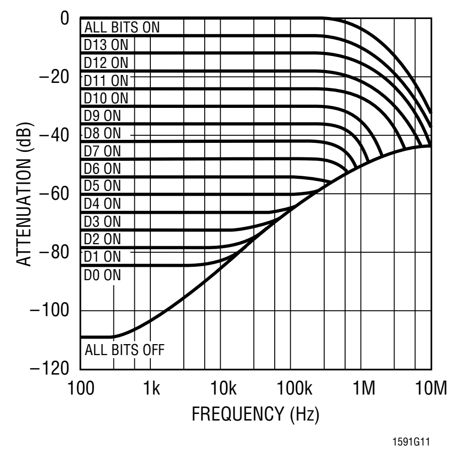


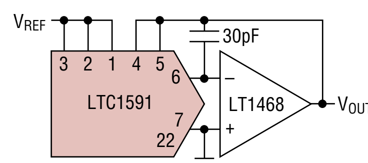
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)

Differential Nonlinearity vs Supply Voltage in Bipolar Mode

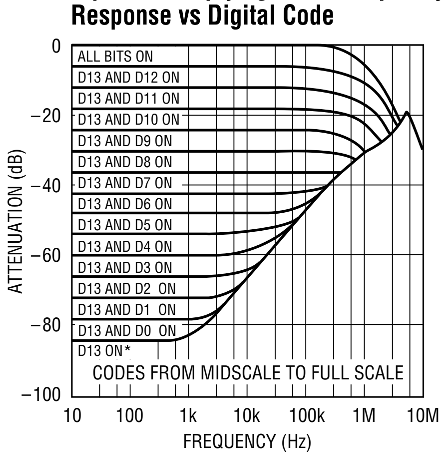


Unipolar Multiplying Mode Frequency Response vs Digital Code

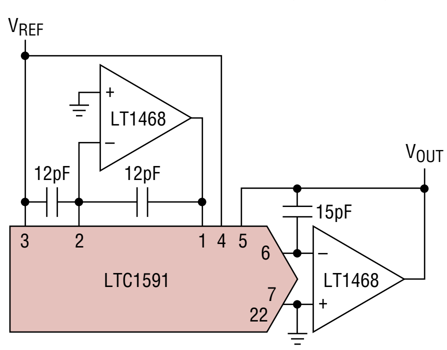




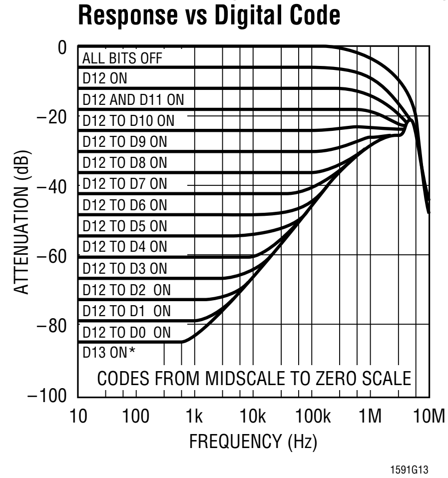
Bipolar Multiplying Mode Frequency Response vs Digital Code



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO −84dB TYPICAL (−70dB MAX)



Bipolar Multiplying Mode Frequency Response vs Digital Code



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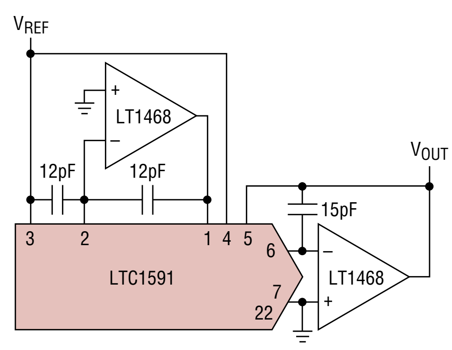
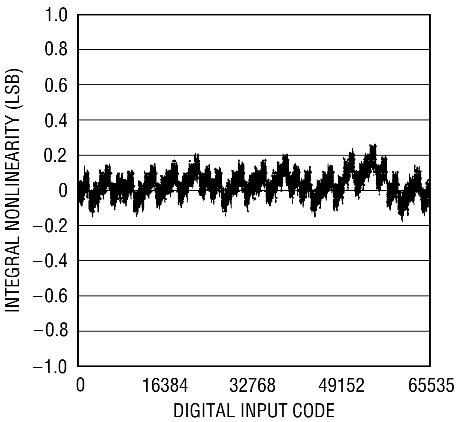


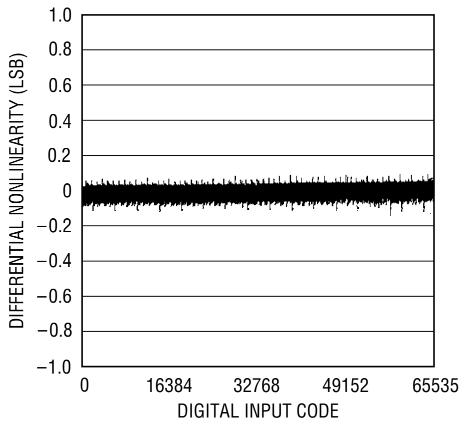
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)

Integral Nonlinearity (INL)



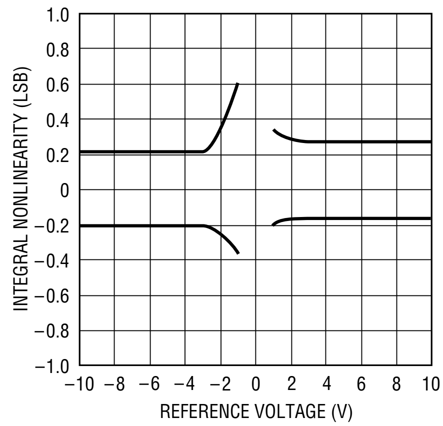
1597 G01

Differential Nonlinearity (DNL)



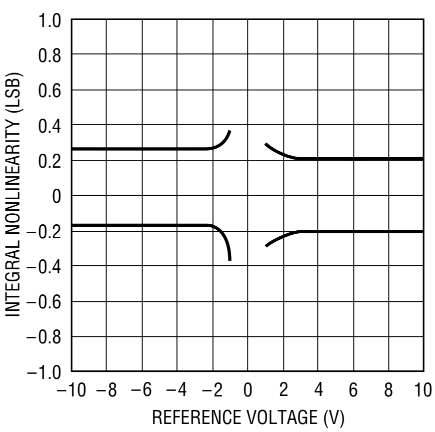
1597 G02

Integral Nonlinearity vs Reference Voltage in Unipolar Mode



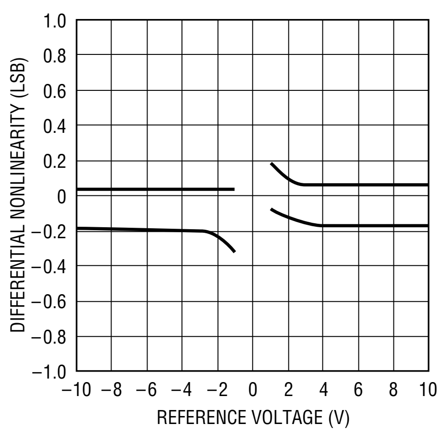
1597 G03

Integral Nonlinearity vs Reference Voltage in Bipolar Mode



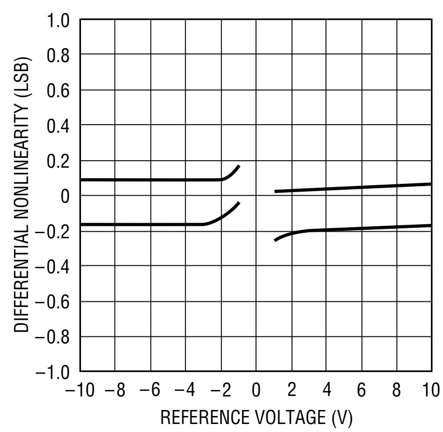
1597 G04

Differential Nonlinearity vs Reference Voltage in Unipolar Mode



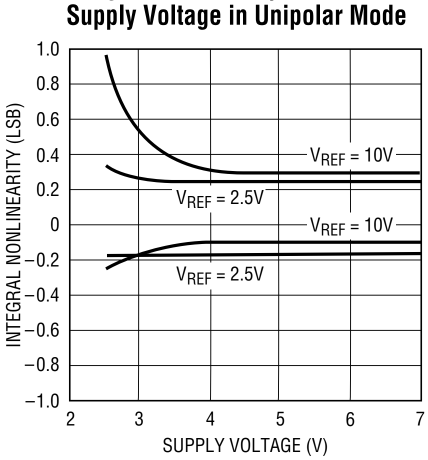
1597 G05

Differential Nonlinearity vs Reference Voltage in Bipolar Mode



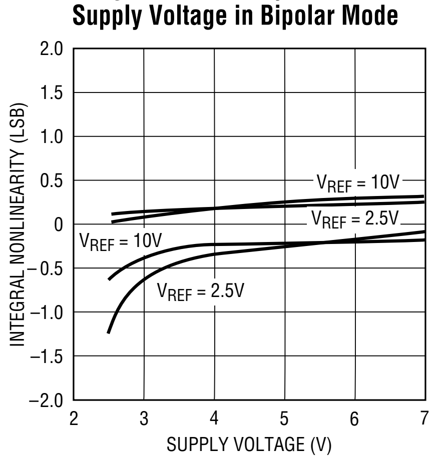
1597 G06

Integral Nonlinearity vs Supply Voltage in Unipolar Mode



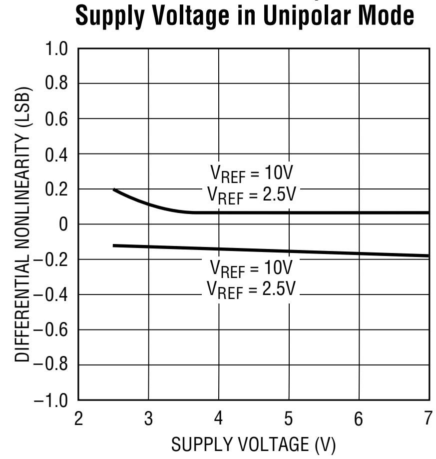
1597 G07

Integral Nonlinearity vs Supply Voltage in Bipolar Mode



1597 G08

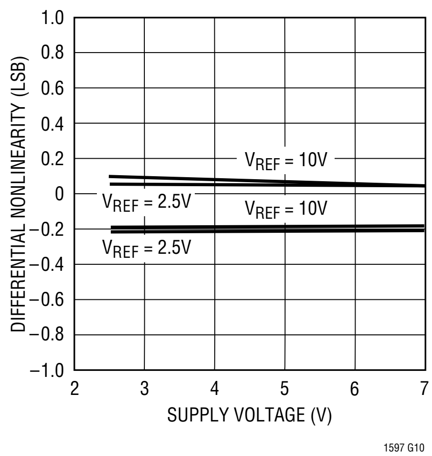
Differential Nonlinearity vs Supply Voltage in Unipolar Mode



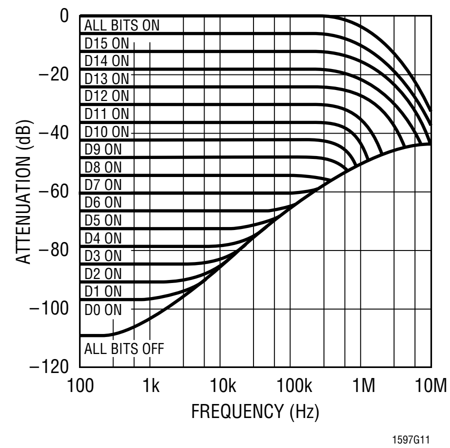
1597 G09

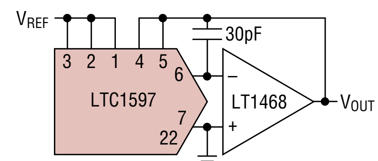
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)

Differential Nonlinearity vs Supply Voltage in Bipolar Mode

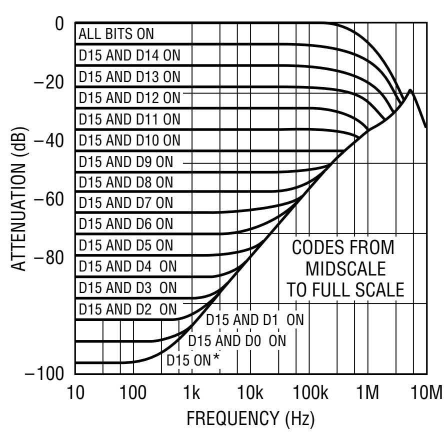


Unipolar Multiplying Mode Frequency Response vs Digital Code

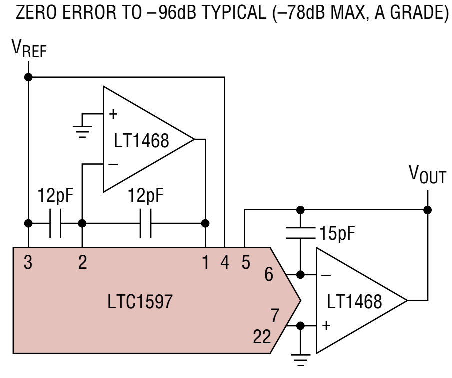




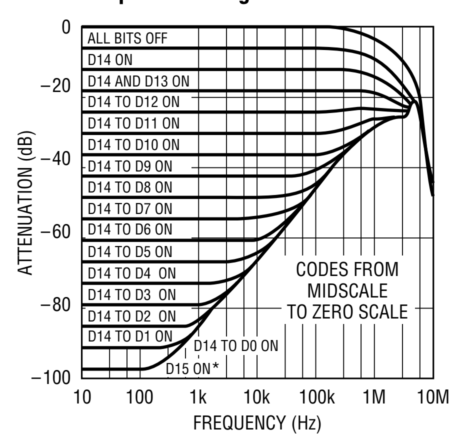
Bipolar Multiplying Mode Frequency Response vs Digital Code



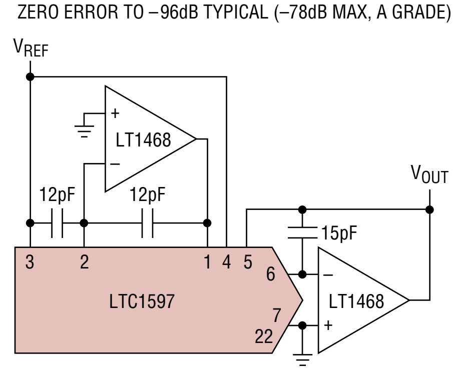
*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO –96dB TYPICAL (–78dB MAX, A GRADE)



Bipolar Multiplying Mode Frequency Response vs Digital Code



*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO –96dB TYPICAL (–78dB MAX, A GRADE)



PIN FUNCTIONS

LTC1591

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically ±10V, accepts up to ±25V. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (Pin 2): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1a and 2a.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFS} (Pin 4).

R_{OFS} (Pin 4): Bipolar Offset Resistor. Typically swings ±10V, accepts up to ±25V. In 2-quadrant operation tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{REF}$. V_{REF} is typically ±10V.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

$\overline{WR}$ (Pin 9): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the digital input pins into the 14-bit wide input register.

DB13 to D2 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (Pin 23): The Positive Supply Input. $4.5V \le V_{CC} \ge 5.5V$. Requires a bypass capacitor to ground.

DB1, DB0 (Pins 24, 25): Digital Input Data Bits.

NC (Pins 26, 27): No Connect.

$\overline{CLR}$ (Pin 28): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1591 and midscale code for the LTC1591-1.

LTC1597

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically ±10V, accepts up to ±25V. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (Pin 2): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1b and 2b.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFS} (Pin 4).

R_{OFS} (Pin 4): Bipolar Offset Resistor. Typically swings ±10V, accepts up to ±25V. In 2-quadrant operation tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{REF}$. V_{REF} is typically ±10V.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

$\overline{WR}$ (Pin 9): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the digital input pins into the 16-bit wide input register.

DB15 to D4 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (Pin 23): The Positive Supply Input. $4.5V \le V_{CC} \ge 5.5V$. Requires a bypass capacitor to ground.

DB3 to DB0 (Pins 24 to 27): Digital Input Data Bits.

$\overline{CLR}$ (Pin 28): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1597 and midscale code for the LTC1597-1.

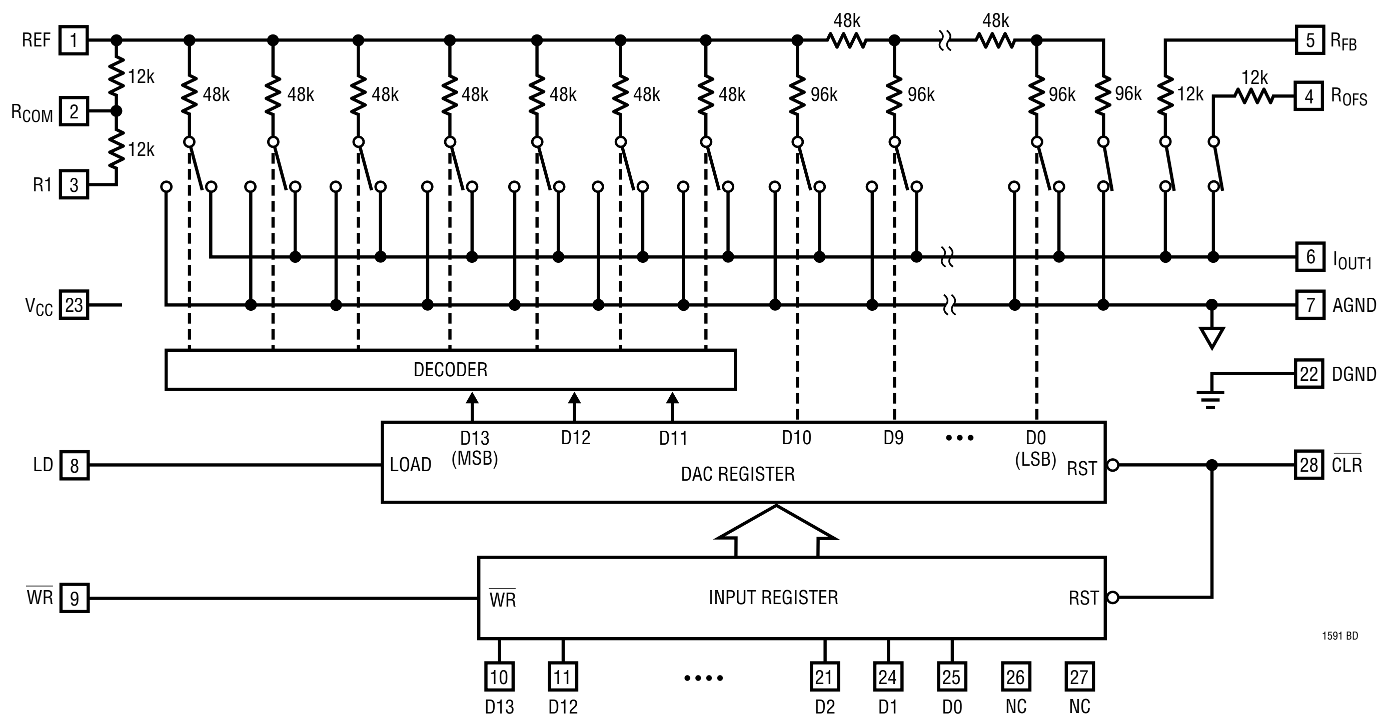
TRUTH TABLE

Table 1

CONTROL INPUTS $\overline{CLR}$	$\overline{WR}$	LD	REGISTER OPERATION
0	X	X	Reset Input and DAC Register to All 0s for LTC1591/LTC1597 and Midscale for LTC1591-1/LTC1597-1 (Asynchronous Operation)
1	0	0	Load Input Register with All 14/16 Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1	0	1	Input and DAC Register Are Transparent
1	‾|_|‾	‾|_|‾	CLK = LD and $\overline{WR}$ Tied Together. The 14/16 Data Bits Are Loaded into the Input Register on the Falling Edge of the CLK and Then Loaded into the DAC Register on the Rising Edge of the CLK
1	1	0	No Register Operation

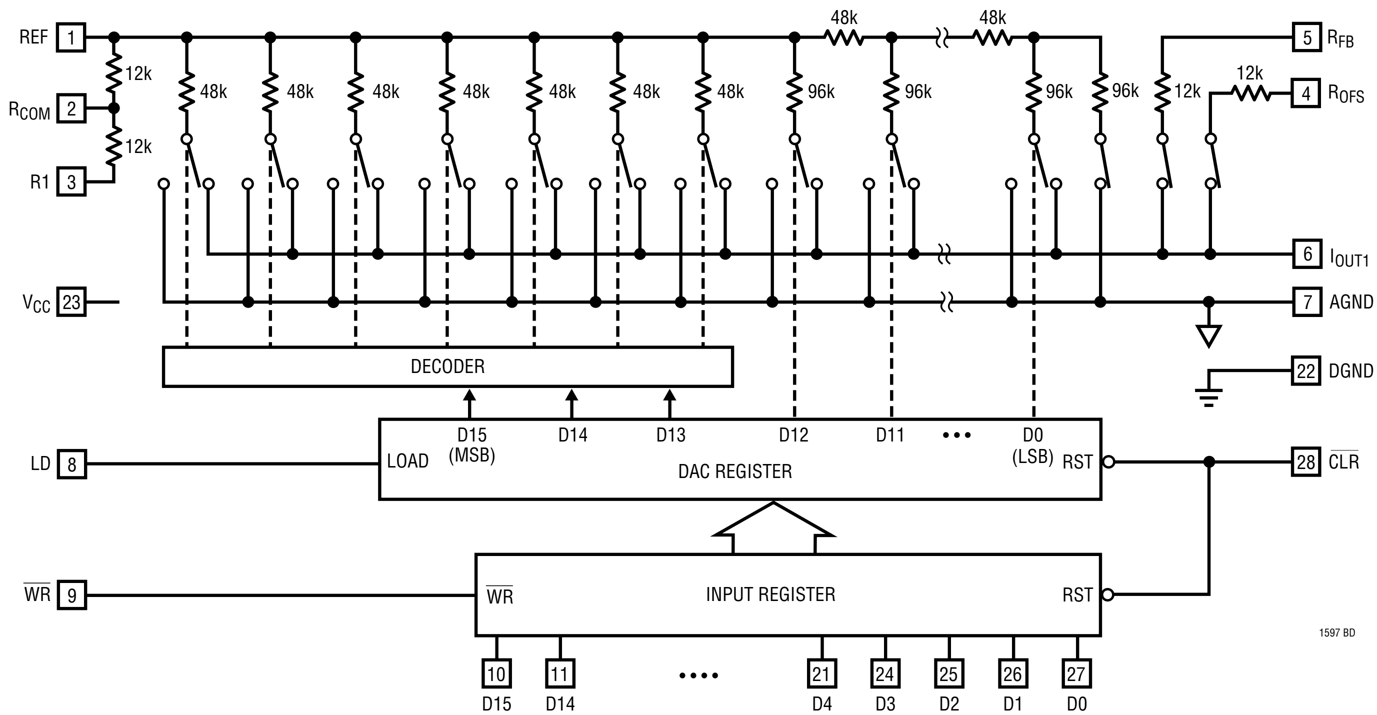
BLOCK DIAGRAMS

LTC1591

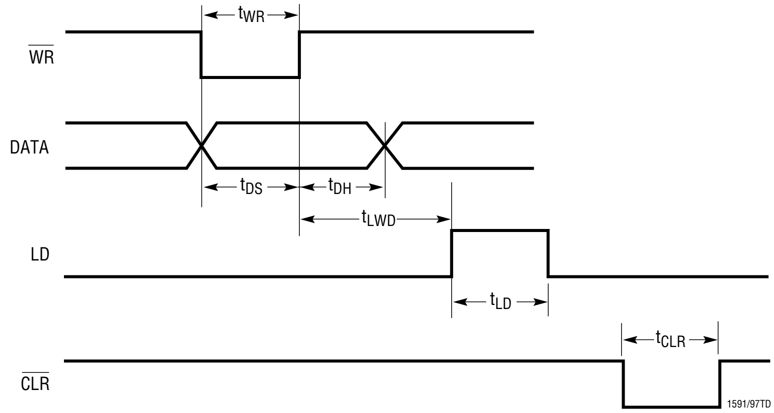


BLOCK DIAGRAMS

LTC1597



TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1591/LTC1597 are 14-/16-bit multiplying, current output DACs with a full parallel 14-/16-bit digital interface. The devices operate from a single 5V supply and provide both unipolar 0V to –10V or 0V to 10V and bipolar ±10V output ranges from a 10V or –10V reference input. They have three additional precision resistors on chip for bipolar operation. Refer to the block diagrams regarding the following description.

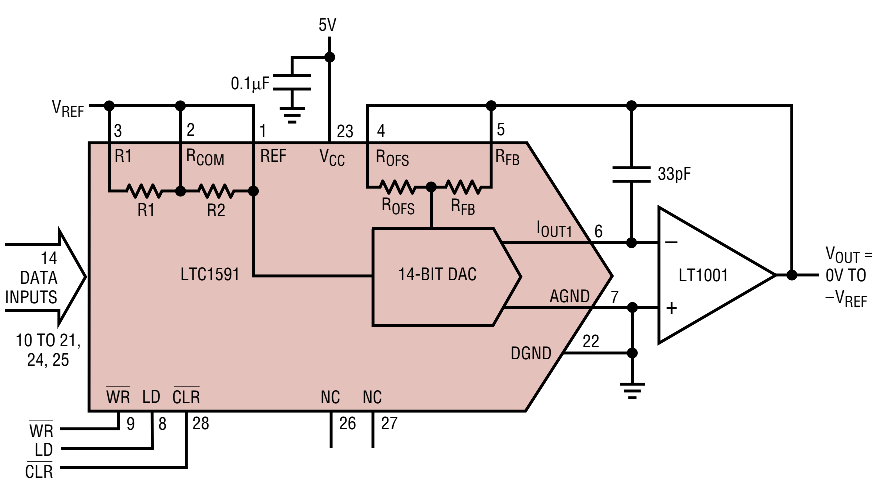
The 14-/16-bit DACs consist of a precision R-2R ladder for the 11/13LSBs. The 3MSBs are decoded into seven segments of resistor value R. Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FB} and 4-quadrant resistor R_{OFS} have a value of R/4. 4-quadrant resistors R1 and R2 have a magnitude of R/4. R1 and R2 together with an external op amp (see Figure 2) inverts the reference input voltage and applies it to the 14-/16-bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of R/8 in unipolar mode and R/12 in bipolar mode. The output impedance of the current output pin I_{OUT1} varies with DAC input code. The I_{OUT1} capacitance due to the NMOS current steering switches also varies with input code from 70pF to 115pF. An added feature of these devices, especially for waveform generation, is a proprietary deglitcher that reduces glitch energy to below 2nV-s over the DAC output voltage range.

Digital Section

The LTC1591/LTC1597 are 14-/16-bit wide full parallel data bus inputs. The devices are double-buffered with two 14-/16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from a 16-bit microprocessor bus when the $\overline{WR}$ pin is brought to a logic low level. The second register (DAC register) is updated with the data from the input register when the LD pin is brought to a logic high level. Updating the DAC register updates the DAC output with the new data. To make both registers transparent for flowthrough mode, tie $\overline{WR}$ low and LD high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the LD pin. The versatility of the interface also allows the use of the input and DAC registers in a master slave or edge-triggered configuration. This mode of operation occurs when $\overline{WR}$ and LD are tied together. The asynchronous clear pin resets the LTC1591/LTC1597 to zero scale and the LTC1591-1/LTC1597-1 to midscale. $\overline{CLR}$ resets both the input and DAC registers. These devices also have a power-on reset. Table 1 shows the truth table for the LTC1591/LT1597.

Unipolar Mode
(2-Quadrant Multiplying, V_{OUT} = 0V to $–V_{REF}$)

The LTC1591/LTC1597 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuits shown give a precision unipolar 0V to 10V output swing.



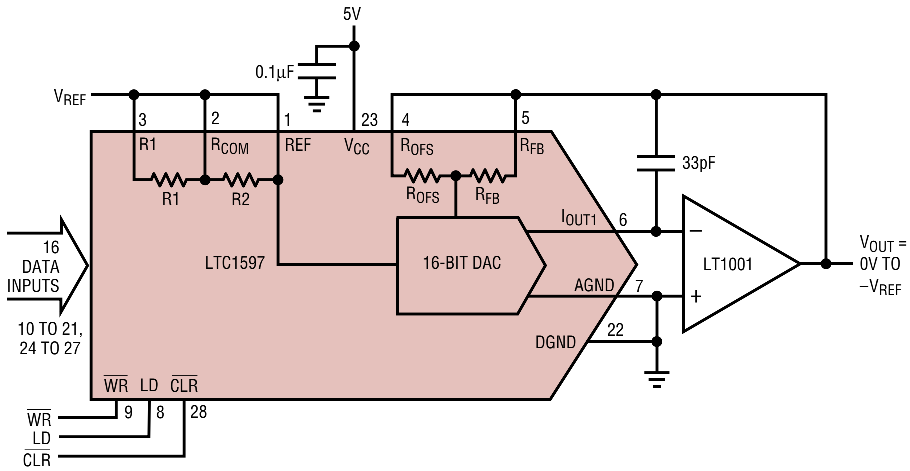
Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER (MSB … LSB)	ANALOG OUTPUT V_{OUT}
1111 1111 1111 11	$–V_{REF}$ (16,383/16,384)
1000 0000 0000 00	$–V_{REF}$ (8,192/16,384) = $–V_{REF}/2$
0000 0000 0000 01	$–V_{REF}$ (1/16,384)
0000 0000 0000 00	0V

1591/97 F01a

Figure 1a. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $–V_{REF}$

APPLICATIONS INFORMATION



Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	$-V_{REF}$ (65,535/65,536)
1000 0000 0000 0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000 0000 0000 0001	$-V_{REF}$ (1/65,536)
0000 0000 0000 0000	0V

1591/97 F01b

Figure 1b. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$

Bipolar Mode (4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1591/LTC1597 contain on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components, a capacitor and a dual op amp, as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar –10V to 10V output swing.

Op Amp Selection

Because of the extremely high accuracy of the 14-/16-bit LTC1591/LTC1597, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For the LTC1597, a 500µV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For the LTC1597, the same 500µV op amp offset (2mV offset for LTC1591) will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

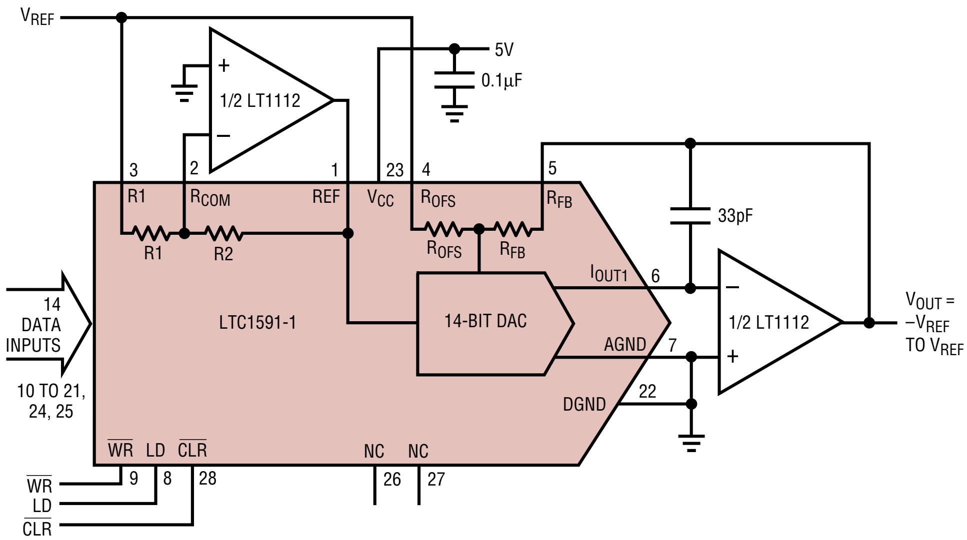
Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}/R_{OFS}) = I_{BIAS}(6k)$. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74, "*Component and Measurement Advances Ensure 16-Bit DAC Settling Time.*"

Reference Input and Grounding

For optimum performance the reference input of the LTC1597 should be driven by a source impedance of less than 1kΩ. However, these DACs have been designed to minimize source impedance effects. An 8kΩ source impedance degrades both INL and DNL by 0.2LSB.

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. AGND must be tied to the star ground with as low a resistance as possible.

APPLICATIONS INFORMATION

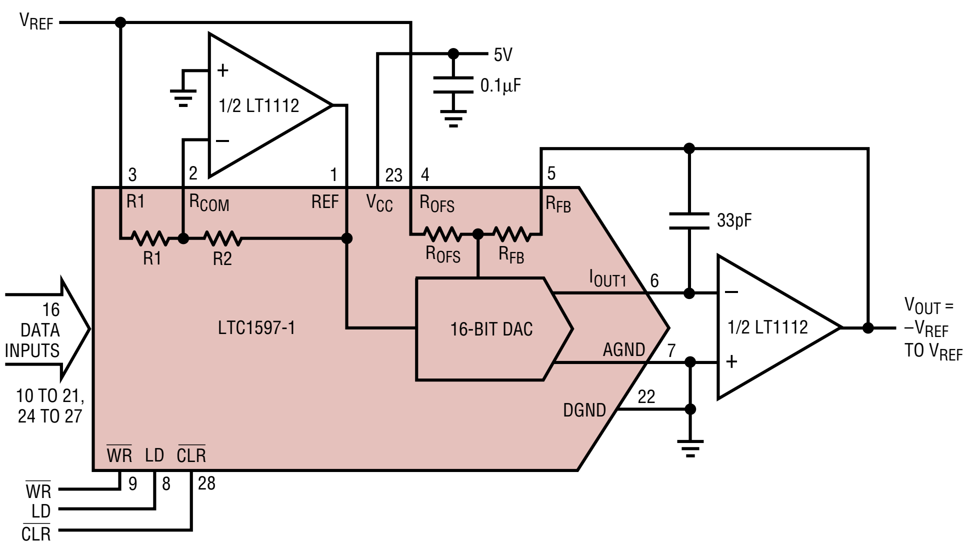


Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER (MSB … LSB)	ANALOG OUTPUT V_{OUT}
1111 1111 1111 11	V_{REF} (8,191/8,192)
1000 0000 0000 01	V_{REF} (1/8,192)
1000 0000 0000 00	0V
0111 1111 1111 11	$-V_{REF}$ (1/8,192)
0000 0000 0000 00	$-V_{REF}$

1591/97 F02a

Figure 2a. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}



Bipolar Offset Binary Code Table

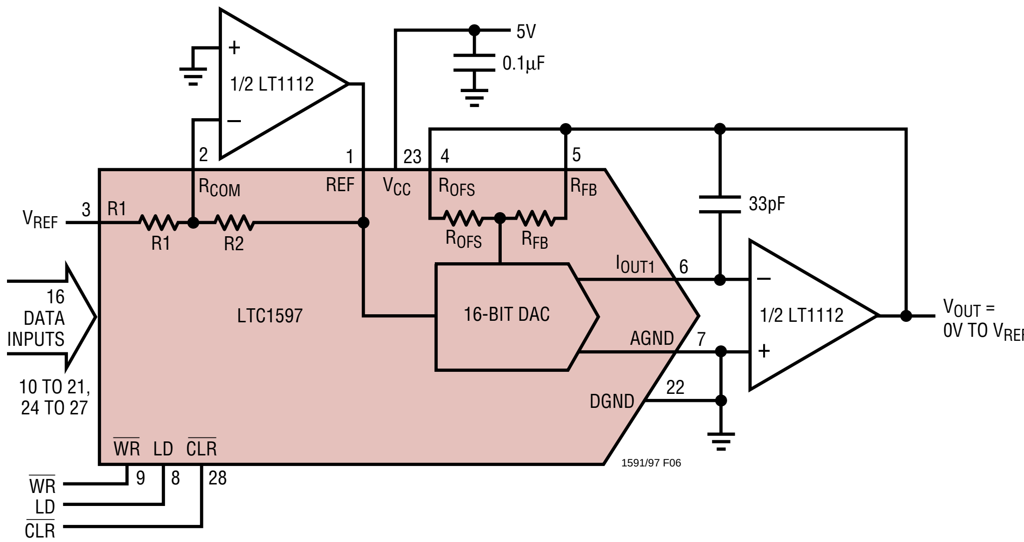
DIGITAL INPUT BINARY NUMBER IN DAC REGISTER (MSB … LSB)	ANALOG OUTPUT V_{OUT}
1111 1111 1111 1111	V_{REF} (32,767/32,768)
1000 0000 0000 0001	V_{REF} (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ (1/32,768)
0000 0000 0000 0000	$-V_{REF}$

1591/97 F02b

Figure 2b. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

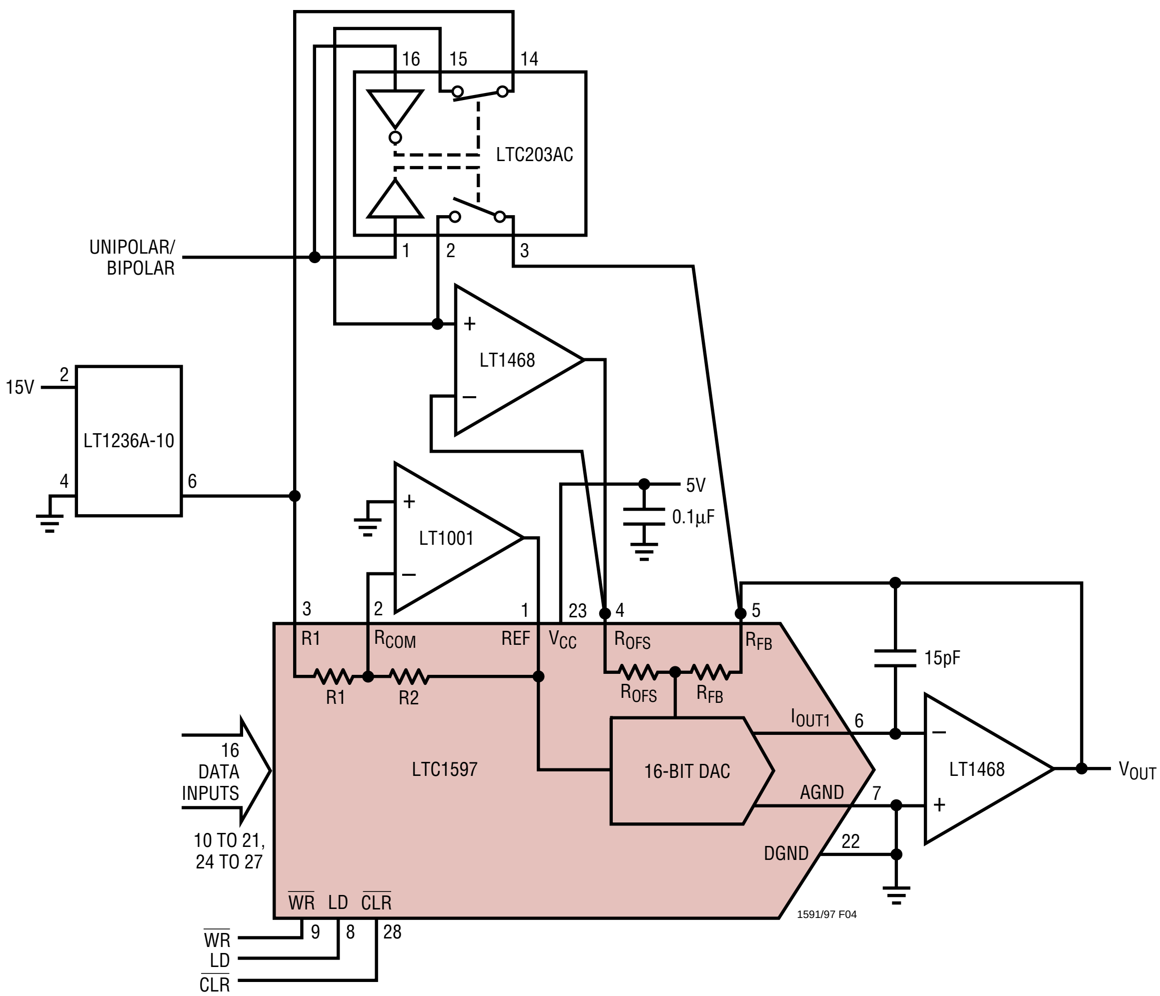
TYPICAL APPLICATIONS

Noninverting Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to V_{REF}



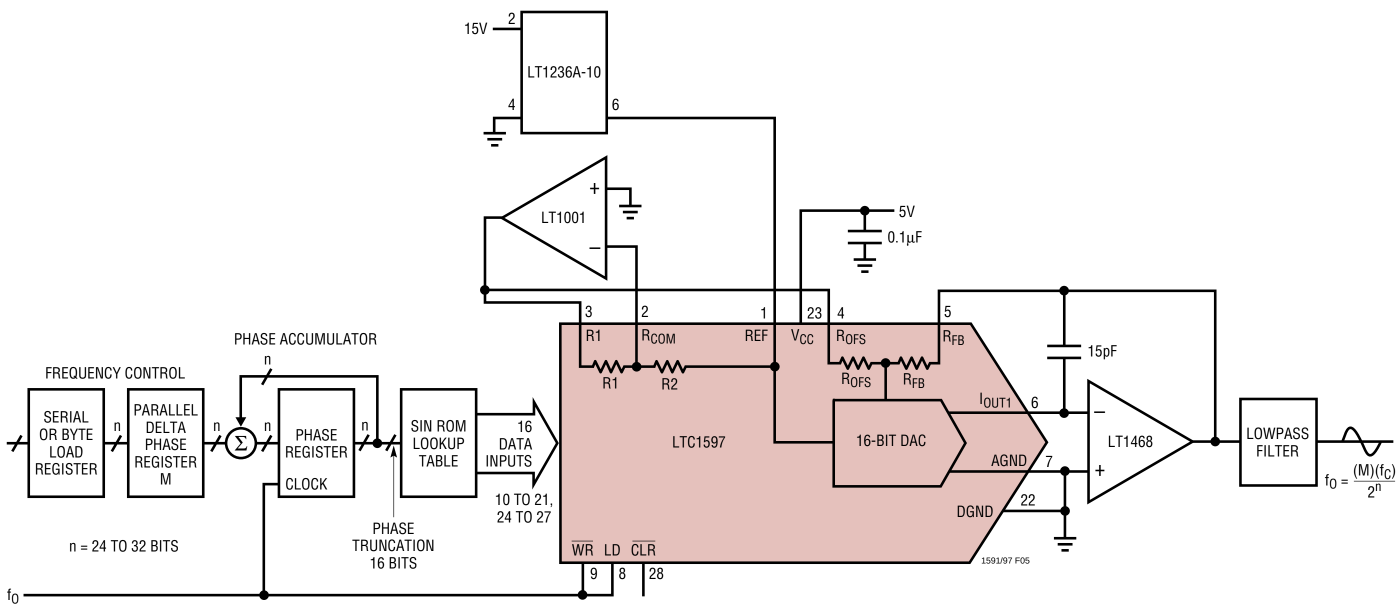
TYPICAL APPLICATIONS

16-Bit V_{OUT} DAC Programmable Unipolar/Bipolar Configuration



TYPICAL APPLICATIONS

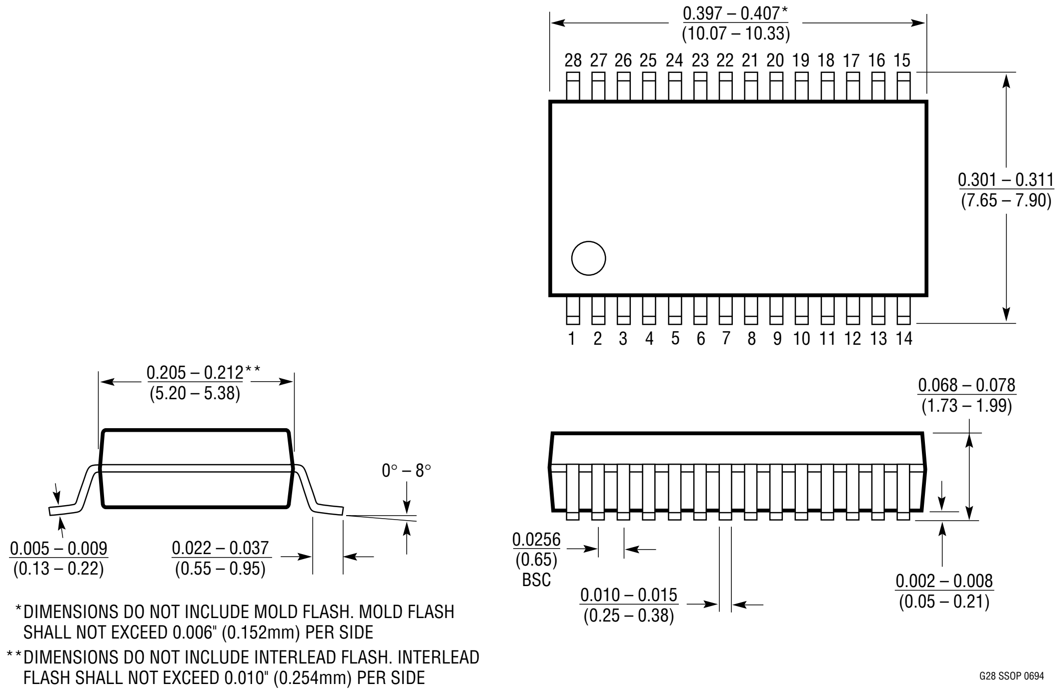
Digital Waveform Generator



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

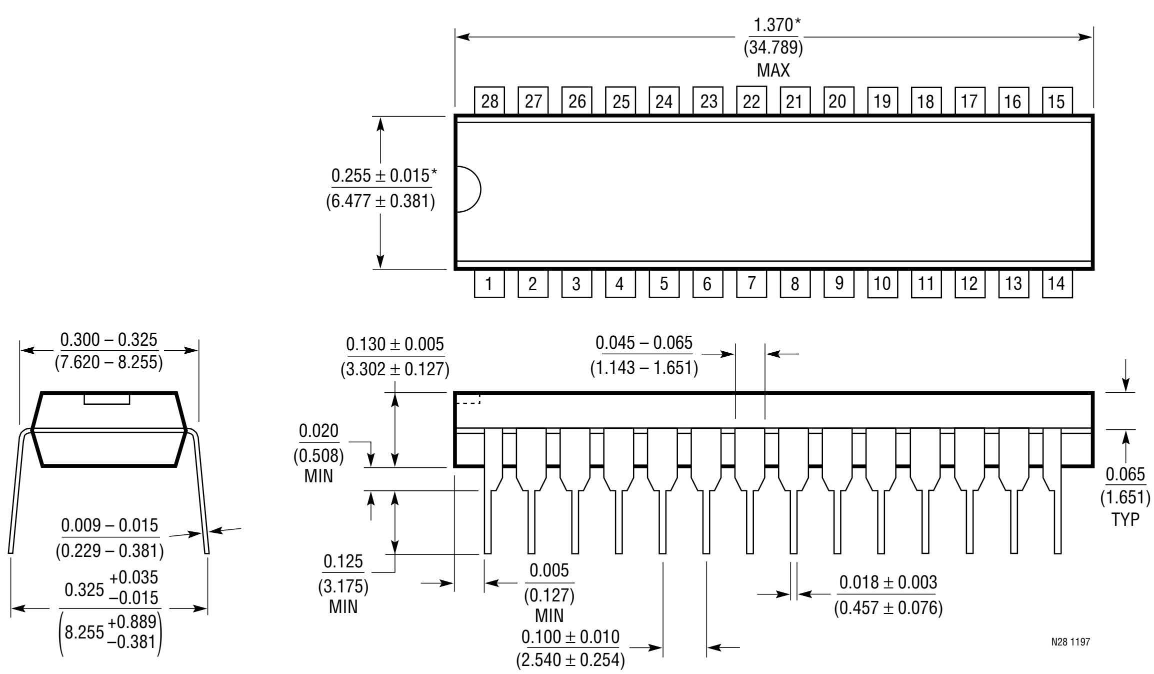
G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

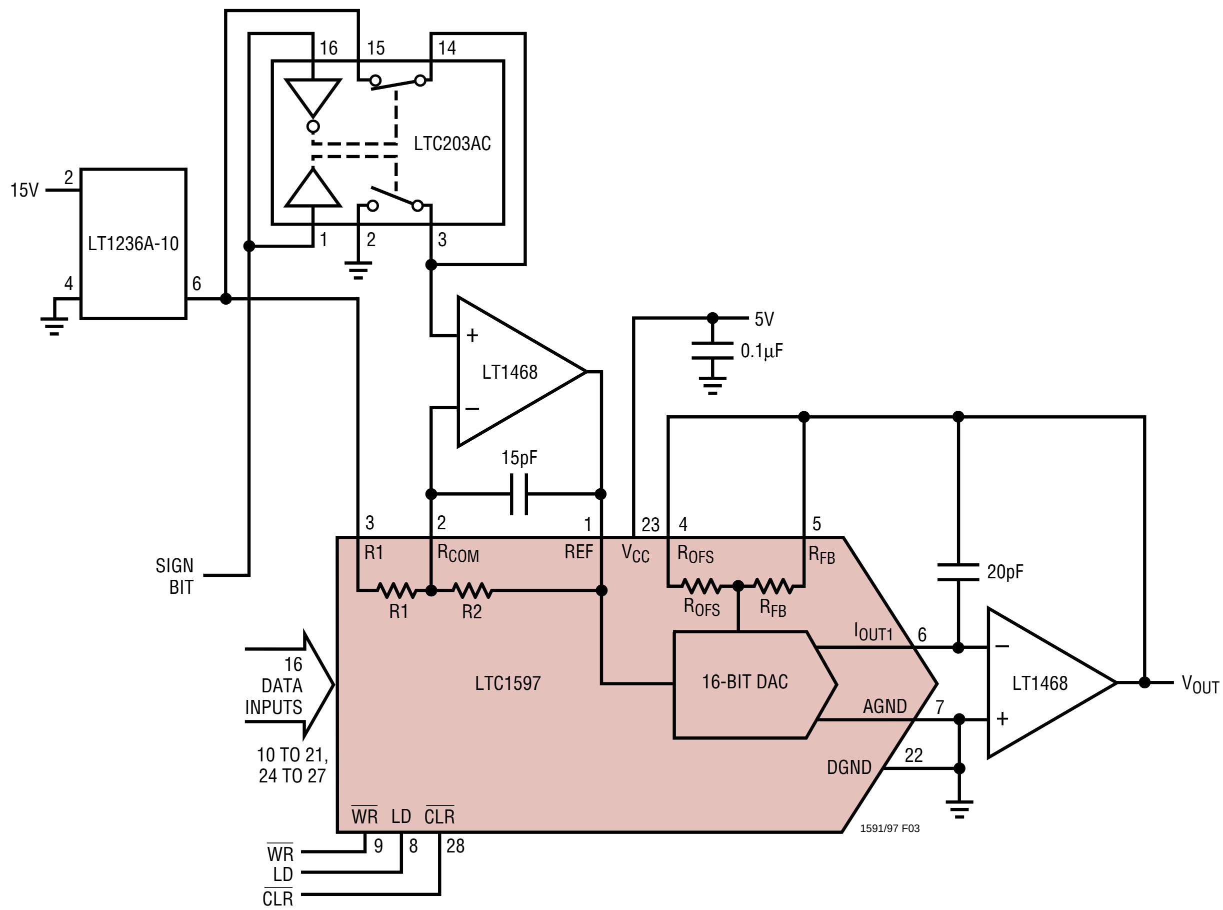
N Package
28-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

TYPICAL APPLICATION

17-Bit Sign Magnitude DAC with Bipolar Zero Error of 140μV (0.92LSB at 17 Bits) at 25°C



RELATED PARTS

PART NUMBER		DESCRIPTION	COMMENTS
Op Amps	LT1001	Precision Operational Amplifier	Low Offset, Low Drift
	LT1112	Dual Low Power, Precision Picoamp Input Op Amp	Low Offset, Low Drift
	LT1468	90MHz, 22V/μs, 16-Bit Accurate Op Amp	Precise, 1μs Settling to 0.0015%
DACs	LTC1595/LTC1596	Serial 16-Bit Current Output DACs	Low Glitch, ±1LSB Maximum INL, DNL
	LTC1650	Serial 16-Bit Voltage Output DAC	Low Noise and Glitch Rail-to-Rail VOUT
	LTC1658	Serial 14-Bit Voltage Output DAC	Low Power, 8-Lead MSOP Rail-to-Rail VOUT
ADCs	LTC1418	14-Bit, 200ksps 5V Sampling ADC	16mW Dissipation, Serial and Parallel Outputs
	LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = 100dB
	LTC1605	Single 5V, 16-Bit 100ksps ADC	Low Power, ±10V Inputs
References	LT1236	Precision Reference	Ultralow Drift, 5ppm/°C, High Accuracy 0.05%

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