



ICS580-01 Glitch-Free Clock Multiplexer

Description

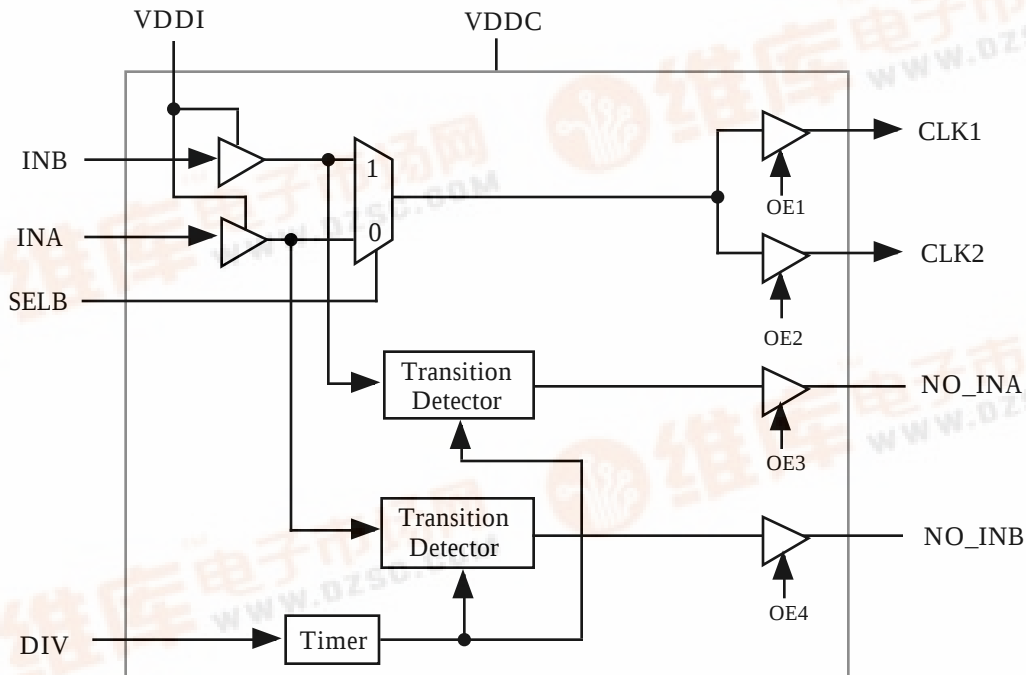
The ICS580-01 is a clock multiplexer (mux) designed to switch between 2 clock sources with no glitches or short pulses. The operation of the mux is controlled by an input pin but the part can also be configured to switch automatically if one of the input clocks stops. The part also provides clock detection by reporting when an input clock has stopped.

For a clock mux with zero delay and smooth switching, see either the ICS581-01 or ICS581-02.

Features

- Packaged in 16 pin narrow (150 mil) SOIC 
- No short pulses or glitches on output
- Operates to 200 MHz
- Does not add jitter or phase noise to the clock
- User controlled or automatic switching
- Low skew outputs
- Clock detect feature
- Ideal for systems with backup or redundant clocks
- Selectable timeouts for clock detection
- Separate supply voltages allow power supply voltage translation
- Operates to 2.5 V

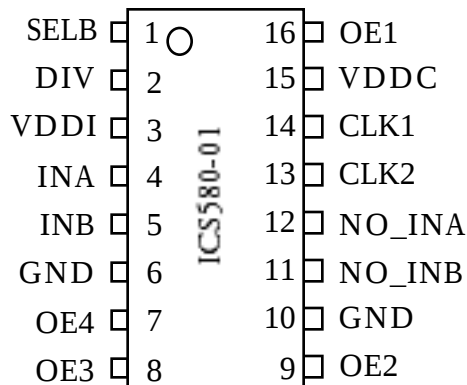
Block Diagram





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Pin Assignment



Timeout Selection

DIV	Nominal Timeout
0	600 ns
1	75 ns

Pin Descriptions

Number	Name	Type	Description
1	SELB	I	Mux select. Selects INB when high. Internal pull-up.
2	DIV	I	Time out select. See table above. Internal pull-up.
3	VDDI	P	Supply for input clocks only. Can be higher than VDDC.
4	INA	I	Input Clock A.
5	INB	I	Input Clock B.
6	GND	P	Connect to ground.
7	OE4	I	Output Enable. Tri-states NO_INB when low. Internal pull-up.
8	OE3	I	Output Enable Tri-states NO_INA when low. Internal pull-up.
9	OE2	I	Output enable. Tri-states CLK2 when low. Internal pull-up.
10	GND	P	Connect to ground.
11	NO_INB	O	Goes high when clock on INB stops.
12	NO_INA	O	Goes high when clock on INA stops.
13	CLK2	O	Clock 2 Output. Low skew compared to CLK1.
14	CLK1	O	Clock 1 Output. Low skew compared to CLK2.
15	VDDC	P	Main chip supply. Output clocks amplitude will match this VDD.
16	OE1	I	Output Enable. Tri-states CLK1 when low. Internal pull-up.

Key: I = Input; O = output; P = power supply connection



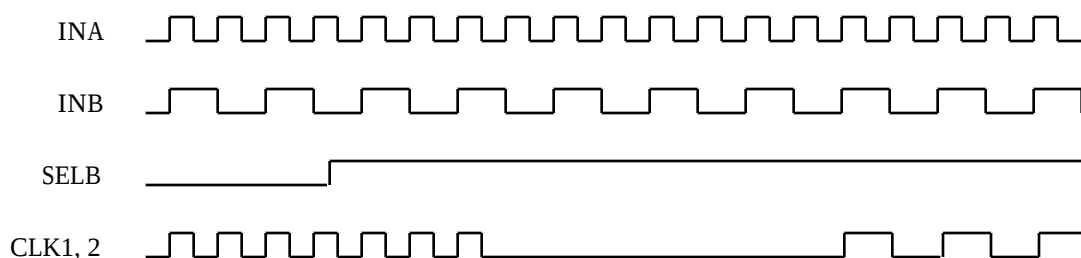
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Device Operation and Applications

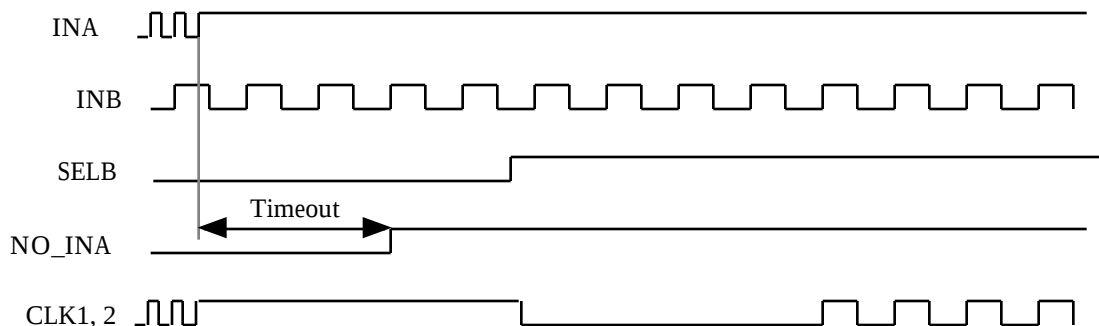
The ICS580-01 consists of a glitch free mux between INA and INB controlled by SELB. The device is designed to switch between 2 clocks, whether running or not. In the first example, clocks are running on both INA and INB. When SELB changes, the output clock goes low after 3 cycles of the output clock (nominally). The output then stays low for 3 cycles of the new input clock (nominally) and then starts with the new input clock. This is shown in Figure 1.

Figure 1



In the second example, one of the inputs was selected and running but has since stopped (either high or low). This is indicated by either NO_INA or NO_INB going high depending on whether INA or INB has stopped. These signals go high following a selectable time-out period after the clock has stopped. The timeout period is determined by the DIV input pin. The SELB pin is now changed to select the new input clock which is running. The output clock immediately goes low and stays low for 3 cycles of the new input clock and then starts with the new input clock. Figure 2 shows an example of this.

Figure 2



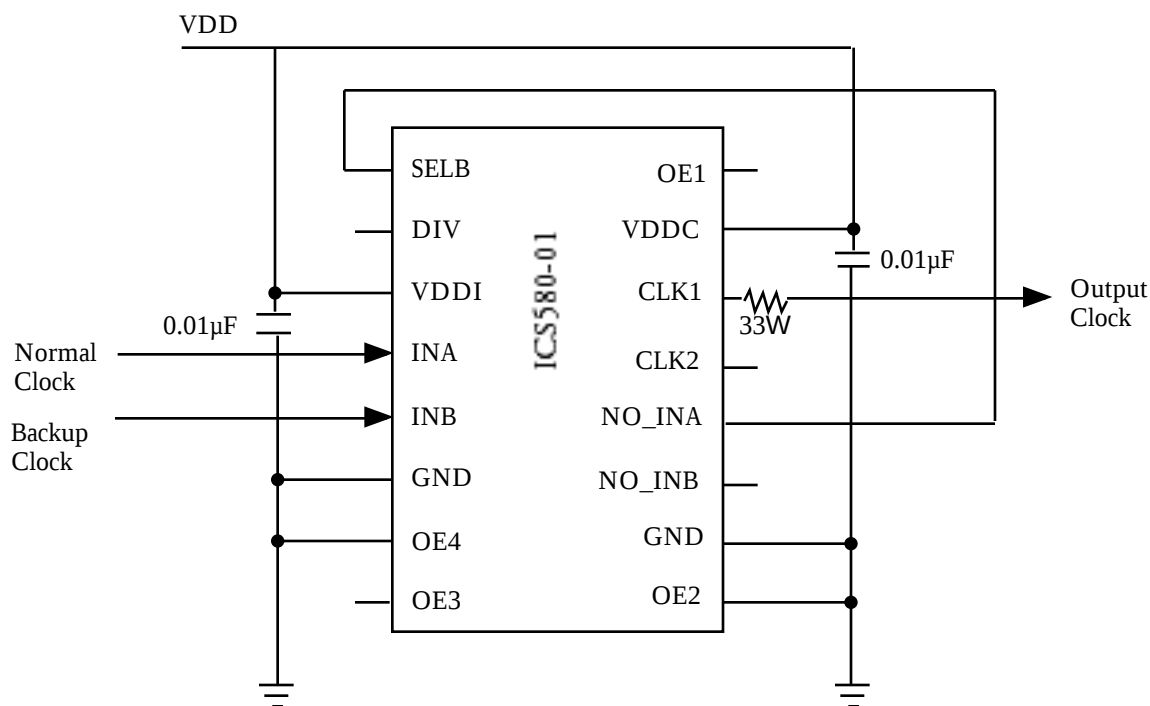


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In the third example, the ICS580-01 is configured to automatically switch clocks when an input stops. The clock that could stop is connected to INA while the backup, always running, clock is connected to INB. The output NO_INA is connected to SELB. This means that when the clock on INA stops, NO_INA goes high selecting the clock on INB which is muxed to the output after 3 cycles. When the clock on INA restarts, NO_INA immediately goes low, selecting the clock on INA. The output then switches in the manner described in the first example.

The circuit diagram in Figure 3 shows a typical connection for this example. Note that CLK2 and NO_INB are unused and so are disabled by grounding OE2 and OE4. A 33 Ω series termination resistor is used on the clock output and 2 decoupling capacitors of 0.01 μ F are used. All other inputs are left floating and are therefore pulled high by the on-chip pull-ups.

Figure 3



Output Enable

Each output has a dedicated output enable pin. If an output is unused, it should be tri-stated by tying the appropriate output enable pin to ground.

External Components

The ICS580-01 requires two 0.01 μ F decoupling capacitors, one between VDDI and GND and one between VDDC and GND. Series termination resistors of 33 Ω can be used on CLK1 and CLK2.

Split Power Supplies

The VDDI pin provides the power for the INA and INB input buffers only. All the other inputs and the rest of the chip are connected to VDDC. This allows for supply voltage translation. For example, INA and INB could be 5 V clocks (VDDI=5 V) and the rest of the chip could use a 3.3 V supply on VDDC giving 3.3 V output clocks. For correct operation VDDI must always be greater than or equal to VDDC.



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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Ambient Operating Temperature, I version	Industrial temperature	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDDC = VDDI = 3.3 V unless noted)					
Operating Voltage, VDDC		2.5		5.5	V
Operating Voltage, VDDI		VDDC		5.5	V
Input High Voltage, VIH, note 3	INA and INB only	(VDDC/2)+1	VDDC/2	VDDI	V
Input Low Voltage, VIL, note 3	INA and INB only		VDDC/2	(VDDC/2)-1	V
Input High Voltage, VIH	Non-clock inputs	2		VDDC	V
Input Low Voltage, VIL	Non-clock inputs			0.8	V
Output High Voltage, VOH	IOH=-12mA	VDDC-0.5			V
Output Low Voltage, VOL	IOL=12mA			0.5	V
Operating Supply Current, IDD	50 MHz inputs, no load		6		mA
Short Circuit Current			±70		mA
On-chip pull-up resistor, non-clock inputs	Pull-up to VDDC		250		kΩ
Input Capacitance			4		pF
AC CHARACTERISTICS (VDDC = VDDI = 3.3 V unless noted)					
Input Frequency, INA and INB. Note 1.	VDDC = 5 V	1/timeout		270	MHz
	VDDC = 3.3 V	1/timeout		220	MHz
	VDDC = 2.7 V	1/timeout		180	MHz
Propagation Delay, INA or INB to output	VDDC = 5 V		4	8	ns
	VDDC = 3.3 V		5	10	ns
	VDDC = 2.7 V		6	12	ns
Transition Detector Timeout, DIV=0	VDDI = 5 V	175	350	700	ns
	VDDI = 3.3 V	500	1000	2000	ns
	VDDI = 2.7 V	750	1500	3000	ns
Transition Detector Timeout, DIV=1	VDDI = 5 V	20	40	80	ns
	VDDI = 3.3 V	55	110	210	ns
	VDDI = 2.7 V	100	200	400	ns
Output Clock Rise Time				1.5	ns
Output Clock Fall Time				1.5	ns
Output Clock Skew, CLK1 to CLK2	Note 2	-250	0	250	ps

Note 1. Frequencies less than the minimum may cause a timeout, which will not guarantee glitch-free switching unless the clock is actually stopped.

Note 2. Assumes identically loaded outputs with identical rise times, measured at VDD/2.

Note 3. Output duty cycle is set by duty cycle of input clock at VDDC/2.

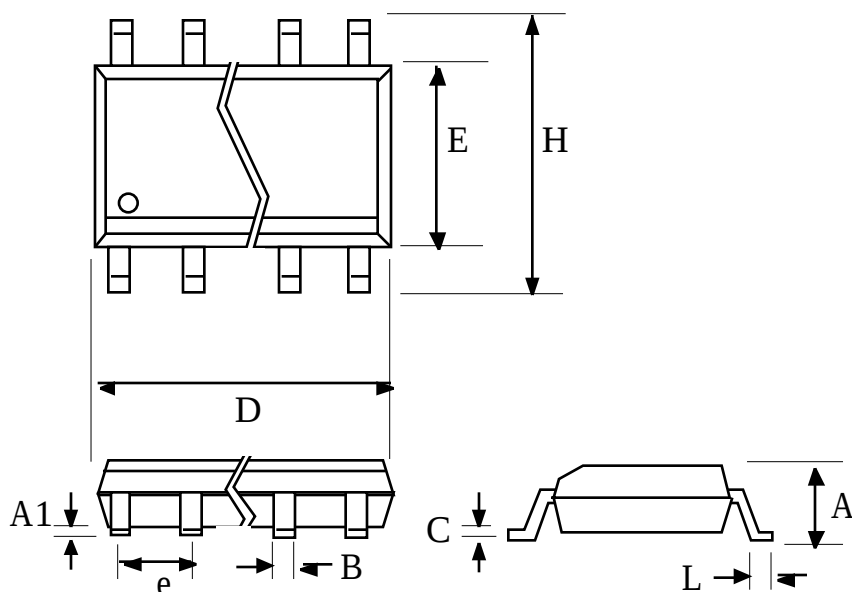


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Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC publication no. 95.)

16 pin SOIC narrow



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.059	0.069	1.50	1.75
A1	0.004	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.0098	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.05	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS580M-01	ICS580M-01	16 pin SOIC	0 to 70 °C
ICS580M-01T	ICS580M-01	16 pin SOIC on tape and reel	0 to 70 °C
ICS580M-01I	ICS580M-01I	16 pin SOIC	-40 to 85°C
ICS580M-01IT	ICS580M-01I	16 pin SOIC on tape and reel	-40 to 85°C

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