Galileo Technology, Inc.

Single-Chip System Controller

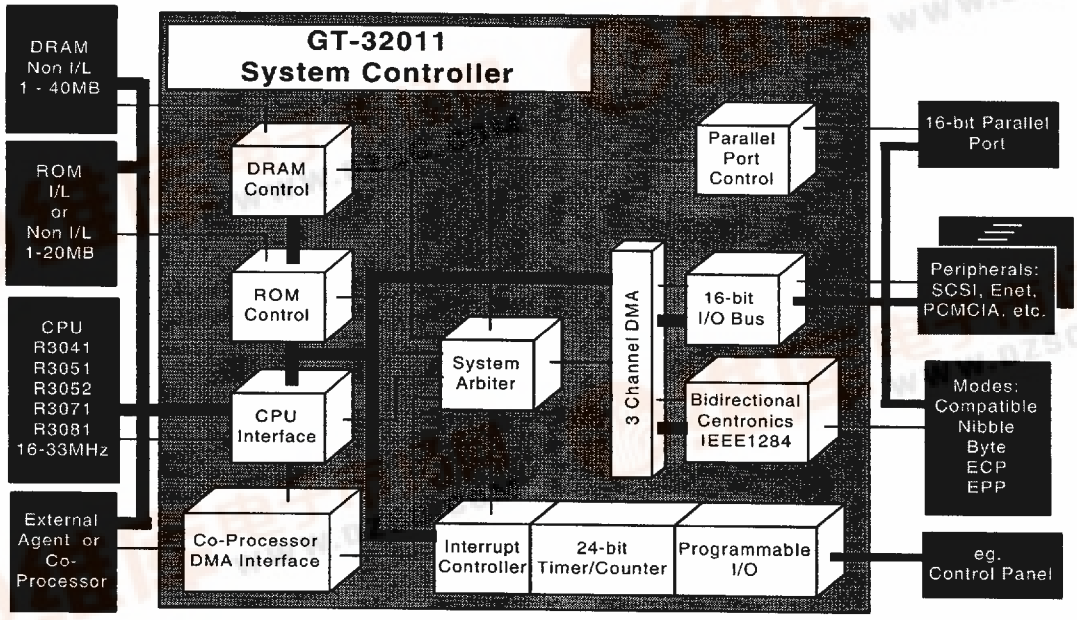
GT-32011

Rev. 2, July 95
Preliminary

NOTE: Always contact Galileo Technology for possible updates before starting a design.

FEATURES

- Single Chip System Controller for the IDT R3051 family of processors
- Features facilitate the implementation of high-performance embedded control systems
- 16Mhz - 33Mhz CPU interface to: R3041/51/52/71/81
- DRAM Controller
  - 1 - 40 MB directly
  - Device depth supported: 256K - 4M
  - 1 - 3 banks directly
  - Non-interleave
- ROM Controller
  - 1 - 20MB
  - Address-space support bank size: 1- 8MB
  - Support for standard and burst ROMs
  - Support for interleave or non interleave
- Direct Interface to External Agent/Coprocessor
- I/O Bus follows 8/16 Intel 80186 style
- I/O Controller
  - Two 8-bit and two 16-bit external channels
  - DMA and non-DMA access for the 8-bit channels
  - 8-32 packing and 32-8 unpacking logic for DMA access
  - Round robin arbitration
  - Programmable timing for I/O and control signals
  - Big and little endian support
  - 16-32 packing and 32-16 unpacking for CPU/ External Co-processor accesses
- PCMCIA Support
  - Through 16-bit I/O bus, using simple glue logic
  - 16-bit to 32-bit packing and 32-bit to 16-bit unpacking
  - Big and little endian support
  - 256MB address space dedicated for 2 PCMCIA slots
- Parallel Port
  - Supports control for reading and writing from a 16-bit parallel port
- Centronics Interface
  - Bi-directional Centronics, compliant with IEEE1284
  - Supports DMA and CPU controlled transfers
  - Supports the following modes:
    - Compatible; Nibble; Byte; ECP; EPP
- Interrupt Controller
  - 6 external level interrupts (through the PIO pins)
  - 10 internal interrupts
  - Individual interrupt mask capability, enabling polling or interrupt-driven systems
- General Purpose I/O
  - Six programmable Input (interrupts) or Output pins
- 24-bit Timer/Counter
- In-circuit testing capability
- Packaged in a 160-pin PQFP



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OVERVIEW

The GT-32011 is a single chip System Controller designed to complement IDT's R3051 family of 32-bit embedded processors. It has all the features necessary to implement high-performance, high-quality, embedded controllers. The GT-32011 is oriented towards data communications equipment, telecommunications equipment, office automation equipment, industrial and medical instrumentation, and industrial controllers.

The GT-32011 can move large amounts of data quickly without the need for processor intervention. It also achieves a significant reduction in system cost by its high level of integration. Additional savings come from the architecture of the I/O controller, which allows for the utilization of low cost peripheral components (disk controller, network controller, etc.), while attaining the higher level of performance only associated with costlier components.

Some of the architectural characteristics that result in very high performance include:

- incorporating a tightly coupled interface to a specific RISC processor architecture;

- minimizing latency to critical resources;

- partitioning the system in a balanced way to attain efficient use of shared resources;

- enabling several simultaneous operations in the system.

The GT-32011 is ideal for modular design of embedded control systems through a high level of programmability, and by incorporating the control logic for an industry standard interface to peripherals. This gives OEMs the ability to offer several products from the same basic design, as well as the ability to upgrade systems in the field.

1 PIN INFORMATION

1.1 Logic Symbol

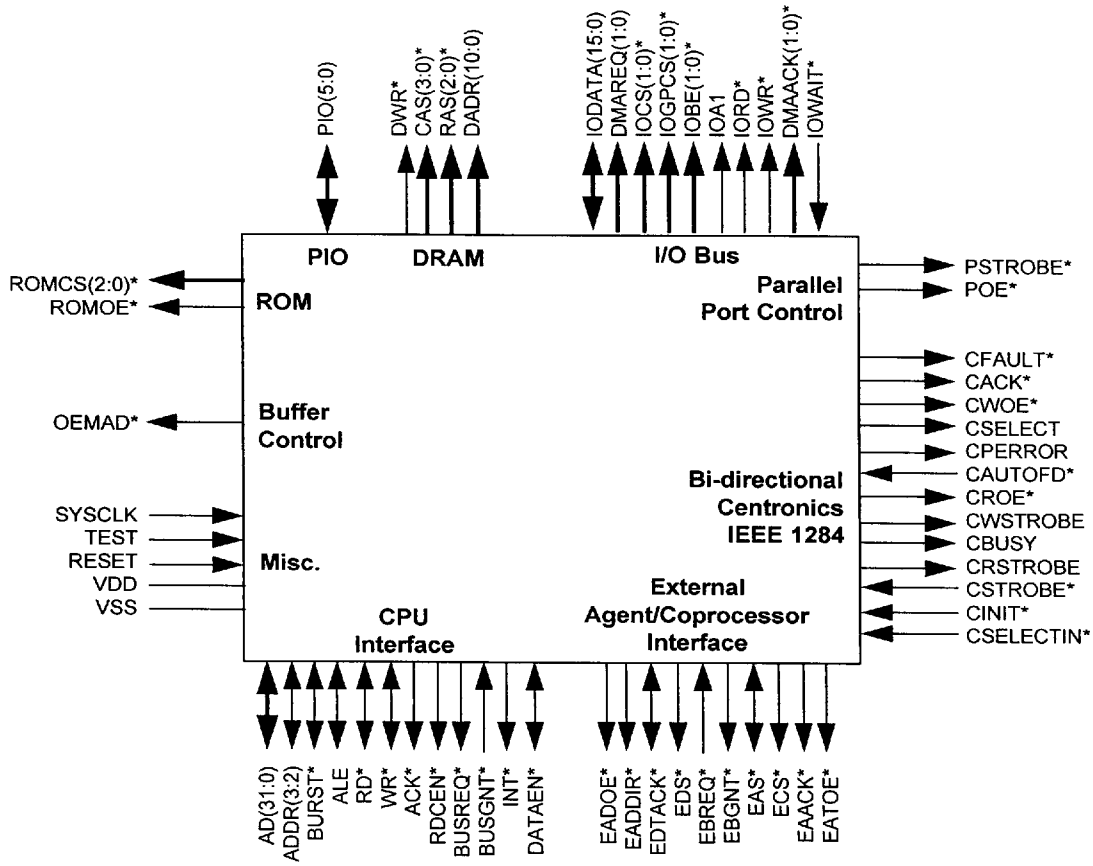


Fig. 1.1 : Logic Symbol

1.2 Pin Assignment Table

Pin Name	Pull Up/ Pull Dn	Type	Drive	Description
CPU Interface				
A/D[31:0]	P.U.	I/O	8mA	**Address/Data:** Multiplexed address and data bus. In the Address phase: A/D[31:4] are address, A/D[3:0] are Byte Enable[3:0]. During Coprocessor Master cycles, A/D[3:2] contain address bits 3 and 2, and not Byte Enables. In the Data phase: Data[31:0]
ADDR[3:2]	P.U.	I/O	4mA	**Non Multiplexed Address:** Connected to the CPU ADDR[3:2]. In DMA cycles the GT-32011 drives these lines.
BURST*	P.U.	I/O	2mA	**Burst Transfer:** Used only during read cycles, the BURST signal indicates that the current bus read is requesting a block of four continuous words from memory. The pin connects to the CPU's BURST/WRNEAR* signal. In DMA cycles the GT-32011 drives this signal HIGH.
ALE	P.D.	I/O	4mA	**Address Latch Enable:** Used by the CPU to indicate that the A/D bus contains valid address information for the bus transaction. During Coprocessor DMA cycles, the GT-32011 asserts ALE to capture the address supplied by the Coprocessor.
SYSCLK		I		**System Clock:** Connected directly to the CPU SYSCLK* output.
RD*	P.U.	I/O	2mA	**Read:** Indicates a read access by the CPU. In DMA cycles the GT-32011 drives the signal HIGH.
WR*	P.U.	I/O	2mA	**Write:** Indicates a write access by the CPU or the Coprocessor. In a non-Coprocessor DMA cycle the GT-32011 drives this signal HIGH.
ACK*		O	2mA	**Acknowledge:** Indicates that the memory system has sufficiently processed the bus transaction i.e. that the CPU may either terminate a write cycle or process read data.
RDCEN*		O	2mA	**Read Buffer Clock Enable:** Indicates to the CPU that there is valid data on the A/D bus.
BUSREQ*		O	2mA	**Bus Request:** The GT-32011 requests the CPU bus which is required for I/O and Coprocessor DMA's.
BUSGNT*		I		**Bus Grant:** Indicates that the CPU has relinquished the bus.
INT*		O	2mA	**Interrupt:** "OR's" the internal and external interrupt sources.
DATAEN*		I/O	4mA	**Data Enable:** indicates the data phase in CPU read cycles. In DMA the GT-32011 asserts DATAEN when the ROM/DRAM drives data onto A/D[31:0].
ROM				
ROMCS[2:0]*		O	4mA	**ROM Chip Select:** Select one of the 3 ROM banks. They can be connected to the ROM's Chip Select or Output Enable. ROMCS[2] is connected to the boot ROM, with a starting physical address 0x1fc00000.

Pin Name	Pull Up/ Pull Dn	Type	Drive	Description
ROMOE*		O	4mA	**ROM Output Enable:** Asserted when there is an access to any of the ROM banks. Used to output- enable the ROM data in systems where there is a buffer between ROM and DRAM data bus; eg. when using an interleaved ROM configuration.
DRAM				
DADR[10:0]		O	8ma	**DRAM Address:** Multiplexed row and column address connected to the DRAM address.
RAS[2:0]*		O	4mA	**Row Adress Select:** Supports up to three banks of DRAM, connected to the RAS inputs of the DRAMs.
CAS[3:0]*		O	4mA	**Column Address Select:** Connects a CAS to each of the four bytes in every bank.
DWR*		O	12ma	**DRAM Write:** Connects to the write pin of each of the DRAMs.
Coprocessor/ External Agent Interface				
EBREQ*	P.U.	I		**Ext. Agent Bus Request:** An Ext. Agent bus request to make system resource access in master mode.
EBGNT*		O	2mA	**Ext. Agent Bus Grant:** The GT-32011 asserts EBGNT* to grant the CPU bus to the Ext. Agent. Once the EBGNT* is asserted, it remains so until EBREQ* is deasserted.
EAS*	P.U.	I/O	2mA	**Ext. Agent Address Strobe:** Master Mode -The external agent indicates that it drives valid data on the A/D bus. Slave mode - The GT-32011 indicates that it drives valid data on the A/D bus.
EDS*		O	2mA	**Ext. Agent Data Strobe:** Master mode - during Write indicates that there is valid data on the A/D bus. During Read indicates a request for data. Slave mode - the GT-32011 drives EDS* to indicate that it is ready to accept data during reads or that valid data is available during writes on the A/D bus.
EDTACK*	P.U.	I/O	2mA	**Ext. Agent Data acknowledge:** Master mode - The GT-32011 asserts EDTACK* to indicate that it is receiving or driving the requested data to/from the A/D bus. Slave mode - The Ext. Agent asserts EDTACK* to signal that it has supplied or received data on its bus.
EAACK*		O	2mA	**Ext. Agent Address Acknowledge:** The GT-32011 asserts EAACK* one clock after asserting ALE for the Ext. Agent. This insures that the Ext. Agent continues driving the address until latched by the system.
ECS*		O	2mA	**Ext. Agent Chip Select:** When the CPU accesses the Ext. Agent, the GT-32011 asserts ECS*. It is active one clock before GT-32011 asserts EAS*.

Pin Name	Pull Up/ Pull Dn	Type	Drive	Description
EADOE*		O	4mA	**Ext. Agent A/D Output Enable:** The GT-32011 asserts EADOE* when the Ext. Agent drives the address to the A/D bus, and in the data phases of the Ext. Agent.
EADDIR*		O	4mA	**Ext. Agent A/D Direction:** The GT-32011 asserts EADDIR* (LOW) when the Ext. Agent drives the A/D bus.
EATOE*		O	4mA	**Ext. Agent Address To Output Enable:** The GT-32011 asserts EATOE* in the address phase of cycles in which the CPU accesses the Ext. Agent.
Buffer Control				
OEMAD*		O	4mA	**Output Enable between Memory and A/D:** Output enable for the data path transceiver, between the memory system and the A/D bus.
I/O Bus				
IODATA[15:0]	P.U.	I/O	8mA	**Input/Output Data:** Bidirectional 16-bit I/O Data bus.
IORD*		O	12mA	**Input/Output Read:** Active during Read from an I/O device.
IOWR*		O	12mA	**Input/Output Write:** Active during Write to an I/O device.
IOCS[1:0]*		O	2mA	**Input/Output Chip Selects:** Chip selects for 8 bit I/O channels 0 and 1.
IOGPCS[1:0]*		O	2mA	**Input/ Output Chip Selects:** Chip select outputs for 16 bit I/O channels 0 and 1.
DMAREQ[1:0]	P.D.	I		**DMA Request:** Requesting DMA service on channels 0 and 1.
DMAACK*[1:0]*		O	2mA	**DMA acknowledge:** Indicating that DMA access is granted on channels 0 and 1.
IOA1		O	8mA	**Input/Output Address bit 1:** Provides a half word (16 bit) address on the I/O bus.
IOBE[1:0]*		O	2mA	**Input/Output Byte Enable:** Indicates which byte data bus is valid on the 16 bit I/O bus.
IOWAIT*	P.U.	I		**Input/Output Wait:** Indicates to the GT-32011 that a transfer cycle on the I/O bus needs to be extended.
PIO[5:0]	P.U.	I/O	8mA	**Programmable Input/Output:** Individually programmed pins for inputs, interrupt inputs or outputs.
Bidirectional Centronics				
CWOE*		O	2mA	**Centronics Write Output Enable:** Controls the Output Enable signal of the data register -from the peripheral to the host.
CROE*		O	2mA	**Centronics Read Output Enable:** Controls the OE of the Centronics external register in the direction from the host to the peripheral (to the IODATA(7:0) bus).
CWSTROBE		O	2mA	**Centronics Write Strobe:** Clocks data from the IODATA(7-0) into the Centronics register (from peripheral to host).
CRSTROBE		O	2mA	**Centronics Read Strobe:** Clocks data from the host into the Centronics register (from host to peripheral).

Pin Name	Pull Up/ Pull Dn	Type	Drive	Description
CSTROBE*	P.U.	I		**Centronics Strobe:** Detailed description in section 4.1 of the IEEE P1284 D2.00 specification.
CACK*		O	2mA	**Centronics acknowledge:** Detailed description in section 4.3 of the IEEE P1284 D2.00 specification.
CBUSY		O	2mA	**Centronics Busy:** Detailed description in section 4.4 of the IEEE P1284 D2.00 specification.
CPERROR		O	2mA	**Centronics Printer Error:** detailed description in section 4.5 of the IEEE P1284 D2.00 specification.
CSELECT		O	2mA	**Centronics Select:** Detailed description in section 4.6 of the IEEE P1284 D2.00 specification.
CAUTOFD*	P.U.	I		**Centronics Autofeed:** Detailed description in section 4.7 of the IEEE P1284 D2.00 specification.
CINIT*	P.U.	I		**Centronics Initialize:** Detailed description in section 4.9 of the IEEE P1284 D2.00 specification.
CFAULT*		O	2mA	**Centronics Fault:** Detailed description in section 4.10 of the IEEE P1284 D2.00 specification.
CSELECTIN*	P.U.	I		**Centronics Select Input:** Detailed description in section 4.11 of the IEEE P1284 D2.00 specification.
Parallel Port Control				
PSTROBE*		O	2mA	**Parallel Strobe:** Clocks 8-bit or 16-bit parallel data from IODATA[15:0]
POE*		O	2mA	**Parallel Output Enable:** When active (LOW), it controls the output enable of a data buffer for8-bit or 16-bit wide parallel data into IODATA[15:0]
Misc.				
TEST	P.D.	I		**Master Output Enable:** When TEST is HIGH and RESET* is active, ALL the device outputs and I/Os are tri-stated (in a system, TEST should be pulled down to GND).
RESET*		I		**Reset:** Active low-will reset the GT-32011 to the initial state.
VDD				**+5V** (+/-5%)
VSS				**Ground**

NOTE: Pull Up/Pull Dn designates those pins with internal Pull Up (P.U.) or Pull Down (P.D.) resistors

2 FUNCTIONAL DESCRIPTION

2.1 Processor Interface

The GT-32011 has a glueless interface to the IDT R3041/51/52/71/81 family of RISC processors. It operates as a slave - supporting CPU access to memory and I/O devices, or as a master - handling access on the A/D bus.

As a slave the GT-32011 supports processor single transfer read or write, and burst read accesses. It supports processor access to the ROM, DRAM, devices on the I/O bus, the external agent/coprocessor and the GT-32011 internal registers. Burst read is supported only for DRAM or ROM read accesses. ACK* and RDCEN* timing is fixed for GT-32011 registers. DRAM access can be extended by one clock, and access timing for ROM and I/O is programmable.

As a master the GT-32011 will request the bus by asserting BUSREQ* when a DMA source (internal or external) needs to transfer data to or from the DRAM / ROM / I/O Channel. The priority between the DMA sources is in the following descending order: access in process; I/O DMA; external agent/coprocessor DMA.

In the default state, when there is no DMA request, the bus is owned by the CPU. The CPU will get ownership of the A/D bus for at least one cycle after three DMA accesses.

2.2 Co-Processor/External Agent Interface

The GT-32011 has a glueless interface to an external agent or coprocessor. It supports slave and master modes of operation. As a slave it supports the processor read and write accesses to the coprocessor, and as a master it enables coprocessor access to the DRAM, ROM, and 16 bit I/O bus. The GT-32011 directly controls the data buffers and the address needed to isolate the external agent/coprocessor from the A/D bus.

The GT-32011 decodes CPU accesses to the coprocessor and asserts ECS*, EAS* and EDS*. The address is latched into an external transparent latch (373-type) when the processor asserts ALE and driven into the a coprocessor bus by EATOE*. Data is driven to or from the coprocessor by transceivers controlled by EADDIR and EADOE. To end a coprocessor cycle the GT-32011 asserts RDCEN* and ACK* to the CPU, when the coprocessor asserts EDTACK*.

In coprocessor master mode, the coprocessor requests the bus by asserting EBREQ*. The GT-32011 will grant the bus by asserting EBGNT* (provided no other DMA device has requested the bus and it was granted by the CPU to the GT-32011). The coprocessor will assert EAS* and EDS* to initiate an access to a system resource (e.g. DRAM). The GT-32011 will assert EADOE* and EADDIR* to drive the coprocessor address and ALE to latch it. In the data phase it will assert EADDIR* and EADOE* according to the access direction (Read or Write). To end the cycle the GT-32011 will assert EDTACK* to the coprocessor.

The coprocessor will release the bus by deasserting EBREQ* when it does not require the bus any longer.

A coprocessor access to the DRAM takes 5 clocks from EAS* to EDTACK*. One clock can be added to this interval (for frequencies above 25Mhz) using the EAExtCas bit in the DRAM control register if necessary.

The coprocessor/external agent interface can support both multiplexed bus and non-multiplexed bus agents. By using glue logic, it is possible to interface to an even greater variety of buses and coprocessors.

2.3 ROM

The ROM controller supports up to 20 Mbyte of memory with several device types and system configurations. To support these system and device options, the assertion time of RDCEN* and ACK* by the GT-32011GT-32011 can be programmed, thus accommodating different types of memory architectures, including standard ROMs, interleaved ROMs, and burst ROMs. There are three CS signals to support up to three banks of ROM. The ROM can be either non interleaved or interleaved - composed of 2 banks of ROM differentiated by ADDR[2]. ROMCS[2]* controls the boot bank and has a fixed address space of 4 Mbyte. Address space for ROMCS[1]* and ROMCS[0]* is programmable to 1, 2, 4, or 8 Mbyte. The GT-32011 puts the 3 ROM bank address ranges in a contiguous address space, ie. the start address of the next ROMCS[x]* will follow the last address of the previous ROMCS[x-1]*. For interleaved support, ROMOE* is provided to control the OE of the interleave multiplexer. The GT-32011 also supports burst ROMs and the capability to write to the ROM space (for Flash or debug).

After reset, the GT-32011 is configured with the maximum number of wait states between each data transfer (16 clocks between each RDCEN*) and 64 clocks between ROMCS[x]* to ACK*. The initial (reset) space size for ROMCS[1]* and ROMCS[0]* is 1 Mbyte, and 4Mbytes for ROMCS[2]*.

2.4 DRAM

The DRAM controller supports directly 1 to 40 Mbytes of DRAM, with up to three non-interleaved banks. The address space starts at physical address 0. The DRAM

device types supported have the following attributes: page mode, early write, and CAS before RAS refresh. The DRAM controller supports single transfer reads and writes and burst reads. Various DRAM device depths are supported and the address space is continuous for the selected configuration. The DRAM controller can be configured to support different device depth for the base bank (RAS 0) and the extension banks (RAS 1 and RAS 2). For systems running at 33Mhz there is an option to extend the CAS signal by an additional cycle. Since a coprocessor might sample data on the rising edge of SYSCLK, and the CPU on the falling edge, for systems above 20Mhz it may be necessary to extend the CAS by one cycle for coprocessor accesses. To minimize the refresh penalty it is recommended to program the refresh frequency to the value of SYSCLK.

The initial values of the GT-32011 at reset are shown in section 3.12.

2.5 PIO Port

Each of the PIO[5:0] pins can be individually programmed to be an output or input pin by writing to the PIO Control register. When programmed as an input pin it can be used as a level (active LOW) interrupt. The PIO pins are synchronized and pulled up internally.

At reset, all PIOs are initialized as inputs.

2.6 Interrupt Controller

Each interrupt source on the GT-32011 is maskable. The Cause register bit will reflect the cause of the interrupt, and writing a '0' into it will acknowledge the internal interrupt.

The external interrupts - PIO[5:0], are acknowledged at the source of the interrupt (the interrupt flag is set when PIO is inactive), the corresponding bits in the Interrupt Cause register are read only.

At reset, all interrupts are masked in the mask register.

2.7 Timer/Counter

The general purpose timer/counter can be programmed to function as a timer or as a counter. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will start the counter if the Enable bit is active. As a timer on terminal count, it will cause an interrupt, reload with the value stored in the Timer/Counter Value register and continue to count.

The Timer/Counter counting is enabled or disabled by the enable bit. The value n should be written to the Counter in order to count to n clocks. At reset, the counter is disabled.

2.8 I/O Bus

The GT-32011 supports two 8-bit (IOCS[1:0]*) and two 16-bit (IOGPCS[1:0]*) external I/O channels, that share the IODATA[15:0] pins. The two 8-bit I/O channels and the first 16-bit I/O channel (IOGPCS[0]*) each has a 16 Mbyte address space. The second 16 bit I/O channel (IOGPCS[1]*) has a 256Mbyte address space.

Timing of the control signals to an I/O channel is programmable. The user can specify the length of IORD* and IOWR* signals. The IOCS[1:0]*, IOGPCS[1:0]* or DMAACK[1:0]* are asserted one cycle before the IORD* or IOWR* signals become active, and remain active for one cycle after IORD* or IOWR* are de-asserted. RDCEN* and ACK* will be asserted by the GT-32011 to end a processor (or EDTACK* to end a coprocessor I/O cycle).

8-bit I/O Channels

The GT-32011 supports processor byte accesses (reads and writes) to devices located on the two 8 bit I/O channels. These accesses can be made using any of the four bytes on the 32 bit data bus, the GT-32011 will transfer the correct byte (according to the 4 Byte Enables) to the 8 bit I/O bus (IODATA[7:0]).

The GT-32011 I/O channel unit operates as a DMA controller with the two 8 bit I/O channels. DMA operations between I/O devices and the DRAM are supported. Eight bit data is packed or unpacked during DMA access into a 32 bit register for I/O DMA read or write respectively.

Processor requests have priority over DMA requests. The priority for DMA operations is round robin for the Centronics and the two external 8-bit DMA engines. DMAREQ[1:0] can be masked by writing '0' to the enable bit of the channel. A channel will not participate in the arbitration if the channel is disabled or if the I/O BIU (Bus Interface Unit) is owned by another channel. The I/O BIU is emptied into memory in a DMA read access if the I/O BIU is full, or if there is no DMA request (DMAREQ[1:0]) from the channel which owns the I/O BIU for a time out period or the byte count reaches zero. In the write direction if the DMAREQ from the channel that owns the I/O BIU is not active for a time out period, and the I/O BIU is not empty, arbitration will resume on the I/O bus. The time out period is set to 32 clocks.

16-bit I/O Channels

The GT-32011 supports processor and coprocessor

accesses (reads and writes) to devices located on the two 16-bit I/O channels.

For 16-bit devices, the CPU can read or write to any byte or half word. Processor or coprocessor access to the 16-bit I/O channels with any combination of byte enables active, will be performed in two consecutive I/O cycles in case of 3 or 4 byte accesses. In the two cycles, data will be packed or unpacked from a 32-bit register for an I/O read or write respectively. Conversion between big and little endian is supported for 16-bit devices.

The following signals support a parallel port interface: *a)* Parallel Strobe (PSTROBE*) - Clocks data out from IODATA[15:0] and *b)* Parallel Output Enable (POE*) - controls the output enable of an external buffer.

2.9 Centronics IEEE 1284 Communication

NOTE: Due to the scope of this data sheet, it would be impossible to cover every aspect of the IEEE 1284 bi-directional Centronics standard. Designers are urged to study the IEEE1284 Rev. 2 specification.

The Centronics implementation meets the IEEE 1284 definition of a compliant device. It supports the following modes: Compatible, Nibble, Byte, ECP and EPP, as well as the negotiation necessary for transition between different modes. Support for the Compatible mode includes the following three variations: Standard, IBM Epson, and Classic. There are two ways to handle the Centronics protocol: In the first option, data is transferred in DMA fashion and is only applicable in the Compatible, ECP, and EPP modes. The second option is interrupt driven, and applies to all modes. That is, Byte and Nibble modes are only interrupt driven. There is support for special character detection in the Centronics incoming data. Control data characters like ^C or ^T can be detected and the CPU will be interrupted.

Negotiation

The GT-32011 defaults after reset to Compatible mode. The negotiation phase starts when the host sets CSELECTIN* HIGH and CAUTOFD* LOW. The GT-32011 interrupts the CPU by asserting the CentWrInt interrupt. The CPU interrupt routine includes reading the extensibility request value from the Centronics External register (0a000000), and writing to the Centronics Control register to specify the supported mode. Note that the interpretation of the CenRdInt and CentWrInt interrupts, and the interrupt handler response, will be different in each mode. Table 2.1 summarizes the values of host requests and the CPU interrupt routine response.

Compatible Mode

The CPU needs to configure the Compatible mode to one of the three supported modes: IBM, Classic or Standard, and to a data transfer option (DMA or interrupt per byte). Setting the modes and options is done by writing to the mode register (values are specified in the Centronics Mode register table).

In the interrupt per byte mode, the CPU will read data from the Centronics External register every time it responds to the CentRdInt interrupt. In DMA mode the CPU will initialize the DMA registers (addresses 1d0000a0, 1d000080 & 1d00098) before starting the DMA operation.The GT-32011 will assert interrupt CentDMAInt when the DMA counter will reach terminal count.

Table 2.1: Interrupt Responses During Negotiation Phase

Request mode	Request value	Interrupt response: mode supported value	Interrupt response: mode not supported value
Extensibility link first byte	1000 0000 xxxx xxxx	1110 1xxx	0111 0110
EPP	0100 0000	1100	0111
ECP with RLE	0011 0000	1011	0111
ECP	0001 0000	1011	0111
Device ID: -Nibble -Byte -ECP with RLE -ECP without RLE	 0000 0100 0000 0101 0001 0100 0011 0100	 1001 1010 1011 1011	 0111 0111 0111 0111
Byte	0000 0001	1010	0111
Nibble	0000 0000	0001	1111

A host request to return to compatibility mode from any of the other modes is indicated to the CPU by the assertion of the CentRstInt interrupt.

Nibble Mode

The GT-32011 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to the Nibble data register. The GT-32011 sends the byte to the host over the control lines in two consecutive nibble transactions.

Byte Mode

The GT-32011 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to Centronics External register.

Extensibility Link

Assertion of CentWrInt interrupt while in Compatibility mode indicates to the CPU an extensibility request. The CPU will read from the Centronics External register the extensibility request value, and write to the control register the next mode and proper response.

ECP Mode

DMA and interrupt per byte options are supported for the ECP mode.

In the interrupt per byte option, the GT-32011 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt.

In reverse transfer, in response to CentWrInt, the CPU must first write to the Centronics status register (to the Busy bit). This indicates whether the CPU sends a command or data byte, and then write the data to the Centronics External register.

In forward transfer, in response to CentRdInt the CPU needs to read from the Centronics host register (Autofeed bit) to know whether the host is sending data or command, and then read the data from the Centronics register.

RLE compression is supported only in interrupt per byte mode.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA. CentWrInt will be asserted when the host requests data and the DmaDir bit in the Mode register indicates a read direction (From the IEEE1284 port to memory). CentRdInt will be asserted when the host sends data and the DmaDir bit indicates a write direction or when the host sends a command byte.

EPP Mode

DMA and interrupt per byte options are supported for the EPP mode.

In the interrupt per byte option, the GT-32011 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt. It will distinguish between data and address by the contents of the strobe Selectin and AutoFd bits in the host
buffer.
In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA. CentWrInt will be asserted when the host requests data

and the DmaDir bit in the Mode register indicates a read direction (from the Centronics port to memory) or when the host asks for an address byte. CentRdInt will be asserted when the host sends data and the DmaDir bit indicates a write direction or when the host sends an address byte.

CPU Control

This mode enables the CPU to set the values of the Centronics status register, and communicate with the host in compatible mode.

Character Detection.

The value of the three CentDetect 8-bit registers is constantly compared to the Centronics incoming data. When a match occurs the CPU is interrupted. Characters as ^C or ^T can be detected during Centronics DMA operations and the CPU can respond without the need to wait to the end of the DMA operation.

Programmable Timing

To allow for higher than specified (by the IEEE1284 standard) data rates, the minimum delay can be programmed to values lower than the minimum required by this standard.

3 REGISTER TABLES

3.1 Register Map

Description	Address	Description	Address
ROM Configuration	0x1d000000	DMA Centronics Count	0x1d000098
Reserved	0x1d000020	I/O Channel Timing	0x1d0000a0
PIO Value	0x1d000040	Reserved	0x1d0000c0
PIO Control	0x1d000044	Reserved	0x1d0000c4
PIO Read Pins	0x1d00005c	Reserved	0x1d0000c8
Timer/Counter Value	0x1d000048	Reserved	0x1d0000cc
Timer/Counter Control	0x1d00004c	Reserved	0x1d0000do
Interrupt Cause	0x1d000050	Centronics Status	0x1d000100
Interrupt Mask	0x1d000054	Centronics Control	0x1d000104
Interrupt Write	0x1d000060	Centronics Nibble Data	0x1d000108
Test	0x1d000064	Centronics Host	0x1d00010c
DRAM Control	0x1d000058	Centronics Mode	0x1d000110
DMA Address 0	0x1d000080	Centronics Minimum Delay	0x1d000114
DMA Address 1	0x1d000084	Centronics Data Detect 0	0x1d0000a4
DMA Centronics Address	0x1d000088	Centronics Data Detect 1	0x1d0000a8
DMA Count 0	0x1d000090	Centronics Data Detect 2	0x1d0000ac
DMA Count 1	0x1d000094		

NOTES: ***a) In all the following Tables, bit 0 is the Least Significant Bit.***

b) Most counters need to be loaded with the value n-1 in order to count to n. Please keep this in mind and take careful note of the few exceptions.

c) Reads and writes from/to the GT-32011 internal registers should be word (32-bit) accesses.

d) The 0x notation indicates hexadecimal values, as in C language notation.

3.2 ROM Configuration

This register is used to set the ROM address space for the 2 configurable ROM banks (ROMCS[1:0]*) and to set the

number of wait state cycles inserted between data phases.

Address: 1d000000

Bits	Field name	Function	Initial Value
0-3	First	The gap (number of cycles) from ROMCS* active to the first RDCEN*. The range is 16 cycles. 0000 - 16 cycles 0001 - 1 cycle n - n cycles (except for 0000)	0xf
4-7	Gap1	The gap between the first RDCEN* and the second RDCEN*. The range is 16 cycles. 0000 - 16 cycles 0001 - 1 cycle n - n cycles (except for 0000)	0xf
8-11	Gap2	The gap between the second RDCEN* and the third RDCEN*. The range is 16 cycles. 0000 - 16 cycles 0001 - 1 cycle n - n cycles (except for 0000)	0xf
12-15	Gap3	The gap between the third RDCEN* and the fourth RDCEN* The range is 16 cycles. 0000 - 16 cycles 0001 - 1 cycle n - n cycles (except for 0000)	0xf
16-21	AckTime	The gap from ROMCS* active to AckTime in block read. The range is 64 cycles. 000000 - 64 cycles 000001 - 1 cycle n - n cycles (except for 000000)	0x3f
22-23	SpaceSize	ROMCS[1:0]* address space size (ROMCS[2] has a fixed 4Mbyte address space) 00 - 8 Mbyte 01 - 4 Mbyte 10 - 2 Mbyte 11 - 1 Mbyte	0x3

Note: It is the user's responsibility to set AckTime timing correctly.

3.3 PIO Value

This register is used to set the value for those PIO pins configured by the PIO Control register as outputs.

Address: 1d000040

Bits	Field name	Function	Initial Value
0-5	PIO Value	Value of the PIO pins configured as outputs	0x0

3.4 PIO Control

This register sets the direction of the PIO pins.

Address: 1d000044

Bits	Field name	Function	Initial Value
0-5	PIO Control	Sets the direction of the corresponding PIO pin: 0 - Output 1 - Input	0x3f
6	Reserved	Must be 0	0

3.5 PIO Read Pins

This address is used to read inputs from the PIO pins

Address: 1d00005C

Bits	Field name	Function	Initial Value
0-5	PIO Input Value	Value on the PIO pins	

3.6 Timer/Counter Value

This register is used to set the number of clocks to be counted by the Timer/Counter.

Address: 1d000048

Bits	Field name	Function	Initial Value
0-23	T/C Value	Number of clocks to count. Set to n to count to n.	0x000000

3.7 Timer/Counter Control

This register is used to enable and disable the Timer/Counter and to select the specific mode of use.

Address: 1d00004c

Bits	Field name	Function	Initial Value
0	Enable	Timer/Counter count enable 0 - Disable 1 - Enable	0x0
1	Select	Select mode of operation 0 - Counter 1 - Timer	0x0

3.8 Interrupt Cause

This register is used to identify the source behind an interrupt ; it can also be used for polling of a specific interrupt or set of interrupts. A value of 1 indicates assertion of the interrupt. This register is also used to clear internal interrupts, writing a 0 will reset the corresponding internal interrupt. Writing a 1 will have no effect on the interrupt. External interrupts should be cleared via an external mechanism.

Address: 1d000050

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

3.9 Interrupt Mask

This interrupt is used to mask (disable) specific interrupt sources, both internal and external (PIO). All the interrupts are maskable. A value of 0 masks the corresponding interrupt.

Address: 1d000054

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		

Bits	Field name	Function	Initial Value
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CenRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

3.10 Interrupt Write

This register is used to write to the Interrupt Cause register. This register should be used for interrupt testing only.

Address: 1d000060

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	

Bits	Field name	Function	Initial Value
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	

3.11 Test

No reading or writing from/to this address.

Address: 1d000064

3.12 DRAM Control

This register is used to set the desired DRAM device depth, access time (both for the CPU and Coprocessor) and refresh frequency.

Address: 1d000058

Bits	Field name	Function	Initial Value
0-2	DevDepth Bank 1-2	Depth of the DRAM device used. 000 - 256K 001 - 512K 010 - 1M 011 - 2M 100 - 4M	0x0
3-4	DevDepth Bank 0	Depth of the DRAM device used. 00 - 256K 01 - 512K 10 - 1M 11 - 2M	0x0
5	ExtCas	CAS duration for both CPU and Coprocessor accesses 0 - CAS is active for one and a half cycles 1 - CAS is active for two and a half cycles	0x0
6	EAExtCas	CAS duration for Coprocessor accesses only 0 - CAS is active in Coprocessor accesses for one and a half cycles 1 - CAS is active in Coprocessor accesses for two and a half cycles	0x0
7-8	RefFreq	SYSCLK frequency 00 - 15.6 uS refresh time at 16Mhz 01 - 15.6 uS refresh time at 20Mhz 10 - 15.6 uS refresh time at 25Mhz 11 - 15.6 uS refresh time at 33Mhz	0x0

3.13 DMA Address 0

This register is used to set the first DRAM address used in channel 0 DMA operations.

Address: 1d000080

Bits	Field name	Function	Initial Value
0-25	DmaAddr0	First address for DMA channel 0.	0x0

3.14 DMA Address 1

This register is used to set the first DRAM address used in channel 1 DMA operations.

Address: 1d000084

Bits	Field name	Function	Initial Value
0-25	DmaAddr1	First address for DMA channel 1.	0x0

3.15 DMA Centronics Address

This register is used to set the first DRAM address used in Centronics DMA operation.

Address: 1d000088

Bits	Field name	Function	Initial Value
0-25	DmaAddrCent	First address for Centronics DMA.	0x0

3.16 DMA Count 0

This register is used to set the number of bytes to be transferred in a channel 0 DMA operation.

Address: 1d000090

Bits	Field name	Function	Initial Value
0-15	DmaCnt0	DMA count channel 0. Load with n-1 to transfer n.	0x0

3.17 DMA Count 1

This register is used to set the number of bytes to be transferred in a channel 1 DMA operation.

Address: 1d000094

Bits	Field name	Function	Initial Value
0-15	DmaCnt1	DMA count channel 1. Load with n-1 to transfer n.	0x0

3.18 DMA Centronics Count

This register is used to set the number of bytes to be transferred in a Centronics DMA operation.

Address: 1d000098

Bits	Field name	Function	Initial Value
0-15	DmaCntCen	Centronics DMA count. Load with n-1 to transfer n.	0x0

3.19 I/O Channel Timing

This register is used to configure the I/O bus parameters, including signal timing; DMA enabling , time-out, and direction; and the endianess of the 16-bit I/O channels. The DevTime fields specify the number of cycles IORD* or IOWR* are asserted in an I/O or DMA access. The Time Out Enable (TOEn) field chooses between inserting 32 clock cycles between arbitration cycles or not; normally, enabling this bit results in better system performance.

Address: 1d00000a0

Bits	Field name	Function	Initial Value
0-3	DevTime0	8-bit I/O channel 0 (IOCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
4	DmaEn0	DMA enable 8-bit channel 0. 0 - DMA disable 1 - DMA enable	0x0
5	DmaR/W0	DMA Read or Write 8-bit channel 0. 0 - DMA write 1 - DMA read	0x0
6-9	DevTime1	8-bit channel 1 (IOCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
10	DmaEn1	DMA enable 8-bit channel 1. 0 - DMA disable 1 - DMA enable	0x0
11	DmaR/W1	DMA Read or Write 8-bit channel 1. 0 - DMA write 1 - DMA read	0x0
12-15	CenTime	Centronics external register access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
16	DmaEnCen	Centronics DMA enable. 0 - DMA disable 1 - DMA enable	0x0

Bits	Field name	Function	Initial Value
17	DmaR/WCen	DMA Read or Write for the Centronics interface. 0 - DMA write 1 - DMA read	
18-21	DevTime3	16-bit I/O channel 0 (IOGPCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
22-25	DevTime4	16-bit I/O channel 1 (IOGPCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
26	BigEndian0	Big or Little Endian for the 16-bit I/O channel 0 0 - Big Endian 1 - Little Endian	0x0
27	BigEndian1	Big or Little Endian for the 16-bit I/O channel 1 0 - Big Endian 1 - Little Endian	0x0
28	TOEn	Time Out Enable for both DMA channels 0 - Time out disabled, time out is 0 clocks 1 - Time out enabled, time out is 32 clocks	0x0

3.20 Centronics Status

This register is used to implement the Centronics hand-shake protocol via software by the CPU.

Address: 1d000100

Bits	Field name	Function	Initial Value
0	Busy	Printer busy indication 0 - Ready 1 - Busy	0x0
1	Ack	Printer acknowledge 0 - acknowledge 1 - Normal	
2	Fault	Fault indication 0 - Fault 1 - Normal	

Bits	Field name	Function	Initial Value
3	Select	Select 0 - Off line 1- On line	
4	Perror	Paper Error indication 0 - No error 1- Error	

3.21 Centronics Control

This register is used to set the Centronics transfer mode per the IEEE 1284 specification Rev. 2

Address: 1d000104

Bits	Field name	Function	Initial Value
0-2	Mode	IEEE 1284 modes 000 - Compatible 001 - Nibble 010 - Byte 011 - ECP 100 - EPP 101 - CPU control 110 - extensibility link 111 - termination	0x0
3	NegRep	Negotiation Reply All modes except nibble mode, but including nibble mode Device ID: 0 - mode requested by host is not supported by the peripheral (eg. printer) 1- mode requested is supported Nibble mode: 0- mode requested by host is supported by the peripheral (eg. printer) 1- mode requested is not supported	0x0

3.22 Centronics Nibble Data

This register is used to post the data to be transferred in nibble mode.

Address: 1d000108

Bits	Field name	Function	Initial Value
0-7	NibData	Nibble mode Centronics data to be sent to the host	

3.23 Centronics Host

This register is used to read inputs from the host in the Centronics protocol pins.

Address: 1d00010c

Bits	Field name	Function (In compatible mode)	Initial Value
0	Strobe	Set LOW by the host to transfer data	
1	SelectIn	Set LOW by host to select printer	
2	Init	Pulsed LOW with SelectIn active LOW to reset the Centronics interface	
3	AutoFd	Set LOW by the host to put the printer in auto-feed mode.	

3.24 Centronics Mode

This register is used to set the Centronics DMA parameters and select the protocol options in Compatible mode.

Address: 1d000110

Bits	Field name	Function	Initial Value
0-1	Application	See IEEE 1284 standard for details 00 - Standard 01 - IBM Epson 10 - Reserved 11 - Classic	
2	DmaEn	0 - transmission executed by CPU 1 - transmission executed by DMA	
3	DmaDir	0 - DMA write 1 - DMA reads	

3.25 Centronics Minimum Delay

This register contains the values that are needed for each operating frequency to comply with the IEEE 1284 standard (minimum of 500ns and 2500ns). However for systems with higher performance requirements, it is possible to program the minimum delays for lower values.

Address:1d000114

Bits	Field name	Function	Initial Value
0-6	2500ns	16Mhz - 0x28	
		20Mhz - 0x32	
		25Mhz - 0x3f	
		33Mhz - 0x53	
7-13	500ns	16Mhz - 0x08	
		20Mhz - 0x0a	
		25Mhz - 0x0d	
		33Mhz - 0x11	

3.26 Centronics Data Detect 0

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued.

Address: 1d0000a4

Bits	Field name	Function	Initial Value
0-7	DataDet0	Data to be used for comparison with the incoming data.	

3.27 Centronics Data Detect 1

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued.

Address: 1d0000a8

Bits	Field name	Function	Initial Value
0-7	DataDet1	Data to be used for comparison with the incoming data.	

3.28 Centronics Data Detect 2

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued.

Address: 1d0000ac

Bits	Field name	Function	Initial Value
0-7	DataDet2	Data to be used for comparison with the incoming data.	

4 EXTERNAL ADDRESS SPACE

The address space allocated to the different resources in the system is shown in Table 1. Bits 29-31 are not decoded so that physical aliases of 512 Mbyte are created. This enables the software to access the same system resource using different attributes (i.e cached space vs. uncached space, kernel vs. user).

Description	Size	Address range
DRAM	40M	0x00000000: 0x027fffff
ROM_CS2	4M	0x1fc00000: 0x1fffffff
ROM_CS1	8M	0x1f400000: 0x1fbfffff
ROM_CS0	8M	0x1ec00000: 0x1f3fffff
IO channel 0	16M	0x08000000: 0x08ffffff
IO channel 1	16M	0x09000000: 0x09ffffff
IO channel 2	16M	0x0b000000: 0x0bffffff
IO channel 3	256M	0x0c000000: 0x1bffffff
Centronics External register	1M	0x0a000000: 0x0a0fffff
Parallel Port	1M	0x0a800000: 0x0a8fffff
Coprocessor address space	16M	0x1c000000: 0x1cffffff
Internal registers	16M	0x1d000000: 0x1dffffff

Note: The table specifies maximum range.

5 PINOUT TABLE

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	AD(14)	41	EAS*	81	IOBE(1)*	121	RAS(0)*
2	AD(13)	42	ECS*	82	IOBE(0)*	122	RAS(1)*
3	AD(12)	43	EAACK*	83	IOGPCS(1)*	123	RAS(2)*
4	AD(11)	44	PIO(0)	84	IOGPCS(0)*	124	CAS(0)*
5	AD(10)	45	PIO(1)	85	IOCS(1)*	125	CAS(1)*
6	VDD	46	PIO(2)	86	IOCS(0)*	126	CAS(2)*
7	VSS	47	PIO(3)	87	DMAREQ(0)	127	CAS(3)*
8	AD(9)	48	PIO(4)	88	DMAREQ(1)	128	DWR*
9	AD(8)	49	PIO(5)	89	IODATA(15)	129	ROMCS(2)*
10	AD(7)	50	CSELECTIN*	90	IODATA(14)	130	VDD
11	AD(6)	51	CINIT*	91	IODATA(13)	131	VSS
12	AD(5)	52	CSTROBE*	92	IODATA(12)	132	ROMCS(1)*
13	AD(4)	53	CRSTROBE	93	IODATA(11)	133	ROMCS(0)*
14	AD(3)	54	CBUSY	94	IODATA(10)	134	ROMOE*
15	AD(2)	55	VDD	95	IODATA(9)	135	VCC
16	AD(1)	56	SYSCLK	96	IODATA(8)	136	VCC
17	AD(0)	57	VSS	97	IODATA(7)	137	VCC
18	VDD	58	CWSTROBE	98	IODATA(6)	138	N.C.
19	VSS	59	CROE*	99	IODATA(5)	139	AD(31)
20	VSS	60	VDD	100	IODATA(4)	140	AD(30)
21	BURST*	61	CAUTOFD*	101	VDD	141	AD(29)
22	ADDR(3)	62	CPERROR	102	VDD	142	AD(28)
23	ADDR(2)	63	CSELECT	103	VSS	143	VSS
24	ALE	64	CWOE*	104	IODATA(3)	144	AD(27)
25	RD*	65	CACK*	105	IODATA(2)	145	AD(26)
26	WR*	66	CFAULT*	106	IODATA(1)	146	AD(25)
27	DATAEN*	67	POE*	107	IODATA(0)	147	AD(24)
28	BUSGNT*	68	PSTROBE*	108	DADR(10)	148	AD(23)
29	RESET*	69	N.C.	109	DADR(9)	149	AD(22)
30	ACK*	70	N.C.	110	DADR(8)	150	VDD
31	RDCEN*	71	N.C.	111	DADR(7)	151	VSS
32	BUSREQ*	72	N.C.	112	VDD	152	AD(21)
33	INT*	73	VDD	113	VSS	153	AD(20)
34	EADOE*	74	VSS	114	DADR(6)	154	AD(19)
35	EADDIR*	75	IOWAIT*	115	DADR(5)	155	AD(18)
36	EATOE*	76	DMAACK*(1)*	116	DADR(4)	156	AD(17)
37	EDTACK*	77	DMAACK*(0)*	117	DADR(3)	157	AD(16)
38	EDS*	78	IOWR*	118	DADR(2)	158	AD(15)
39	EBREQ*	79	IORD*	119	DADR(1)	159	OEMAD*
40	EBGNT*	80	IOA1	120	DADR(0)	160	TEST

6 AC TIMING CHARACTERISTICS

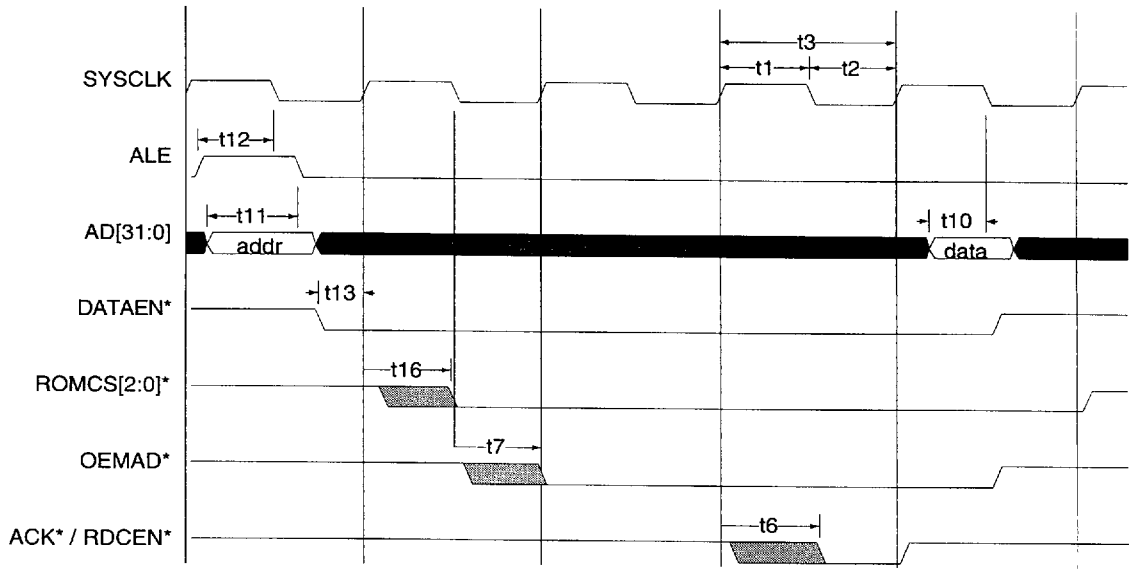
(TC= 0-70°C; VDD= +5V, +/- 5%)))

Symbol	Signals	Description	Min	Max	Unit
t1	SYSCLK	Pulse Width High	12		ns
t2	SYSCLK	Pulse Width Low	12		ns
t3	SYSCLK	Clock period	30		ns
t4	RESET*	Pulse Width from VDD Valid	200		us
t5	RESET*	Minimum Pulse Width	40		VCLKIN
t6	BUSREQ*, ACK*, RDCEN*	Valid from SYSCLK rising	2	17	ns
t7	A/D[31:0], OEMAD*, EADOE*	Valid from SYSCLK falling	2	15	ns
t8	A/D[31:0], ADDR[3:2], WR*, PIO[5:0], EAS*, EDS*, EDTACK*	Driven from SYSCLK rising	0	20	ns
t9	A/D[31:0]	Tri-state from SYSCLK rising	0	15	ns
t10	A/D[31:0]	Set-up to SYSCLK falling	6		ns
t11	A/D[31:0]	Set-up to ALE falling	7		ns
t12	ALE	Set-up to SYSCLK falling	7		ns
t13	BURST*, RD*, DATAEN*, WR*, ADDR[3:2], BUS-GNT*	Set-up to SYSCLK rising	10		ns
t14	ALE, BURST*, RD*, DATAEN*, INT*, PIO[5:0], IODATA[15:0], EAS*, EDS*, EDTACK*	Tri-state from SYSCLK rising	0	20	ns
t15	ALE, BURST*, RD*, DATAEN*, PIO[5:0]	Driven from SYSCLK rising	0	20	ns
t16	ALE, BURST*, RD*, DATAEN*, IOGPCS*, ROMCS*[2:0], IORD*, IOWR*, ROMOE*, IOA1, IOBE*[1:0], INT*, DMAACK*[1:0], PIO[5:0], ADDR[3:2], WR*, EAS*, EDS*, EDTACK*, ECS*, EBGNT*, EAACK*	Valid from SYSCLK rising	3	15	ns
t17	ADDR[3:2], WR*	Tri-state from SYSCLK rising	2	20	ns
t18	DADR[10:0]	Valid from AD address valid	6	25	ns
t19	DADR[10:0]	Valid from SYSCLK rising	3	27	ns
t20	RAS*[2:0], DWR*	Valid from SYSCLK rising	2	17	ns

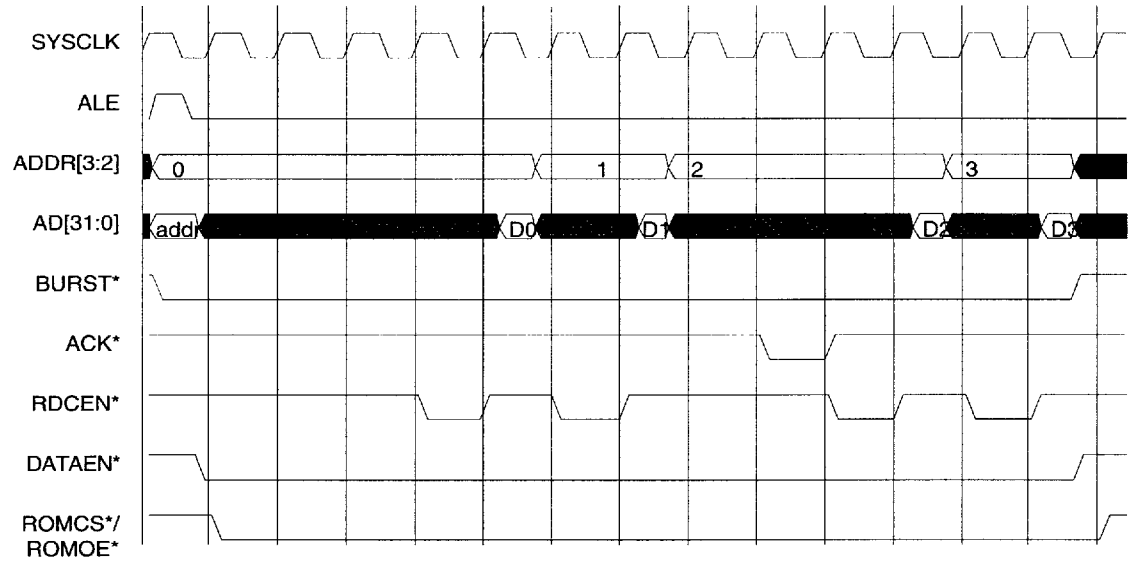
Symbol	Signals	Description	Min	Max	Unit
t21	CAS*[3:0]	SYSCLK rising to CAS* LOW	2	13	ns
t22	CAS*[3:0]	SYSCLK falling to CAS* HIGH	2	13	ns
t23	IODATA[15:0]	Hold from IOWR* rising	15		ns
t24	IODATA[15:0]	Set-up to SYSCLK rising	9		ns
t25	IODATA[15:0]	Driven from SYSCLK rising	0	15	ns
t26	IOWAIT*	Set-up to SYSCLK rising	18		ns
t27	DMAREQ*[1:0], PIO[5:0],	Asynchronous Inputs			
t31	TEST, EBREQ*	Setup to SYSCLK rising	8		ns
t32	EAS*, EDS*, EDTACK*	Setup to SYSCLK rising	13		ns
t33	EADDIR*, EATOE*	Valid from SYSCLK rising	2	20	ns

NOTES:

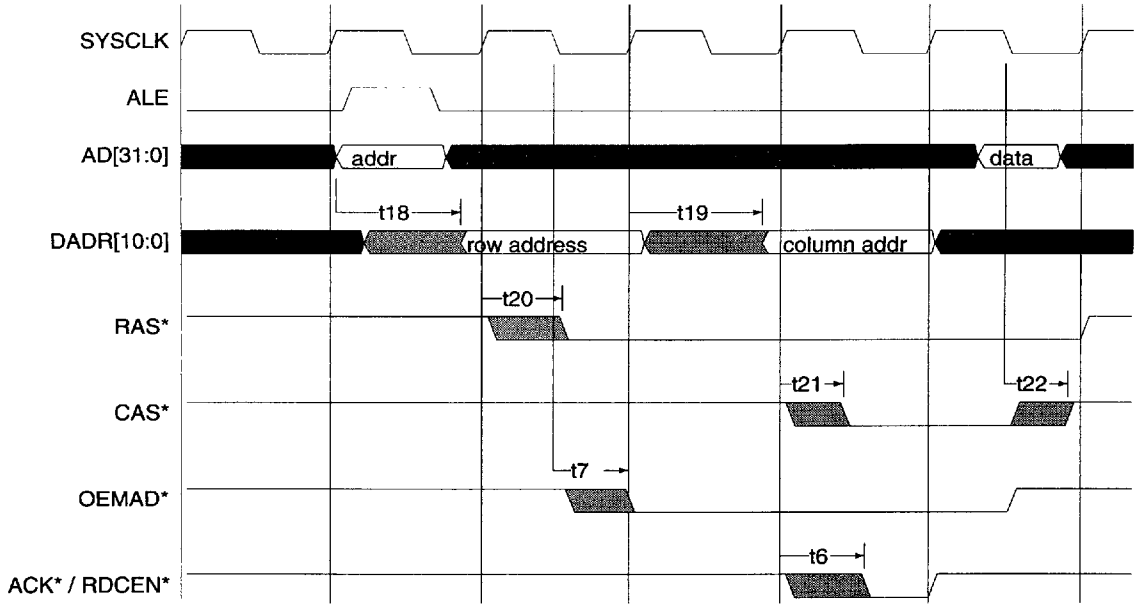
(a) Internal VCLK frequency (divided or not) should be lower than 75% of SYSCLK frequency; Valid only in the SYSCLK during which IODATA is sampled.



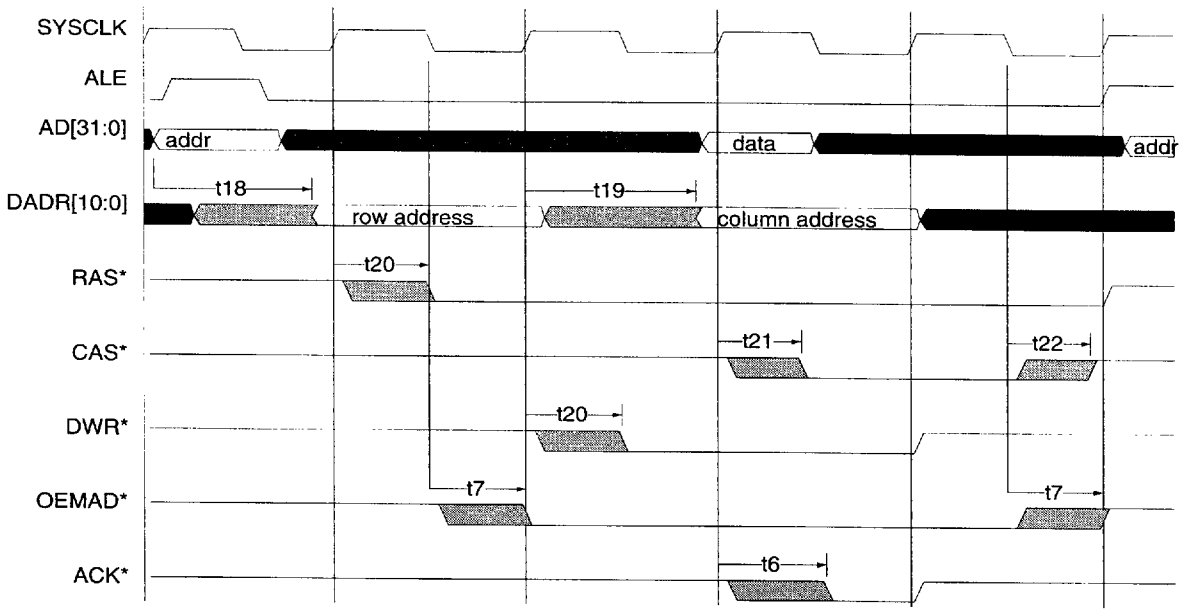
ROM Read



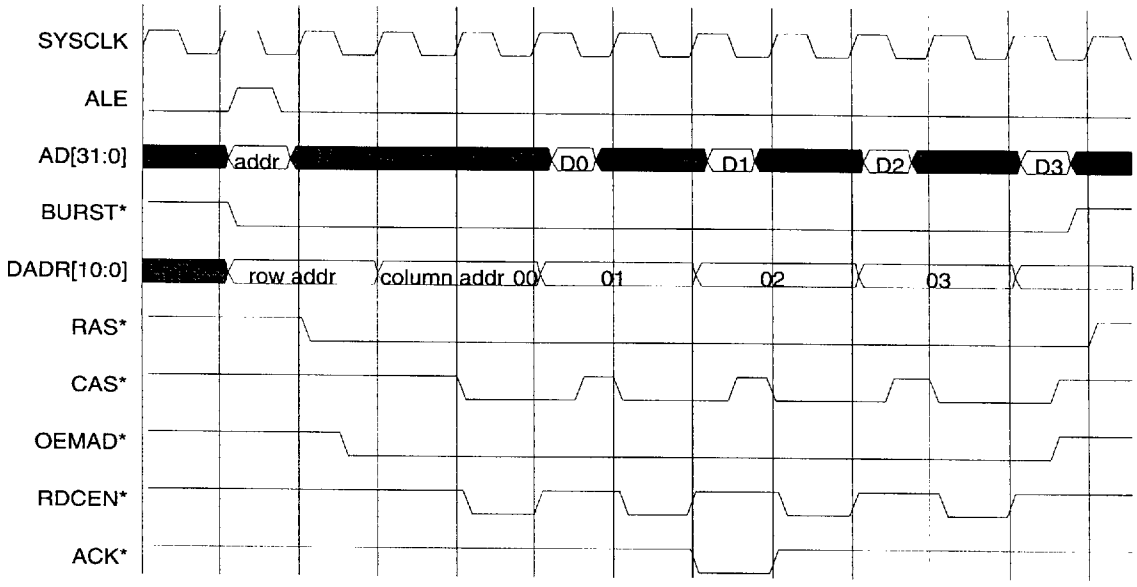
Interleaved ROM Burst Read



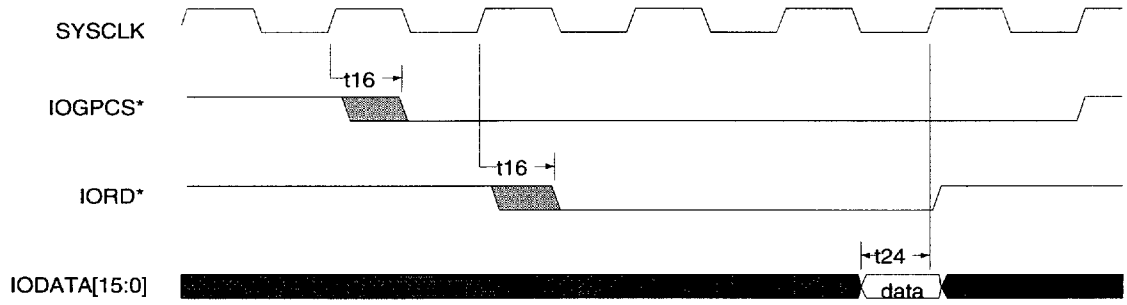
DRAM Read



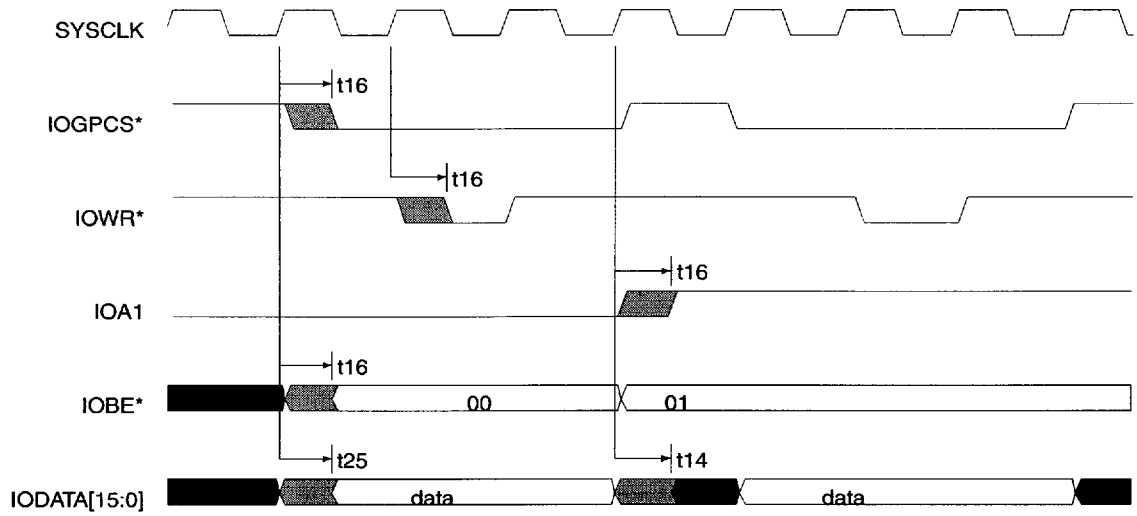
DRAM Write



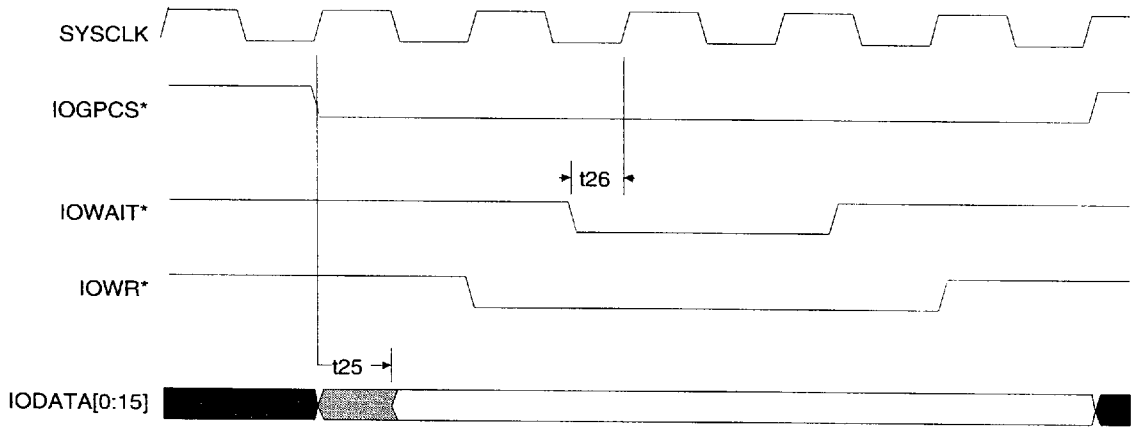
DRAM Burst Read



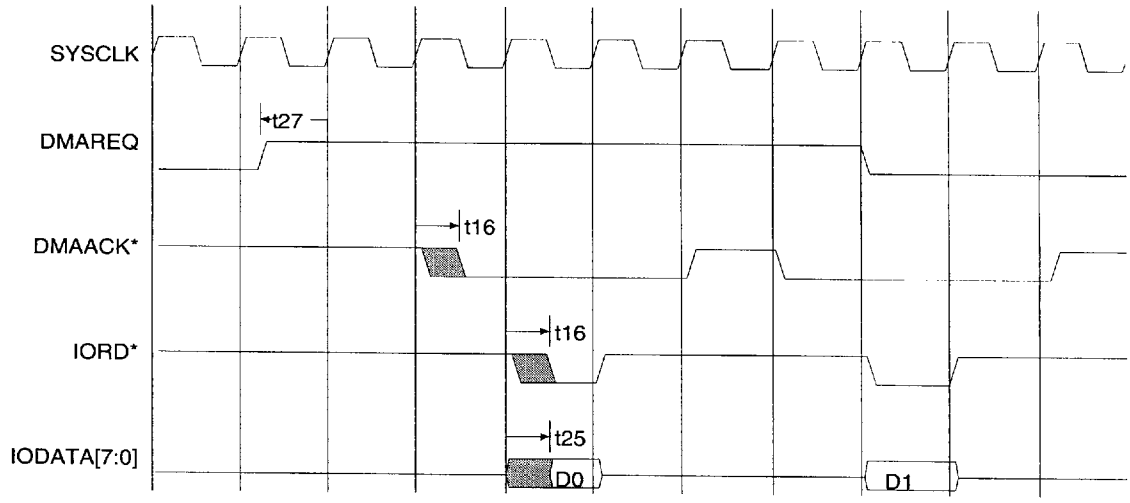
I/O Read



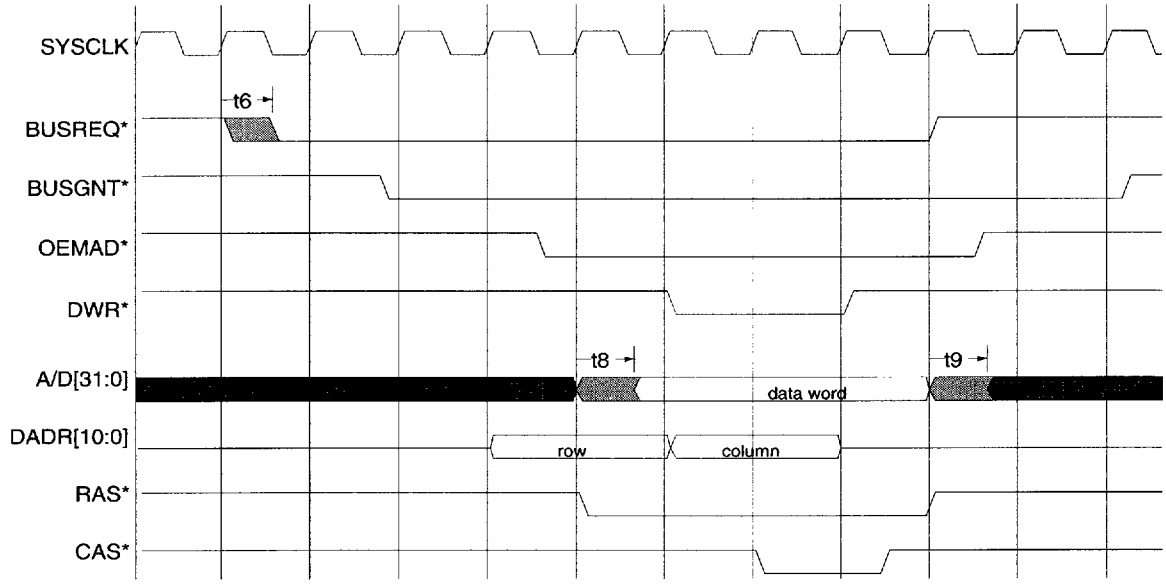
I/O Write 24-Bit



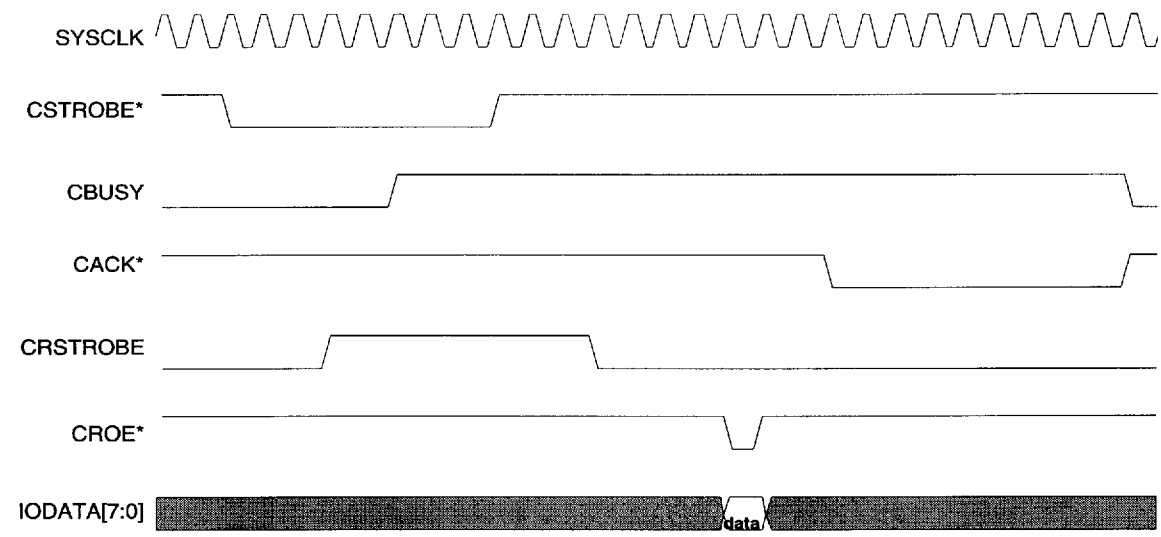
I/O Write (With Wait State)



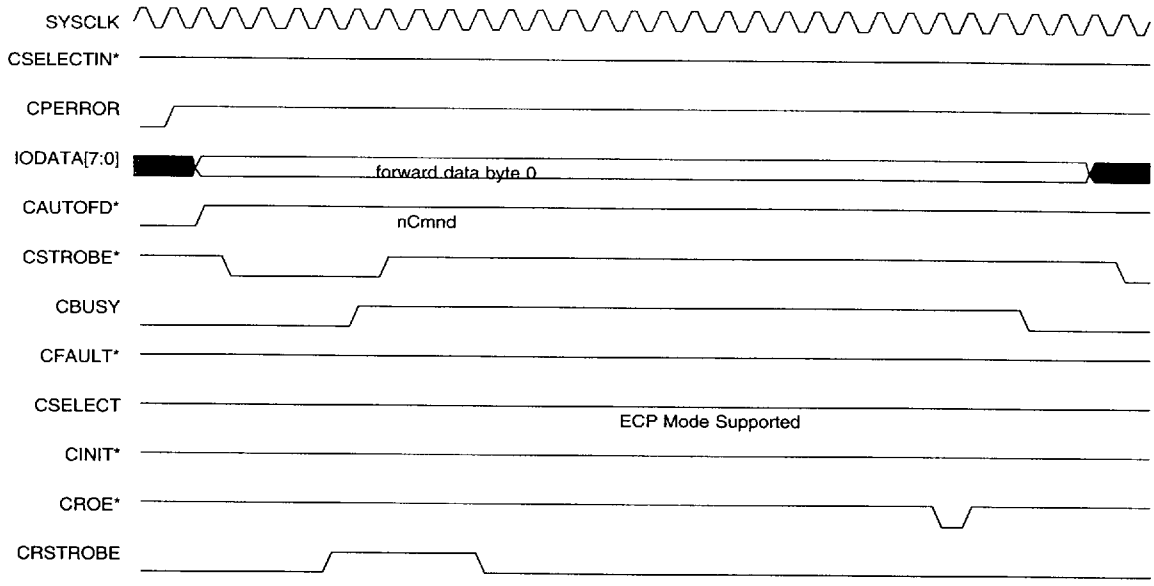
I/O Bus DMA Read



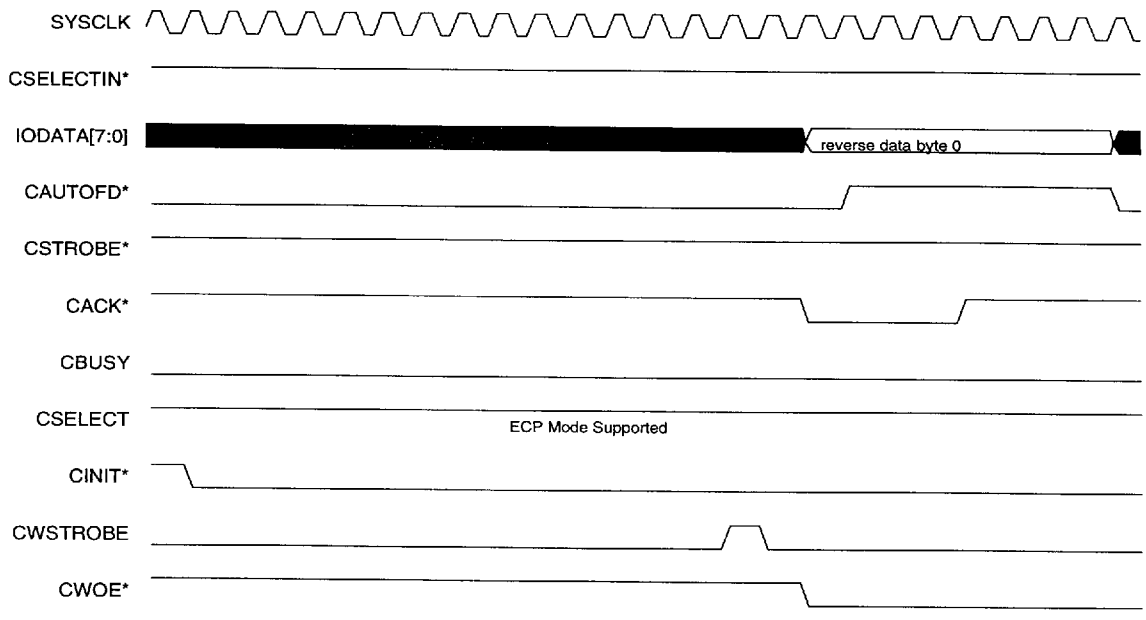
A/D Bus DMA Write



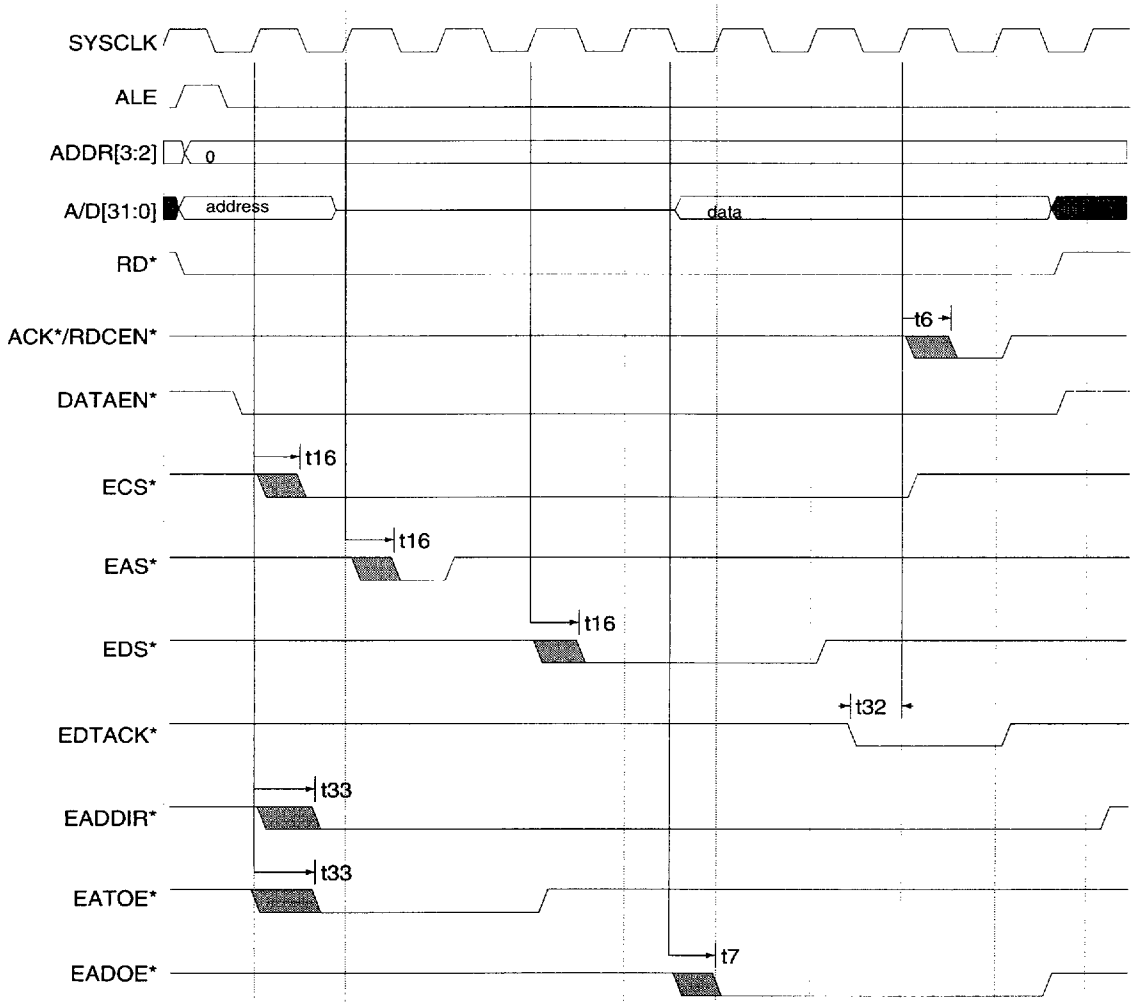
Centronics Compatible Mode (Standard)



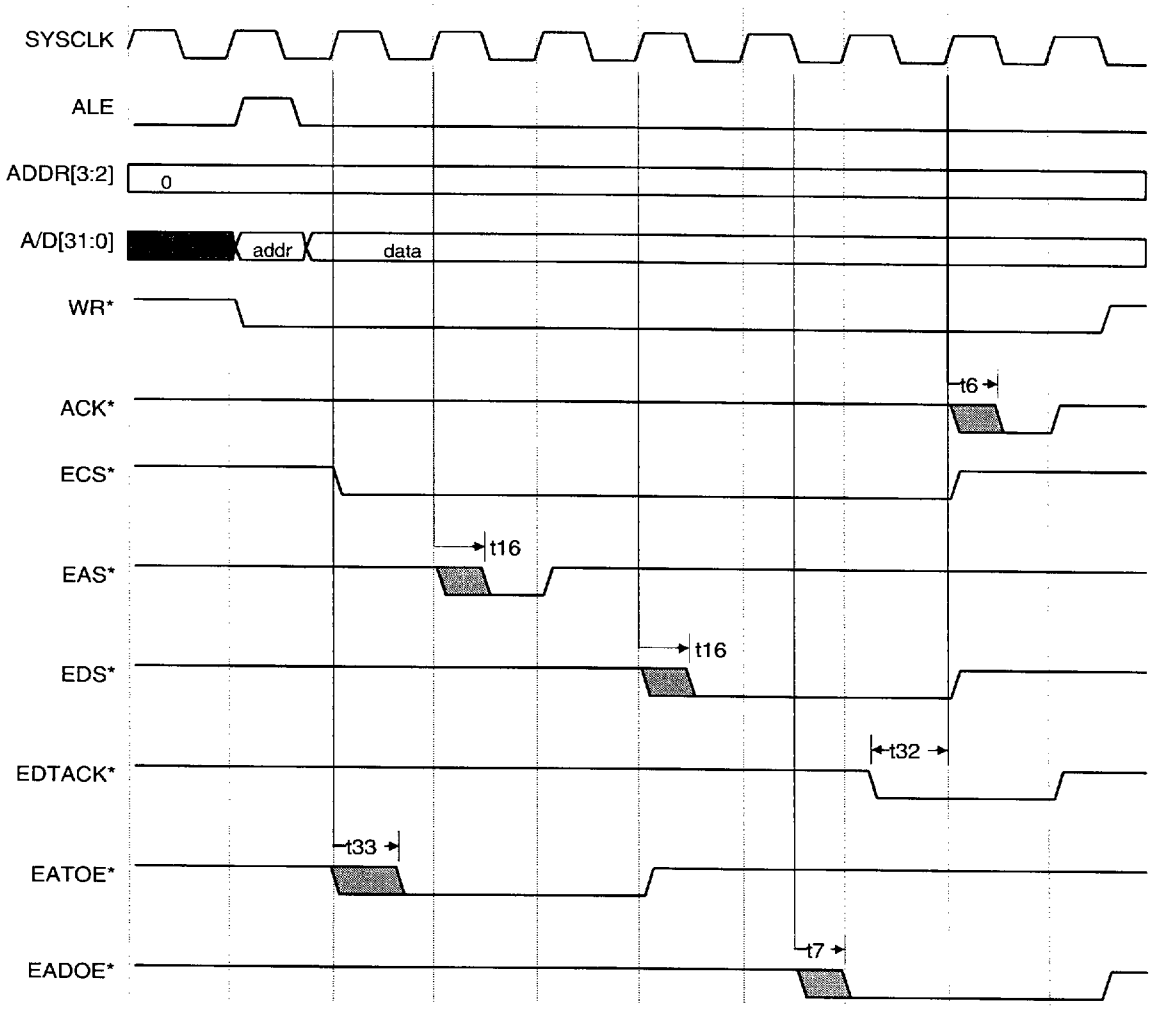
ECP Forward Transfer



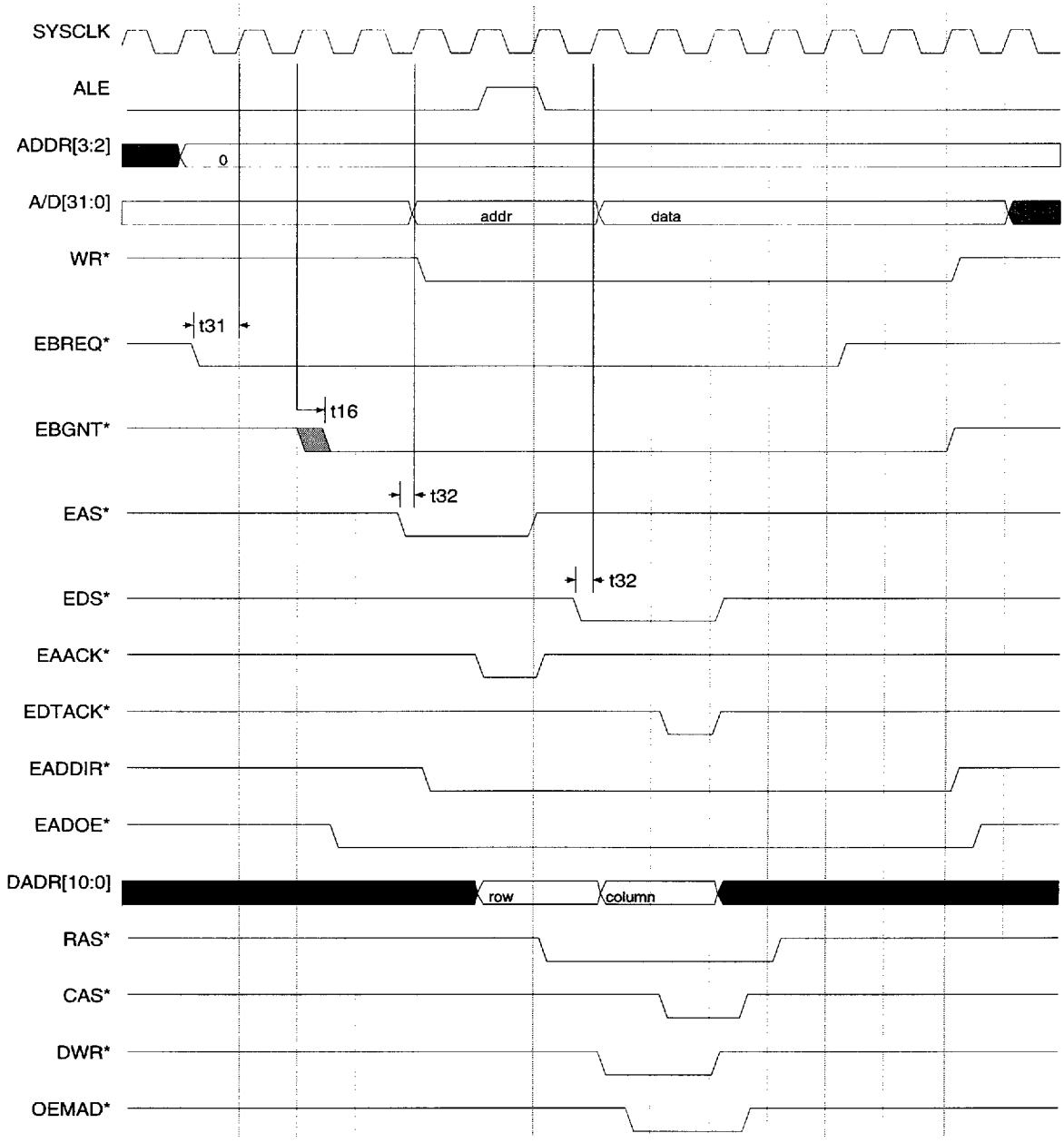
ECP Reverse Transfer



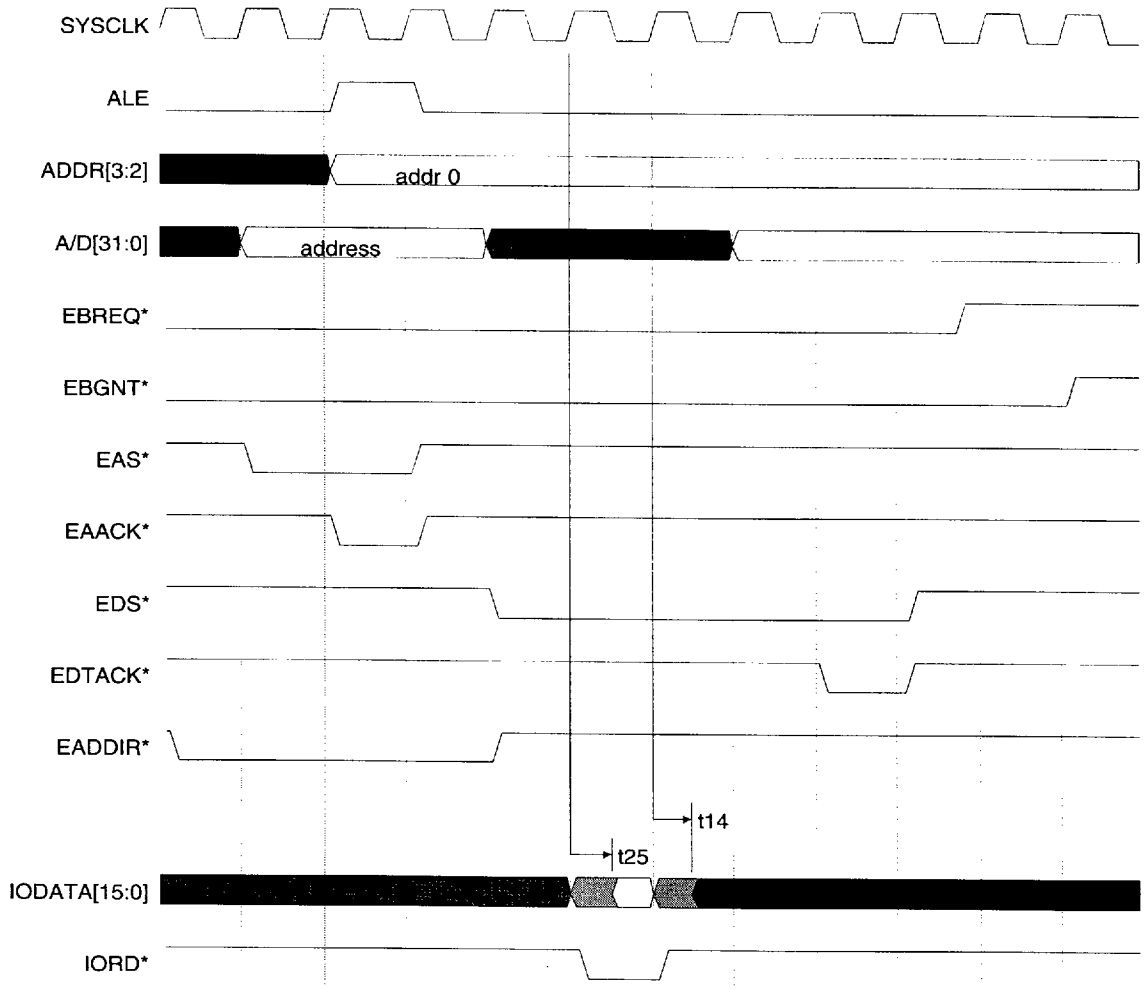
External Agent/Coprocessor Slave Read



External Agent/CoprocessorSlave Write



External Agent/Coprocessor Master DRAM Read



External Agent/Coprocessor Master I/O Read

8 DC ELECTRICAL SPECIFICATIONS

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+ 0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		200	mA	VDD = 5V, Ta=25C
CINCLK	CLK Input Capacitance		11	pF	
CIN	Input Capacitance		5	pF	

9 APPLICATIONS

9.1 Full Implementation

A possible implementation of a fully featured system is shown in Figure 9.1. This system includes a 2-way interleaved ROM array, and uses external multiplexers (FCT257x8) that are controlled by MUX_ADDR[2] to choose one bank or the other. The GT-32011 directly provides the output enable signal to these multiplexers (ROMOE*), as well as the chip select signal to the ROM banks (ROMCS[2:0]*).

The control to the DRAM banks is provided directly by signals coming out of the GT-32011. These signals can directly control up to 3 banks of DRAM and 40Mbytes.

This implementation supports an external agent or coprocessor and thus an extra set of latches and transceivers are used to accommodate it. All control signals necessary to provide DMA master and slave operations to the coprocessor are provided. Multiplexing between the coprocessor and CPU is done via BUSGNT*.

The GT-32011 also generates the control signals necessary to transfer parallel byte or word data to and from the a parallel interface (POE* and PSTROBE*).

A full complement of signals is provided by the GT-32011 to implement an IEEE1284 bi-directional Centronics interface.

The 80186-style I/O bus interfaces to a connector that can be used to expand features by adding standard industry peripherals like SCSI, PCMCIA cards, UARTs, Ethernet, etc.

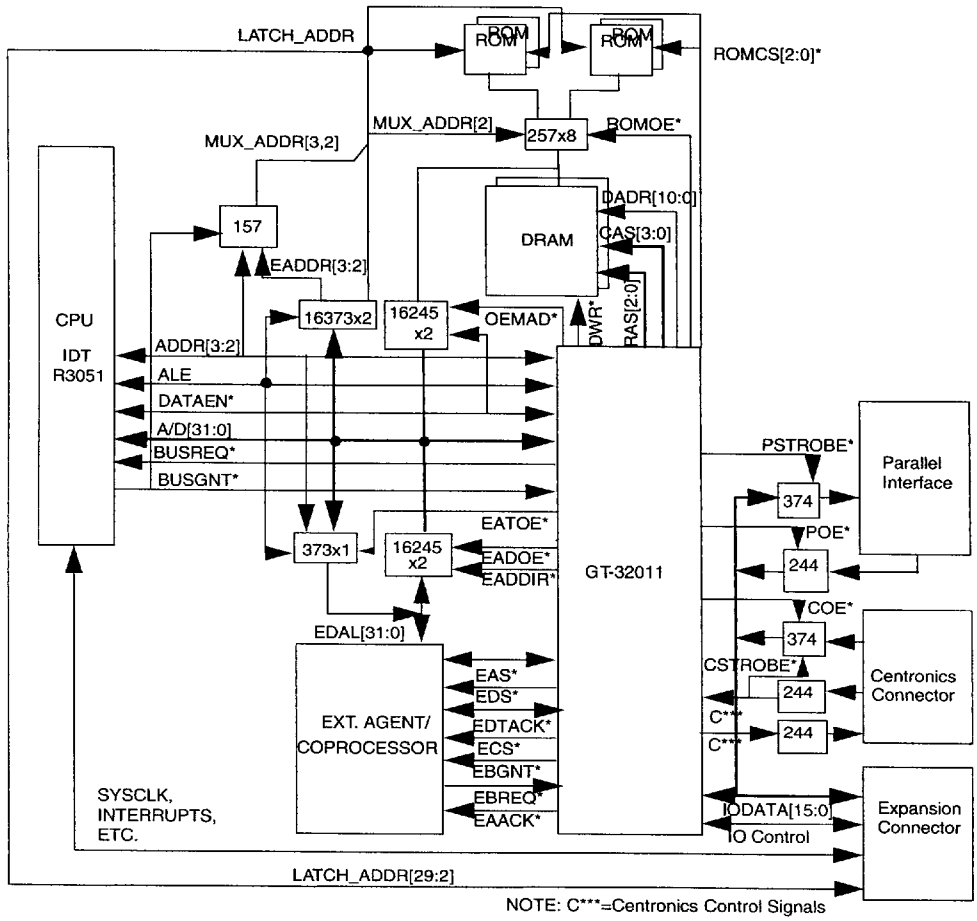


Figure 9.1 Full Implementation With Interleaved ROM

9.2 Minimal Implementatio n

Figure 9.2 shows a minimal implementation. In this case, we show the lower end CPU in the R3051 Family, the R3041. A simple non-interleaved ROM subsystem is used in this case, with only 1 bank - the boot bank ROMCS[2]*.

The DRAM system contains only 1 bank and as we mentioned before, the GT-32011 directly provides all the necessary signals.

Since a coprocessor is not used in this case, the interface to the AD bus is very simple.

The balance of features shown is the same, but they could conceivably include simpler implementations of each, like less peripherals via the IODATA bus, or lower performance peripherals.

Both the full and the minimal implementations shown demonstrate the flexibility of the GT-32011 as a common block that enables modular designs or designs that can be upgraded in the field.

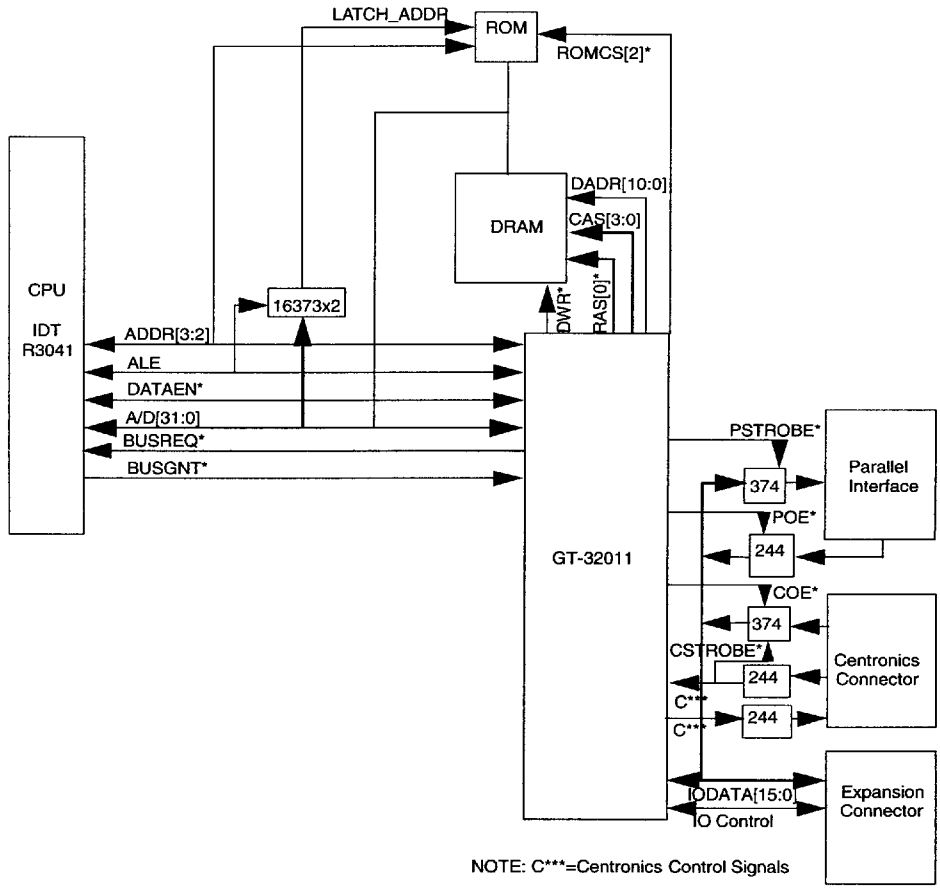
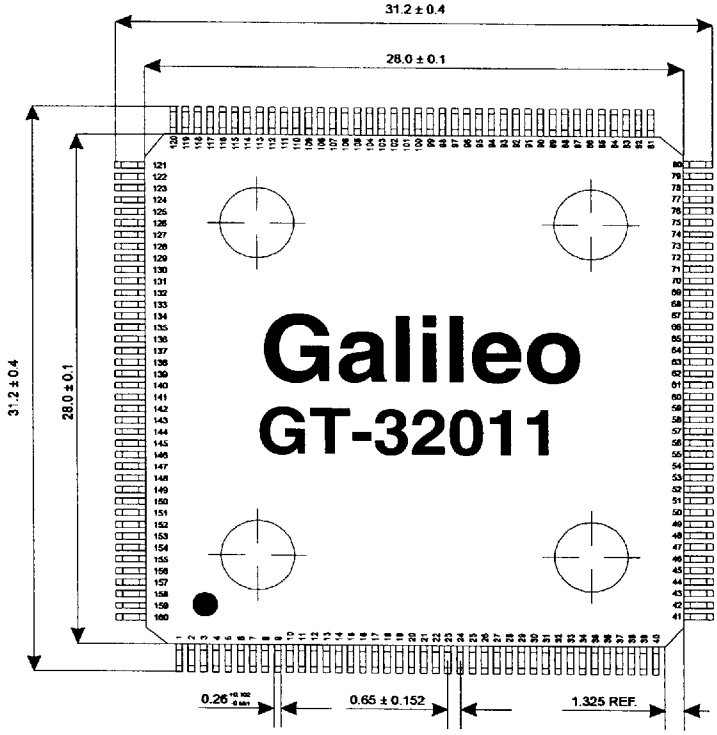


Figure 9.2 Minimal Implementation

10 PACKAGE

10.1 160-Pin Quad Flat Package (QFP, EIAJ)



10.2 160 - Pin Quad Flat Package Expanded View (QFP, EIAJ)

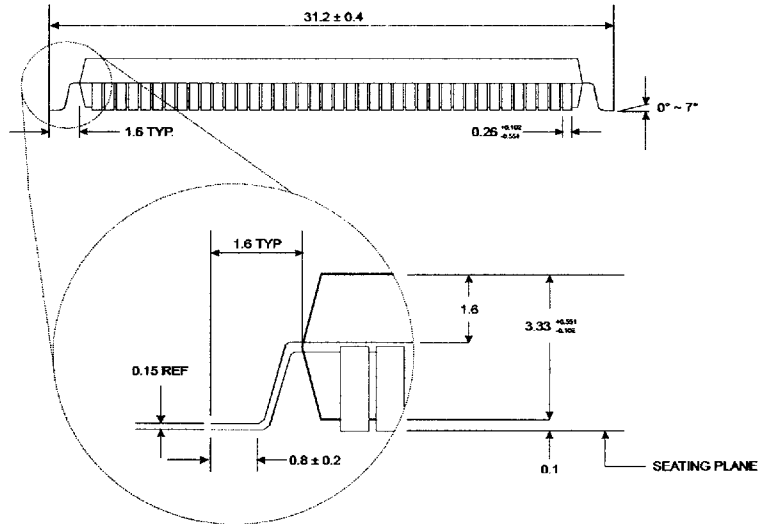


Fig. 10.2 : Expanded View

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