MOTOROLA

MC3486

Quad EIA-422/423 Line Receiver

QUAD EIA–422/3 LINE RECEIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

Motorola's Quad EIA–422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three–state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three–State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 30 mV (Typical) @ Zero Volts Common Mode
- Fast Propagation Times – 25 ns (Typical)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source

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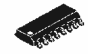
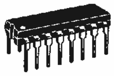


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



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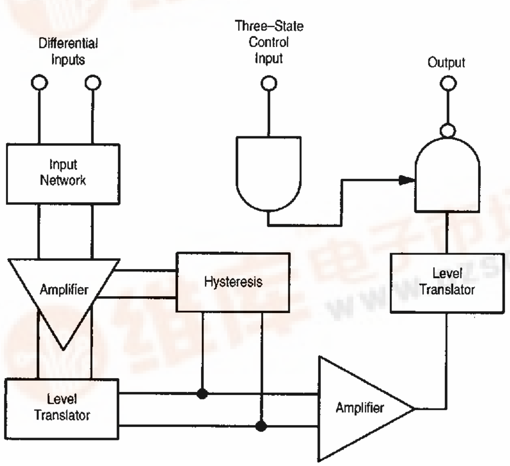
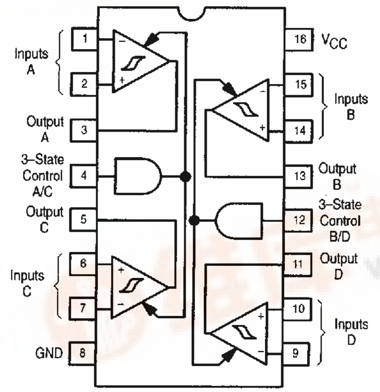
CASE 648

Receiver Chain Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3486P	T_A = 0 to +70°C	Plastic DIP
MC3486D		SO–16

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	± 15	Vdc
Input Differential Voltage	V_{ID}	± 25	Vdc
Three–State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	–7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IK} = 0 V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (Three–State Control)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (Three–State Control)	V_{IL}	–	–	0.8	V
Differential Input Threshold Voltage, Note 2 (– 7.0 V $\leqslant V_{IC} \leqslant$ 7.0 V, V_{IH} = 2.0 V) (I_O = – 0.4 mA, $V_{OH} \geqslant$ 2.7 V) (I_O = 8.0 mA, $V_{OL} \geqslant$ 0.5 V)	$V_{TH(D)}$	 – –	 – –	 0.2 – 0.2	V
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at 0 V) (V_I = – 10 V) (V_I = – 3.0 V) (V_I = + 3.0 V) (V_I = + 10 V)	$I_{IB(D)}$	 – – – –	 – – – –	 – 3.25 – 1.50 + 1.50 + 3.25	mA
Input Balance and Output Level (– 7.0 V $\leqslant V_{IC} \leqslant$ 7.0 V, V_{IH} = 2.0 V, Note 3) (I_O = – 0.4 mA, V_{ID} = 0.4 V) (I_O = 8.0 mA, V_{ID} = – 0.4 V)	 V_{OH} V_{OL}	 2.7 –	 – –	 – 0.5	V
Output Third State Leakage Current ($V_{I(D)}$ = + 3.0 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V) ($V_{I(D)}$ = – 3.0 V, V_{IL} = 0.8 V, V_{OH} = 2.7 V)	I_{OZ}	 – –	 – –	 – 40 40	µA
Output Short–Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, Note 4)	I_{OS}	– 15	–	– 100	mA
Input Current – Low Logic State (Three–State Control) (V_{IL} = 0.5 V)	I_{IL}	–	–	– 100	µA
Input Current – High Logic State (Three–State Control) (V_{IH} = 2.7 V) (V_{IH} = 5.25 V)	I_{IH}	 – –	 – –	 20 100	µA
Input Clamp Diode Voltage (Three–State Control) (I_{IK} = – 10 mA)	V_{IK}	–	–	– 1.5	V
Power Supply Current (V_{IL} = 2.0 V)	I_{CC}	–	–	85	mA

NOTES: 1. All currents into device pins are shown as positive, out of device pins are negative. All voltage referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA–422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

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SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	35	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay time – Three–State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

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Figure 1. Switching Test Circuit and Waveforms

Propagation Delay Differential Input to Output

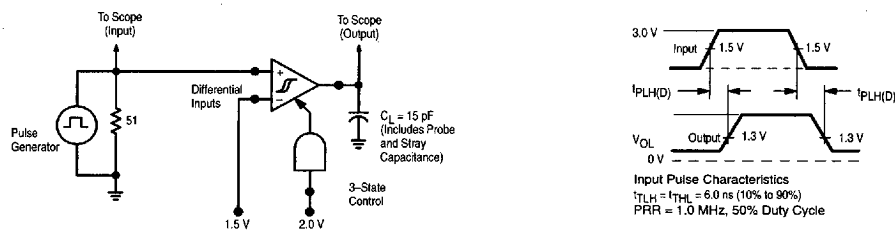
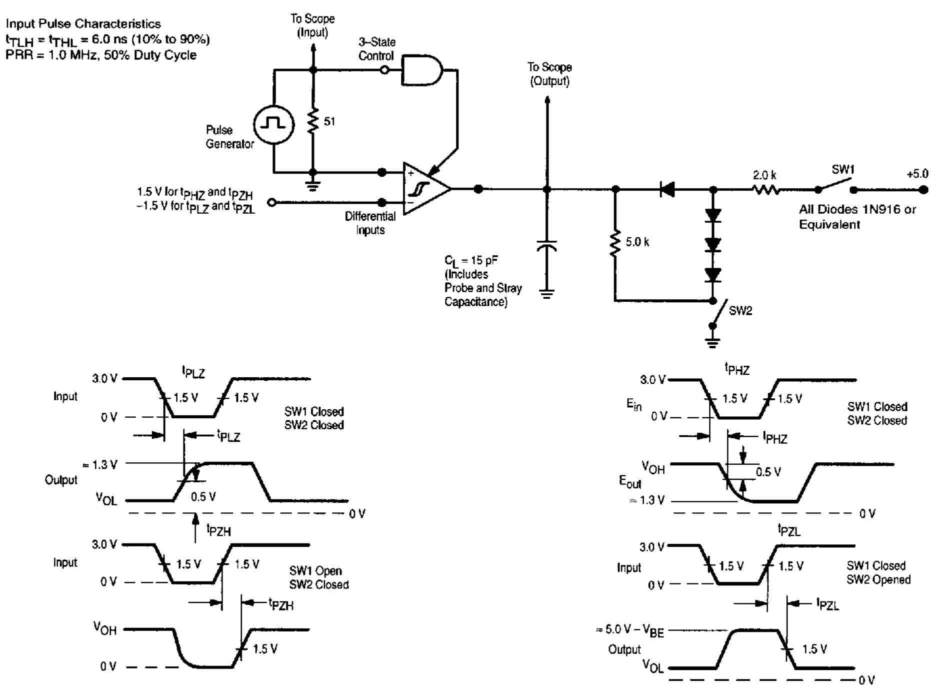


Figure 2. Propagation Delay Three–State Control Input to Output



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