TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS181

November 1997

CD74HC367, CD74HCT367, CD74HC368, CD74HCT368

High Speed CMOS Logic Hex Buffer/Line Driver, Three-State Non-Inverting and Inverting

Features

- **Buffered Inputs**

- **High Current Bus Driver Outputs**

- **Two Independent Three-State Enable Controls**

- **Typical Propagation Delay t_{PLH}, t_{PHL} = 8ns at V_{CC} = 5V, C_L = 15pF, T_A = 25°C**

- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**

- **Wide Operating Temperature Range . . . -55°C to 125°C**

- **Balanced Propagation Delay and Transition Times**

- **Significant Power Reduction Compared to LSTTL Logic ICs**

- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**

- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

The Harris CD74HC367, CD74HCT367, CD74HC368, and CD74HCT368 silicon gate CMOS three-state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The CD74HC367 and CD74HCT367 are non-inverting buffers, whereas the CD74HC368 and CD74HCT368 are inverting buffers. These devices have two output enables, one enable (OE1) controls 4 gates and the other (OE2) controls the remaining 2 gates.

The CD74HCT367 and CD74HCT368 logic families are speed, function and pin compatible with the standard 74LS logic family.
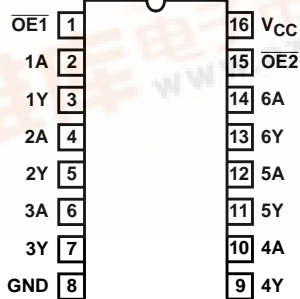
Ordering Information

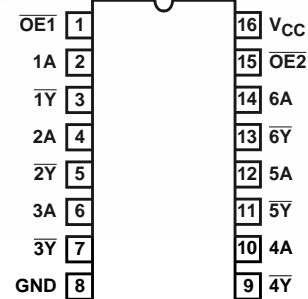| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74HC367E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT367E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT368E	-55 to 125	16 Ld PDIP	E16.3
CD74HC367M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT367M	-55 to 125	16 Ld SOIC	M16.15
CD74HC368M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT368M	-55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

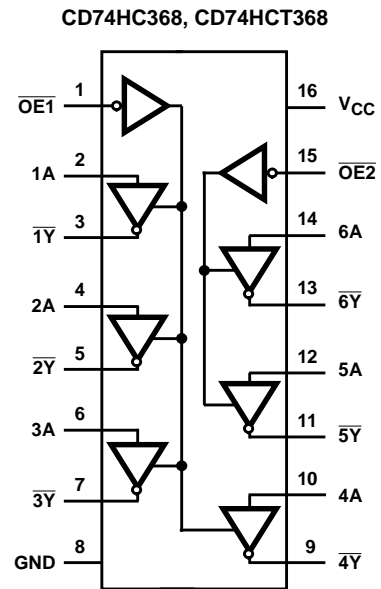## Pinouts

CD74HC367, CD74HCT367 (PDIP, SOIC)
TOP VIEW

$\overline{OE1}$	1	16 V_{CC}
1A	2	15 $\overline{OE2}$
1Y	3	14 6A
2A	4	13 6Y
2Y	5	12 5A
3A	6	11 5Y
3Y	7	10 4A
GND	8	9 4Y

CD74HC368, CD74HCT368 (PDIP, SOIC)
TOP VIEW

$\overline{OE1}$	1	16 V_{CC}
1A	2	15 $\overline{OE2}$
$\overline{1Y}$	3	14 6A
2A	4	13 $\overline{6Y}$
$\overline{2Y}$	5	12 5A
3A	6	11 $\overline{5Y}$
$\overline{3Y}$	7	10 4A
GND	8	9 $\overline{4Y}$

Functional Diagrams

CD74HC367, CD74HCT367

Pin	Signal
1	$\overline{OE1}$
2	1A
3	1Y
4	2A
5	2Y
6	3A
7	3Y
8	GND
16	V_{CC}
15	$\overline{OE2}$
14	6A
13	6Y
12	5A
11	5Y
10	4A
9	4Y

CD74HC368, CD74HCT368

Pin	Signal
1	$\overline{OE1}$
2	1A
3	$\overline{1Y}$
4	2A
5	$\overline{2Y}$
6	3A
7	$\overline{3Y}$
8	GND
16	V_{CC}
15	$\overline{OE2}$
14	6A
13	$\overline{6Y}$
12	5A
11	$\overline{5Y}$
10	4A
9	$\overline{4Y}$
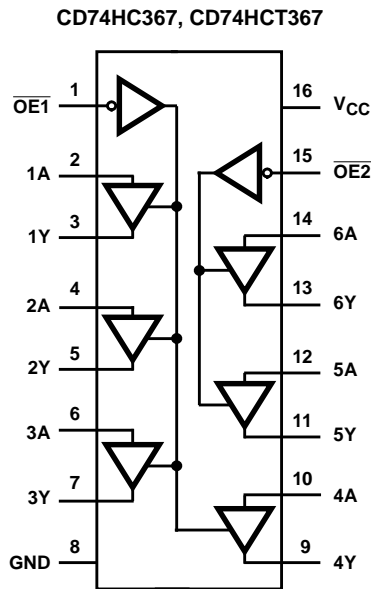
TRUTH TABLE

INPUTS		OUTPUTS (Y)	
$\overline{OE}$	A	HC/HCT367	HC/HCT368
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

NOTE:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance (OFF) State
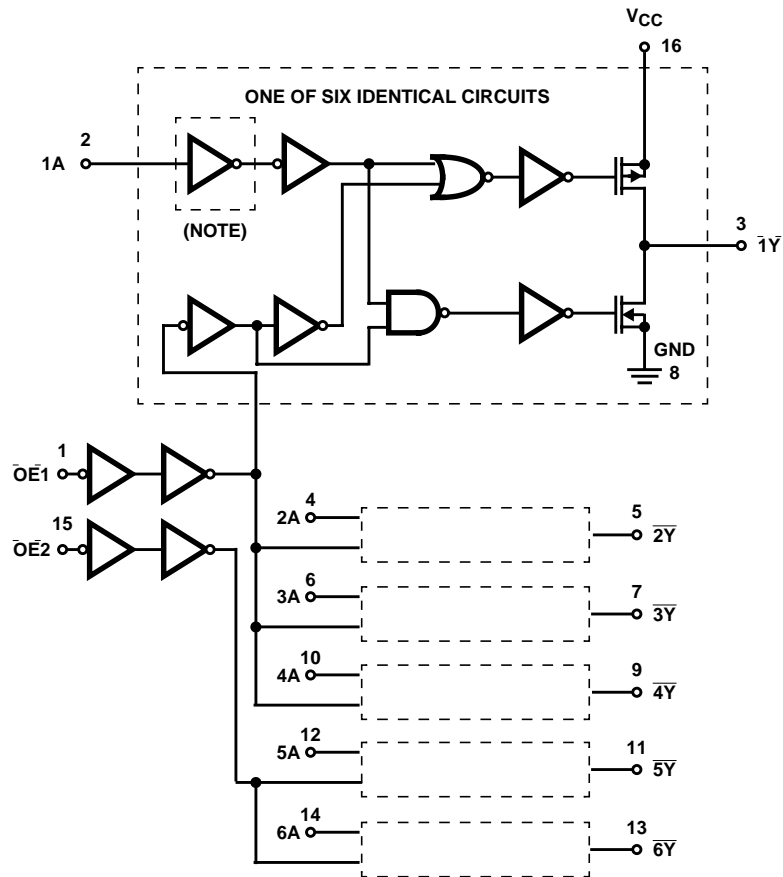
Logic Diagram

NOTE: Inverter not included in HC/HCT367.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT367 AND HC/HCT368 (OUTPUTS FOR HC/HCT367 ARE COMPLEMENTS OF THOSE SHOWN, i.e., 1Y, 2Y, ETC.)

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 7V

DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . .±20mA

DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . .±20mA

DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} + 0.5V . . . .±35mA

DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . .±25mA

DC V_{CC} or Ground Current, I_{CC} . . . .±50mA

Operating Conditions

Temperature Range, T_A . . . . -55°C to 125°C

Supply Voltage Range, V_{CC}
HC Types . . . . .2V to 6V
HCT Types . . . . .4.5V to 5.5V

DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}

Input Rise and Fall Time
2V . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . 400ns (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (^{o}C/W)
PDIP Package	90
SOIC Package	160

Maximum Junction Temperature . . . . 150°C

Maximum Storage Temperature Range . . . .-65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-6	4.5	3.98	-	-	3.84	-	3.7	-	V
			-7.8	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			6	4.5	-	-	0.26	-	0.33	-	0.4	V
			7.8	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA

DC Electrical Specifications   (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	I_O (mA)	V_{CC} (V)	25°C MIN	25°C TYP	25°C MAX	-40°C TO 85°C MIN	-40°C TO 85°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNITS
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	6	-	-	±0.5	-	±5.0	-	±10	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA
Three-State Leakage Current	I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	-	±10	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
$\overline{OE1}$	0.6
All Others	0.55

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications   Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C TYP	25°C MAX	-40°C TO 85°C MAX	-55°C TO 125°C MAX	UNITS
HC TYPES								
Propagation Delay, Data to Outputs HC/HCT367	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	105	130	160	ns
			4.5	-	21	26	32	ns
			6	-	18	24	27	ns
		C_L = 15pF	5	8	-	-	-	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C TYP	25°C MAX	-40°C TO 85°C MAX	-55°C TO 125°C MAX	UNITS
Propagation Delay, Data to Outputs HC/HCT368	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	105	130	160	ns
			4.5	-	21	26	32	ns
			6	-	18	24	27	ns
		C_L = 15pF	5	9	-	-	-	ns
Propagation Delay, Output Enable and Disable to Outputs	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
			6	-	26	33	38	ns
		C_L = 15pF	5	12	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	2	-	60	75	90	ns
			4.5	-	12	15	18	ns
			6	-	10	13	15	ns
Input Capacitance	C_I	-	-	-	10	10	10	pF
Three-State Output Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	40	-	-	-	pF
HCT TYPES								
Propagation Delay, Data to Outputs HC/HCT367	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	25	31	38	ns
		C_L = 15pF	5	9	-	-	-	ns
Propagation Delay, Data to Outputs HC/HCT368	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	30	38	45	ns
		C_L = 15pF	5	11	-	-	-	ns
Propagation Delay, Output Enable and Disable to Outputs	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	35	44	53	ns
		C_L = 15pF	5	14	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	12	15	18	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
Three-State Capacitance	C_O	-	-	-	20	20	20	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	42	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per buffer.

6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
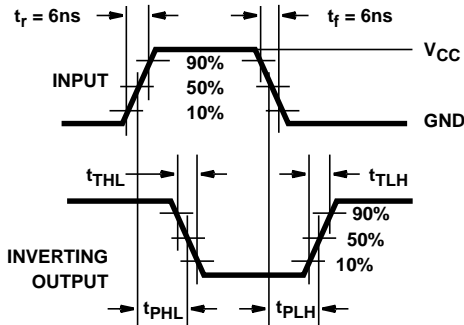
Test Circuits and Waveforms

FIGURE 2. HC TRANSITION TIMES AND PROPAGATION
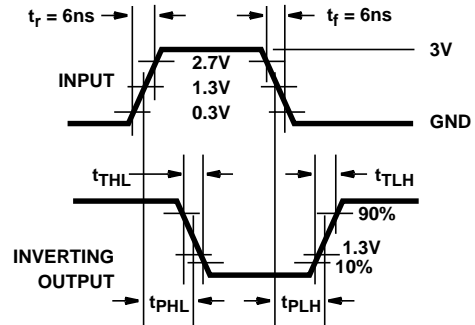DELAY TIMES, COMBINATION LOGIC

FIGURE 3. HCT TRANSITION TIMES AND PROPAGATION
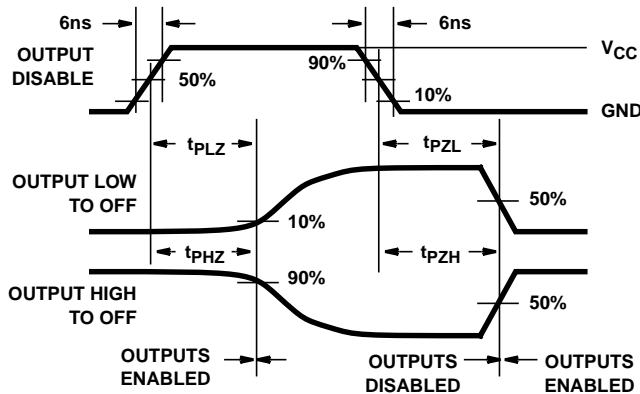DELAY TIMES, COMBINATION LOGIC

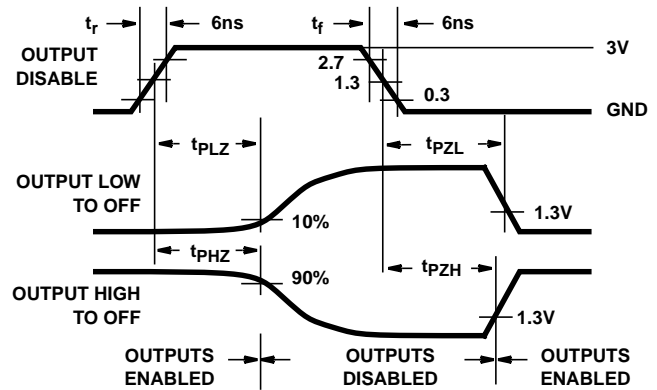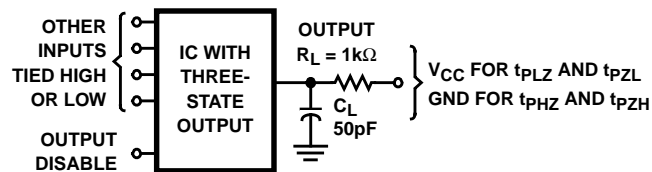FIGURE 4. HC THREE-STATE PROPAGATION DELAY
WAVEFORM

FIGURE 5. HCT THREE-STATE PROPAGATION DELAY
WAVEFORM

NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

FIGURE 6. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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