National Semiconductor

10402 16 x 4-Bit Register File (Random Access Memory)

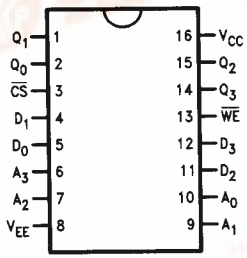
General Description

The 10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, i.e., the memory is non-inverting.

Connection Diagrams

16-Pin Ceramic Dual-In-Line Package



TL/D/9640–2

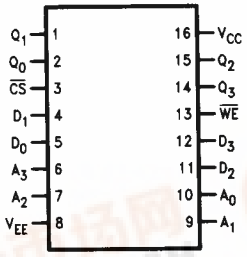
Top View

Order Number 10402DC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Flatpack



TL/D/9640–3

Top View

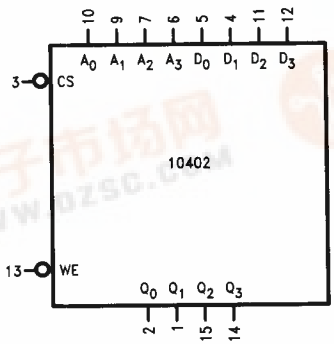
Order Number 10402FC
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select Input
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0–Q_3	Data Outputs



VCC = Pin 16
VEE = Pin 8

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FIGURE 1. Logic Symbol