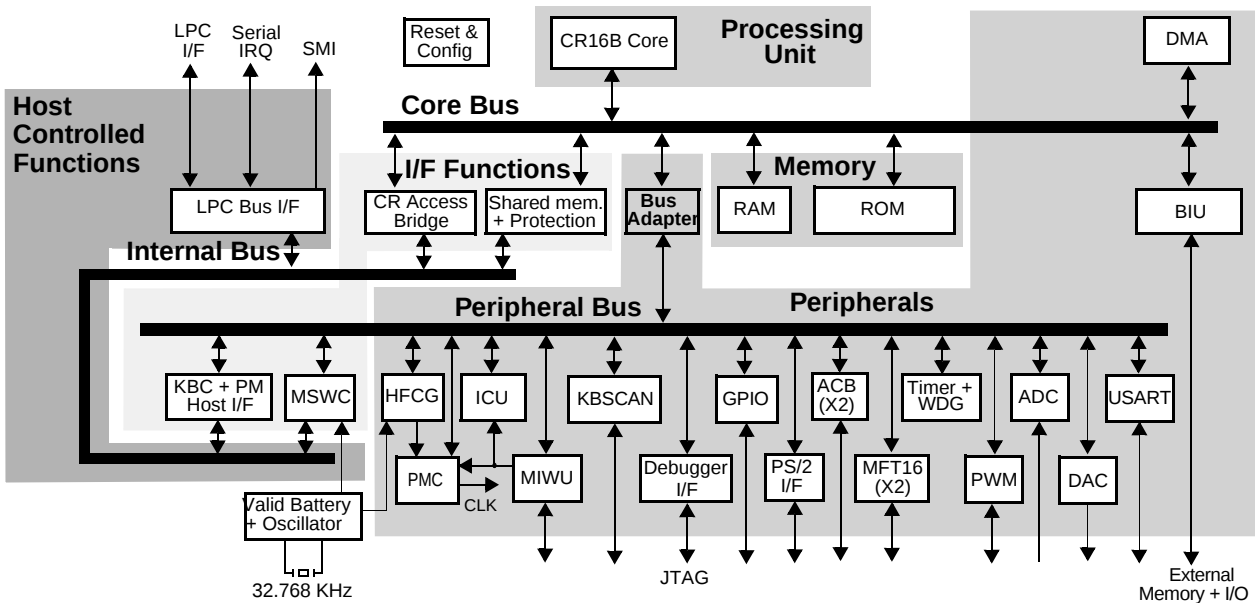


PC97551 Block Diagram



Features

Embedded Controller

- CompactRISC CR16B Processing Unit - a 16-bit embedded RISC processor core (the “core”)
 - Boot block for core code in 4 Kbytes of ROM
 - 4 Kbytes of on-chip RAM with contents protection
 - ROM and RAM both can hold code and data
- Internal Memory
 - Boot block for core code in 4 Kbytes of ROM
 - 4 Kbytes of on-chip RAM with contents protection
 - ROM and RAM both can hold code and data
- Bus Interface Unit (BIU) supporting:
 - Up to 2 Mbytes for code and data
 - Provides two chip-selects for flash/ROM and SRAM devices
 - Provides one chip-select for I/O devices
 - 8- or 16-bit wide bus
 - Configurable wait states
 - Enhanced performance using fast read cycles
 - Single-cycle, fast-read (word-aligned)
 - Two-byte, burst-read (byte-aligned)
 - BIOS sharing with PC host
 - Host-core shared memory access protection
 - Host-controlled with core override
 - 64-Kbyte and 8-Kbyte blocks with independent protection
 - Hardware-protected boot zone for host code
 - Download for on-board code updating
 - Host-controlled via LPC
 - Core-controlled Bus via JTAG or serial port
 - External memory “power-down” mode

Operation Modes

- IRE - Normal operation mode
- OBD - On-Board Development mode
 - Used for development in the final system
 - Communicates with debugger via JTAG interface
 - Hardware breakpoint support
- DEV - Development mode
 - Used in In-System Emulators (ISE) and Application Development Boards (ADB)
 - Communicates with debugger via JTAG interface
 - On-chip ROM is replaced with off-chip SRAM
 - Cycle-by-cycle compatible with IRE mode

LPC System Interface

- 8-bit I/O and 8-bit memory read and write cycles
- 8-bit FWH read and write with wait-sync cycles
- Bootable memory support
- Base Address (BADDR) strap to determine the base address of the Index-Data register pair
- Serial IRQ (SERIRQ) support
- $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support

Core-Controlled Functions

- Interrupt Control Unit (ICU)
 - Non-maskable interrupt input ($\overline{\text{PFAIL}}$)
 - 31 maskable vectored interrupts
 - Enable and pending indication for each interrupt
 - General-purpose external interrupt inputs through MIWU

Features (Continued)

- Provides interrupt on system events (via MSWC)
 - ❑ External modem ring on $\overline{RI}$
 - ❑ IRQ from Keyboard, Mouse and PM channels
 - ❑ Software-triggered event
 - ❑ System ACPI sleep-state change
 - ❑ Power Button mode change
 - ❑ Legacy software “Off” command
- Multi-Input Wake-Up (MIWU)
 - Supports up to 20 wake-up inputs
 - Provides user-selectable trigger conditions
 - Provides wake-up on activity of external pins
 - ❑ General-purpose wake-up inputs
 - ❑ Power switch input
 - ❑ Keyboard scan inputs
 - Generates wake-up event to Power Management Controller (PMC)
 - Generates interrupts to ICU
- General-Purpose I/O (GPIO)
 - 92 port pins (including keyboard scanning)
 - I/O pins individually configured as input or output
 - Optional internal pull-up resistors on inputs
 - Special ports for internal keyboard matrix scanning
 - ❑ 16 open-collector outputs
 - ❑ Eight Schmitt inputs with internal pull-ups
 - Dedicated input for system On/Off switch
 - External GPIO expansion through the BIU I/O Expansion protocol
- PS/2 Interface
 - Supports four external ports for: external keyboard, mouse and two additional pointing devices
 - Supports byte-level handling via hardware accelerator
- Two ACB Interface modules. Each module:
 - Is Intel SMBus and Philips I²C[®] compatible
 - Is SMBus master and slave
 - Detects four simultaneous slave addresses (two user-defined, broadcast and ARP)
 - Supports polling and interrupt controlled operation
 - Generates a wake-up event on detection of a Start Condition (while in Idle mode)
 - Has an optional internal pull-up on SDA and SCL pins
- Universal Synchronous/Asynchronous Receiver-Transmitter (USART)
 - Supports full-duplex USART communication
 - Has programmable baud rate
 - Supports polling and interrupt controlled data transfer
 - Supports synchronous mode with either internal or external clock
 - Supports 9-bit Attention mode
- Two 16-bit Multi Function Timer (MFT16) modules; each module:
 - Contains two 16-bit timers
 - Supports Pulse Width Modulation (PWM), Capture and Counter
- Timer and Watchdog (TWM)
 - 16-bit periodic interrupt timer with 30 μ s resolution and 5-bit prescaler for system tick and periodic wake-up tasks
 - 8-bit watchdog timer
- Pulse Width Modulation (PWM) Module
 - Eight outputs
 - 8/16-bit duty cycle resolution
 - 8/16-bit common input clock prescaler
- Analog to Digital Converter (ADC)
 - Five voltage channels (four external and one internal), with 8-bit resolution
 - Sigma-delta technology for high noise rejection
 - Internal voltage reference
 - Every 100 ms, three of the five channels are measured
- Digital to Analog Converter (DAC)
 - Four channels with 8-bit resolution
 - Rail-to-Rail output range, from AGND to AVCC
 - 1 μ s conversion time

Host-Core Interface Functions

- Host Bus Interface (HBI)
 - Comprises three host interface ports, typically used for KBC and ACPI EC channels:
 - ❑ One 8042 KBC-standard, interface (legacy 60₁₆, 64₁₆).
 - ❑ Two PM interface ports (legacy 62₁₆, 66₁₆ and 68₁₆, 6C₁₆).

These provide ACPI Embedded Controller support with either “Shared” or “Private” interface (regarding SCI/SMI generation).
 - Generates IRQ (with Legacy support), SMI and SCI
 - Provides Fast Gate A20 and Fast Keyboard Reset via firmware
- Core Access to Host-Controlled Functions
 - Host-Core arbitration of function control
 - Host access blocked by the core via lock bits

Features (Continued)

Host-Controlled Functions

- Supports *Microsoft® Advanced Power Management (APM) Specifications Revision 1.2*, February 1996
 - Generates the System Management Interrupt (SMI)
- Supports *ACPI Specification Revision 3.0*, September 2, 2004
 - Generates Power Management Interrupt ($\overline{\text{ECSCI}}$)
 - Generates Power-Up Request ($\overline{\text{PWUREQ}}$)
- Host-controlled functions configuration PC01
 - PnP Configuration Register structure
 - Flexible resource allocation for all logical devices
 - Relocatable base address
 - 15 IRQ routing options
- Mobile System Wake-Up Control (MSWC)
 - Wake-up on detection of:
 - External modem ring on $\overline{\text{RI}}$
 - IRQ from Keyboard, Mouse and PM channels
 - Software-triggered event
 - Routing of wake-up to IRQ, SMI and $\overline{\text{PWUREQ}}$

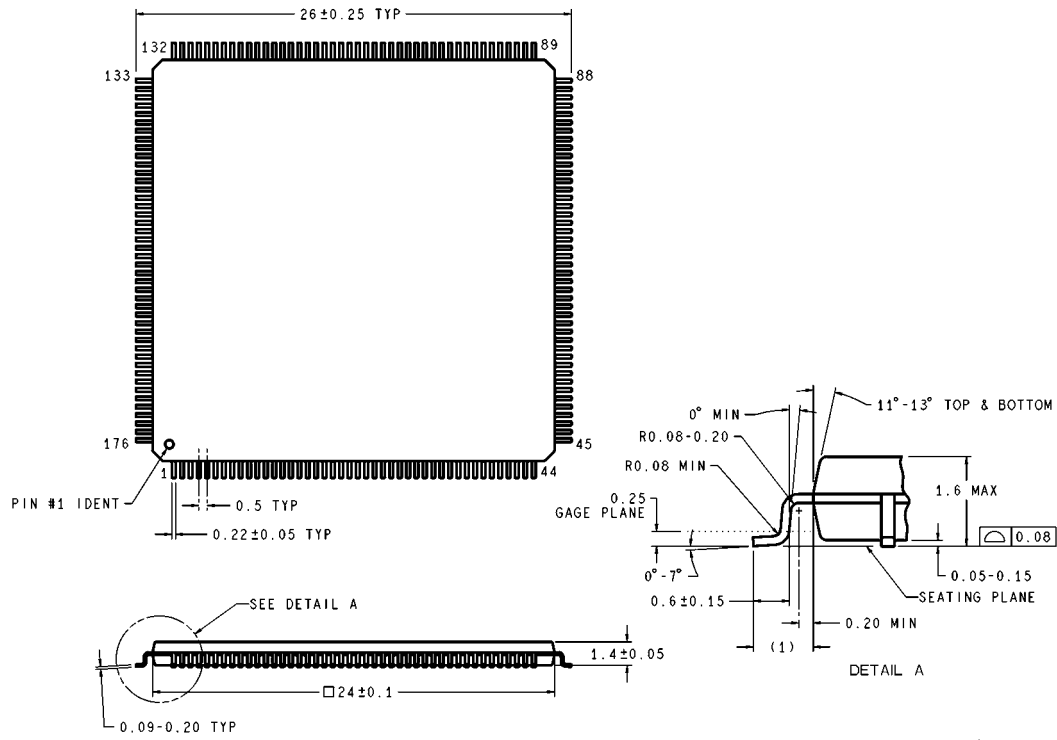
Miscellaneous Features

- Clocks
 - Single 32.768 KHz crystal oscillator with buffered output
 - LPC clock, 0 to 33 MHz
 - On-chip high frequency clock generator
 - Provides core clock, 4-20 MHz
 - Software-controlled frequency generation
 - Generation is based on the 32.768 KHz clock
 - Buffered core clock output
- Strap Inputs for operation control
 - ENV1-0 for IRE/OBD/DEV operating mode selection
 - SHBM for shared BIOS control
 - TRI-STATE® for ISE/ADB support
- Testability
 - XOR-tree structure
 - Includes all device pins (except supply, analog and crystal oscillator pins)
 - Selected at power-up by strap input
 - TRI-STATE device pins, selected at power-up by strap input

- Power Supply
 - 3.3V supply operation
 - 5V tolerance and back-drive protection on all pins (except LPC bus pins, keyboard scan inputs and analog pins)
 - Separate supplies for Host-controlled functions (V_{DD}) and Core-controlled functions (V_{CC})
 - Pin for filtering the on-chip voltage regulator (V_{CORF})
 - Backup battery input for wake-up configuration
 - Four power modes, switched by software or hardware
 - Active mode current (25 mA typ.)
 - Active mode executing WAIT (12 mA typ.)
 - Idle (10 μA typ.)
 - Power off, preserving the wake-up configuration (0.9 μA typ.) from backup battery
- Package
 - 176-pin LQFP package

Physical Dimensions

All dimensions are in millimeters



176-Low Profile Plastic Quad Flatpack (LQFP)
Order Number 97551D5

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