Document Number: MW7IC18100N
Rev. 1, 6/2007

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MW7IC18100NR1
MW7IC18100GNR1
MW7IC18100NBR1

1990 MHz, 100 W, 28 V
GSM/GSM EDGE
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

The MW7IC18100N wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 2050 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulations including GSM EDGE and CDMA.

Final Application

- Typical GSM Performance: V_{DD} = 28 Volts, I_{DQ1} = 180 mA, I_{DQ2} = 1000 mA, P_{out} = 100 Watts CW, 1805-1880 MHz or 1930-1990 MHz
  Power Gain — 30 dB
  Power Added Efficiency — 48%

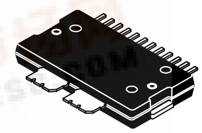
GSM EDGE Application

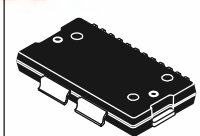
- Typical GSM EDGE Performance: V_{DD} = 28 Volts, I_{DQ1} = 215 mA, I_{DQ2} = 800 mA, P_{out} = 40 Watts Avg., 1805-1880 MHz or 1930-1990 MHz
  Power Gain — 31 dB
  Power Added Efficiency — 35%
  Spectral Regrowth @ 400 kHz Offset = -63 dBc
  Spectral Regrowth @ 600 kHz Offset = -80 dBc
  EVM — 1.5% rms
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 1990 MHz, 100 Watts CW Output Power
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 120 W CW P_{out}.

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

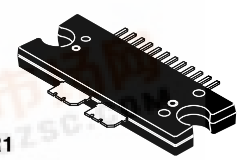
CASE 1618-01
TO-270 WB-14
PLASTIC
MW7IC18100NR1





CASE 1621-01
TO-270 WB-14 GULL
PLASTIC
MW7IC18100GNR1

CASE 1617-01
TO-272 WB-14
PLASTIC
MW7IC18100NBR1



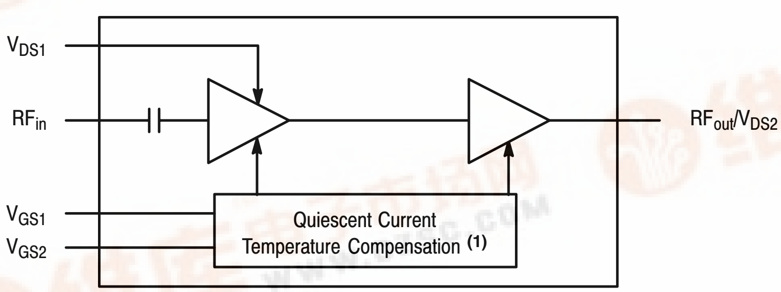
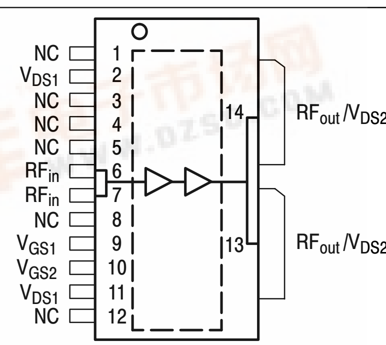


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

freescale™

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value [1,2]	Unit
Thermal Resistance, Junction to Case GSM Application (P_{out} = 100 W CW)	 Stage 1, 28 Vdc, I_{DQ1} = 180 mA Stage 2, 28 Vdc, I_{DQ2} = 1000 mA	$R_{\theta JC}$	 2.0 0.51	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	O (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

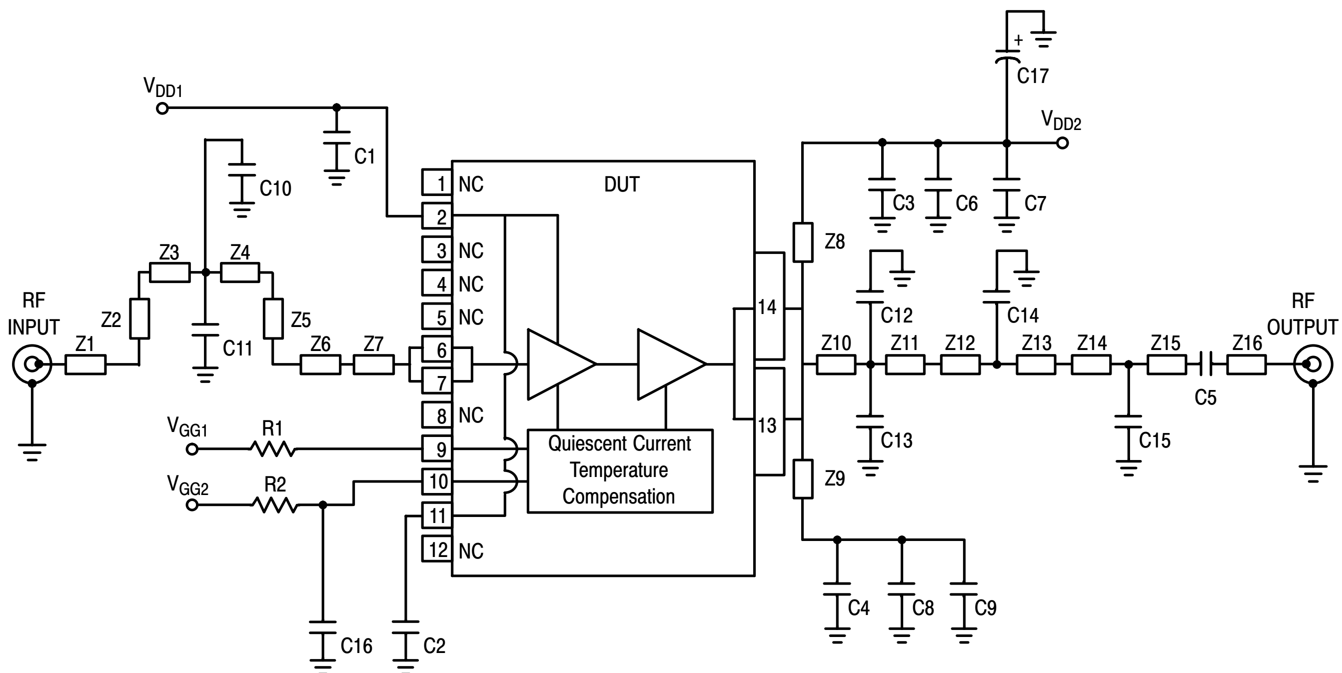
Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 100 W CW, I_{DQ1} = 180 mA, I_{DQ2} = 1000 mA, f = 1990 MHz.					
Power Gain	G_{ps}	27	30	31	dB
Input Return Loss	IRL	—	-15	-10	dB
Power Added Efficiency	PAE	45	48	—	%
P_{out} @ 1 dB Compression Point, CW	P1dB	100	112	—	W
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 215 mA, I_{DQ2} = 800 mA, P_{out} = 40 W Avg., 1805-1880 MHz or 1930-1990 MHz EDGE Modulation.					
Power Gain	G_{ps}	—	31	—	dB
Power Added Efficiency	PAE	—	35	—	%
Error Vector Magnitude	EVM	—	1.5	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-80	—	dBc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
2. MTTF calculator available at http://www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 180 mA, I_{DQ2} = 1000 mA, 1930-1990 MHz Bandwidth					
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 100 W CW	G_F	—	0.37	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 100 W CW	Φ	—	0.502	—	°
Average Group Delay @ P_{out} = 100 W CW, f = 1960 MHz	Delay	—	2.57	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 100 W CW, f = 1960 MHz, Six Sigma Window	ΔΦ	—	63.65	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.048	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.004	—	dBm/°C



Z1	0.083″ x 0.505″ Microstrip	Z11	0.880″ x 0.256″ Microstrip
Z2, Z5	0.083″ x 0.552″ Microstrip	Z12	0.215″ x 0.138″ Microstrip
Z3	0.083″ x 0.252″ Microstrip	Z13	0.215″ x 0.252″ Microstrip
Z4	0.083″ x 0.174″ Microstrip	Z14	0.083″ x 0.298″ Microstrip
Z6	0.083″ x 1.261″ Microstrip	Z15	0.083″ x 0.810″ Microstrip
Z7	0.060″ x 0.126″ Microstrip	Z16	0.083″ x 0.250″ Microstrip
Z8, Z9	0.080″ x 1.569″ Microstrip	PCB	Arlon AD250, 0.030″, ε_r = 2.5
Z10	0.880″ x 0.224″ Microstrip		

Figure 3. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Schematic — 1900 MHz

Table 6. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1900 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C6, C7, C8, C9	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C10, C11	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C12, C13	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C14	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C15	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C16	2.2 μF, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C17	470 μF, 63 V Electrolytic Capacitor, Radial	477KXM063M	Illinois Capacitor
R1, R2	10 KΩ, 1/4 W Chip Resistors	CRCW12061001FKTA	Vishay

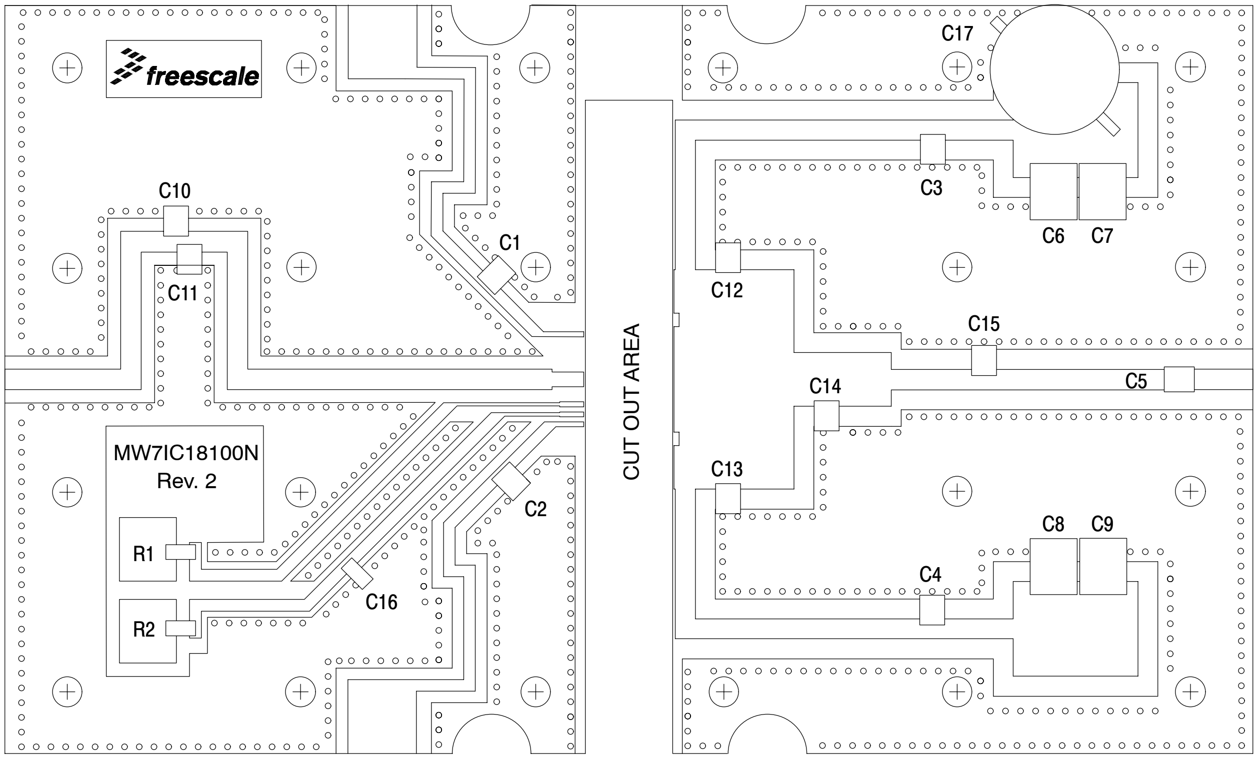


Figure 4. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Component Layout — 1900 MHz

TYPICAL CHARACTERISTICS — 1900 MHz

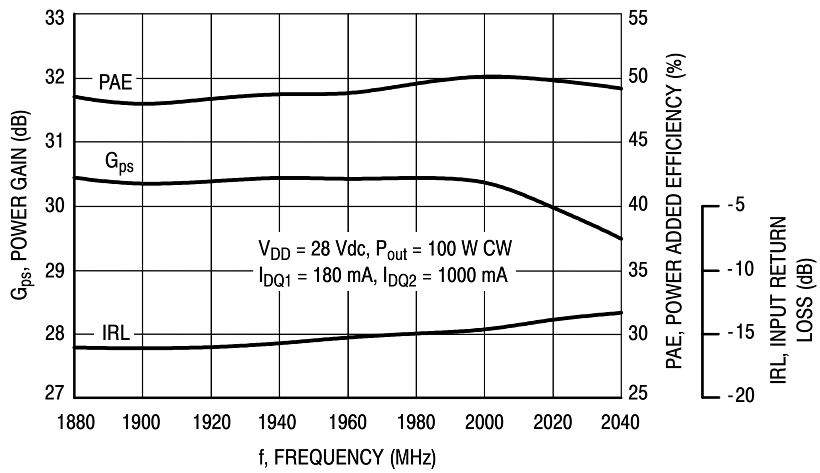


Figure 5. Power Gain, Input Return Loss and Power Added Efficiency versus Frequency @ P_{out} = 100 Watts CW

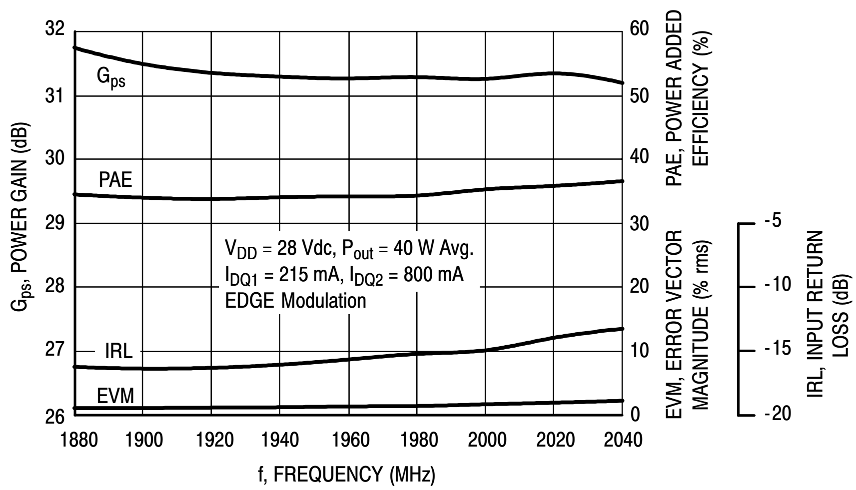


Figure 6. Power Gain, Input Return Loss, EVM and Power Added Efficiency versus Frequency @ P_{out} = 40 Watts Avg.

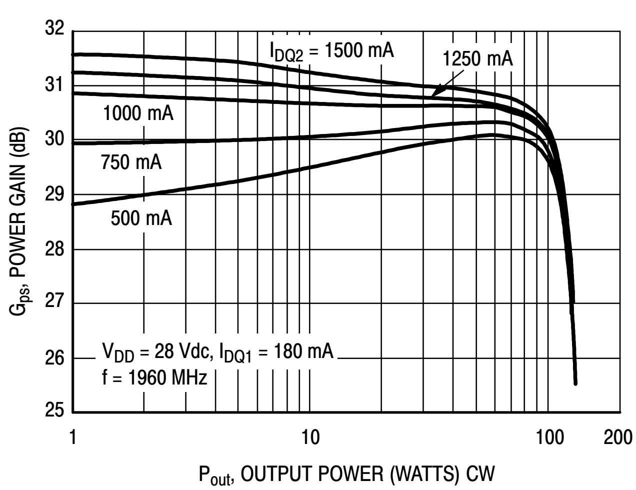


Figure 7. Two-Tone Power Gain versus Output Power @ I_{DQ1} = 180 mA

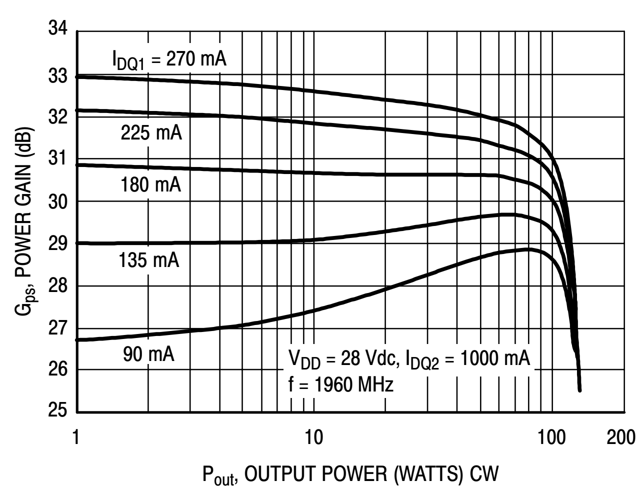


Figure 8. Two-Tone Power Gain versus Output Power @ I_{DQ2} = 1000 mA

TYPICAL CHARACTERISTICS — 1900 MHz

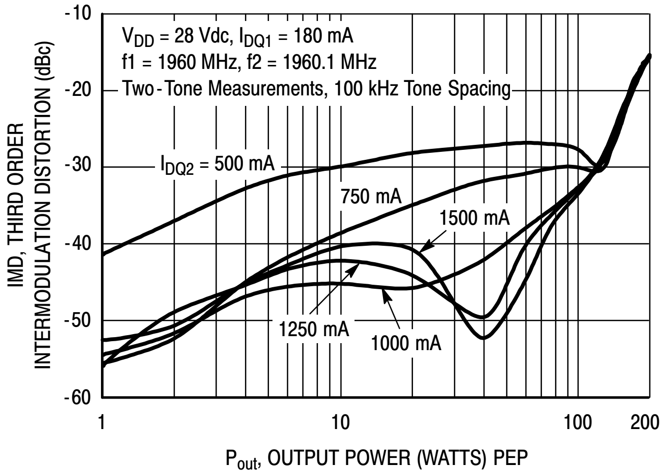


Figure 9. Third Order Intermodulation Distortion versus Output Power @ I_{DQ1} = 180 mA

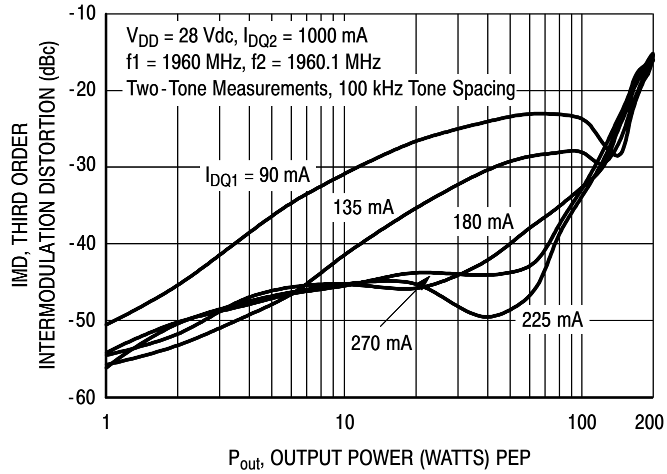


Figure 10. Third Order Intermodulation Distortion versus Output Power @ I_{DQ2} = 1000 mA

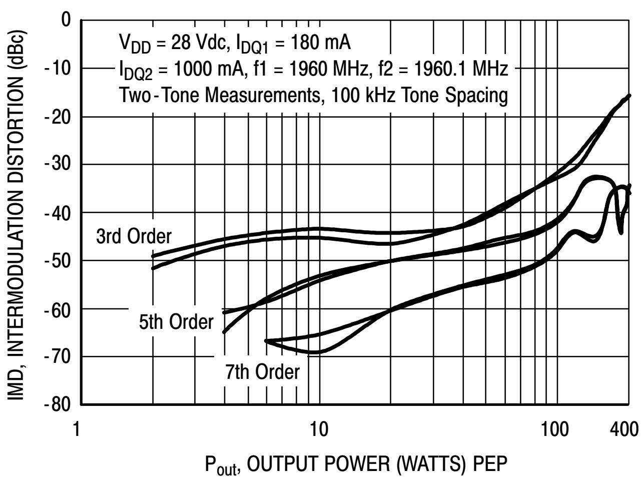


Figure 11. Intermodulation Distortion Products versus Output Power

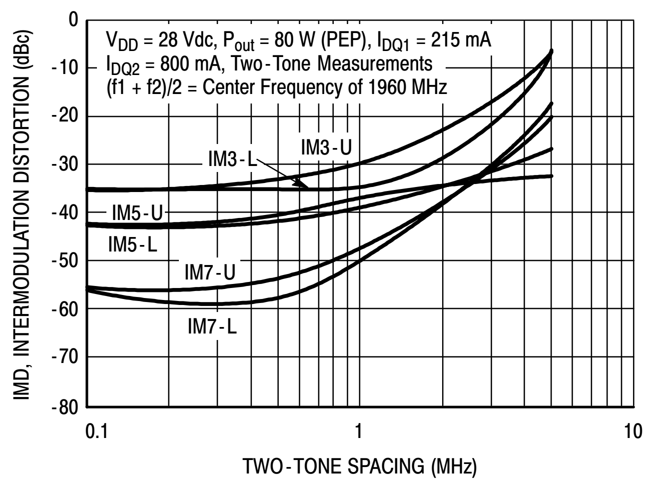


Figure 12. Intermodulation Distortion Products versus Tone Spacing

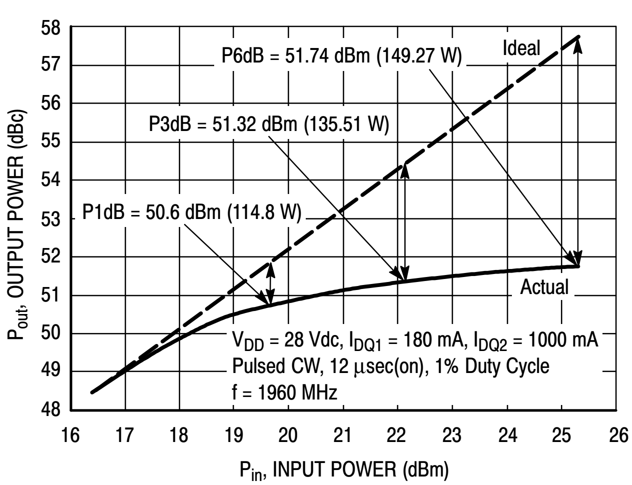


Figure 13. Pulsed CW Output Power versus Input Power

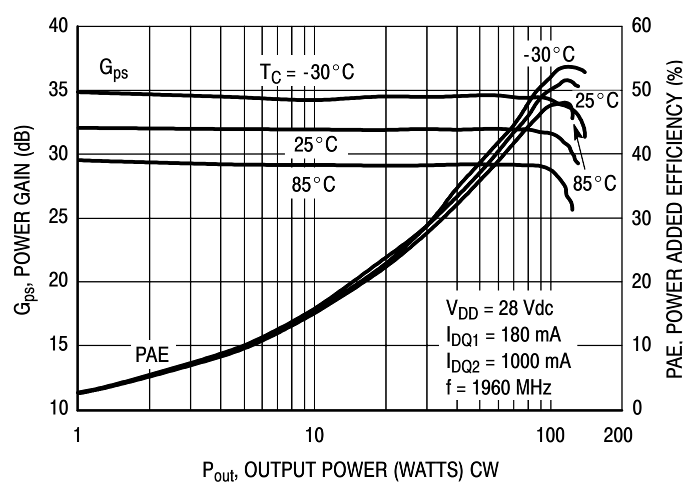


Figure 14. Power Gain and Power Added Efficiency versus Output Power

TYPICAL CHARACTERISTICS — 1900 MHz

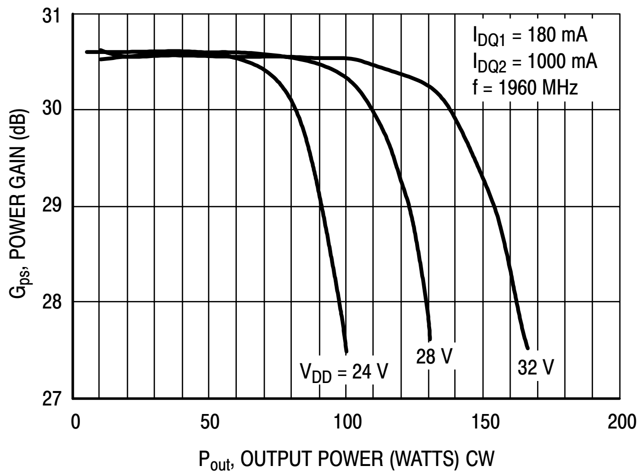


Figure 15. Power Gain versus Output Power

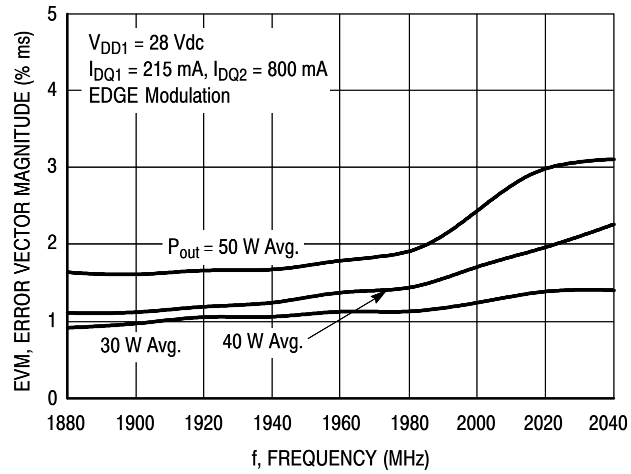


Figure 16. EVM versus Frequency

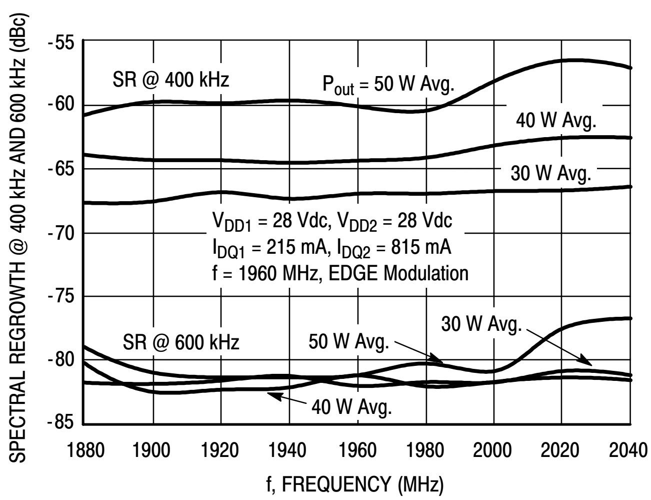


Figure 17. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

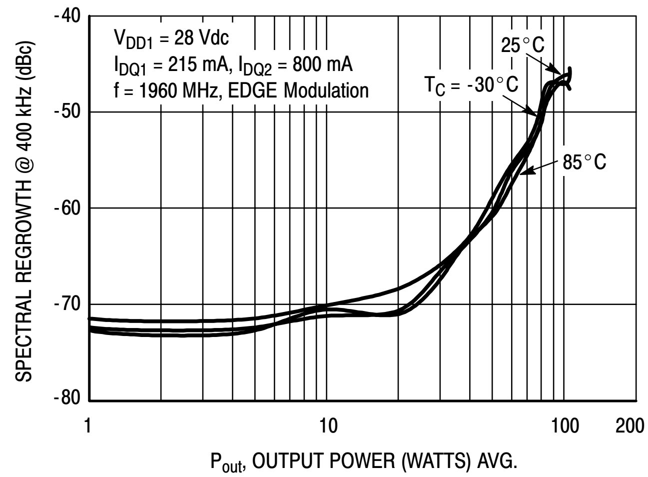


Figure 18. Spectral Regrowth at 400 kHz versus Output Power

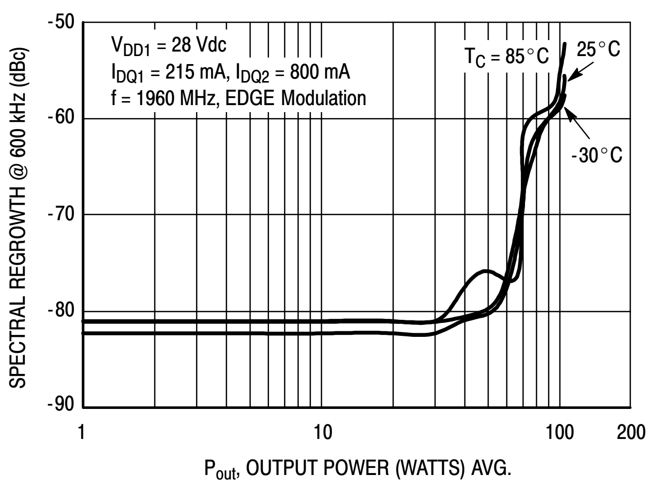


Figure 19. Spectral Regrowth at 600 kHz versus Output Power

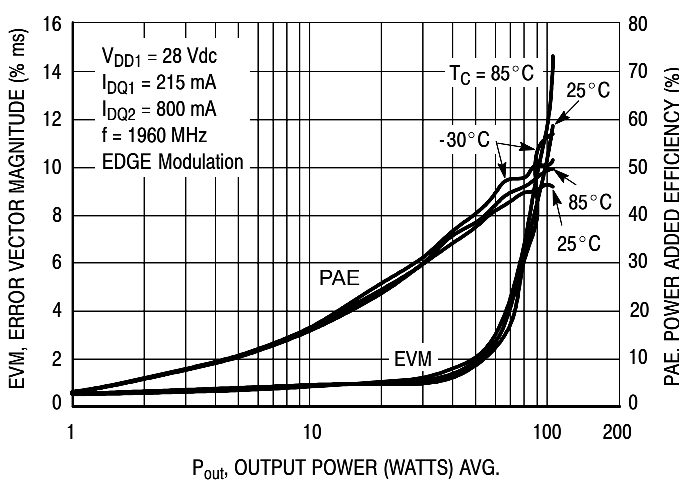


Figure 20. EVM and Power Added Efficiency versus Output Power

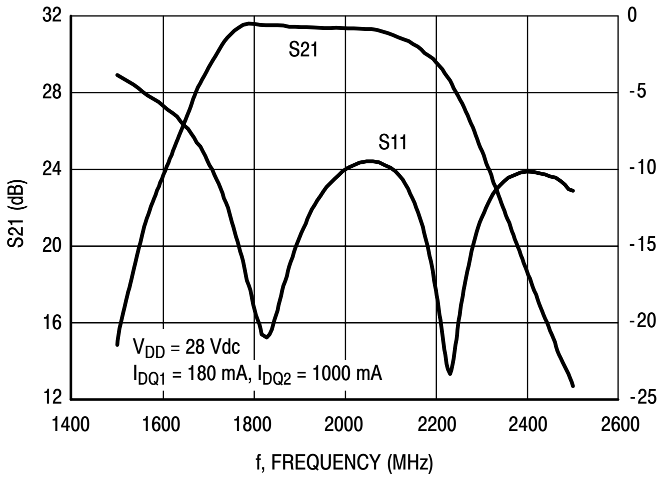


Figure 21. Broadband Frequency Response

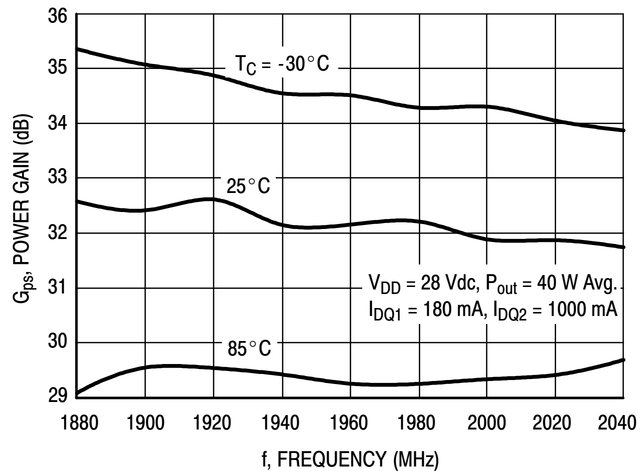
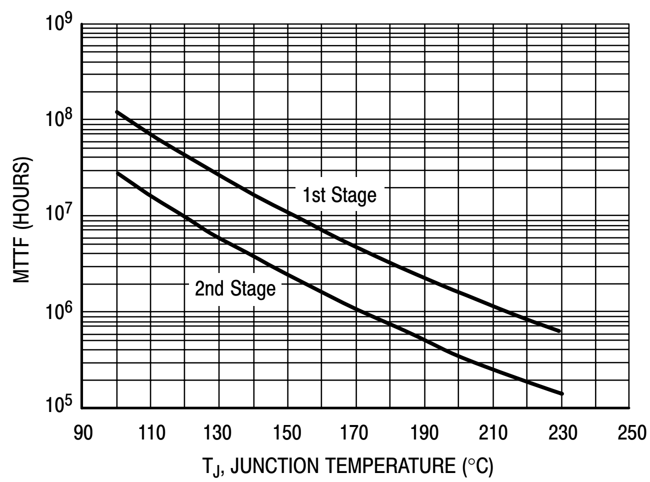


Figure 22. Power Gain versus Frequency



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 28 Vdc, P_{out} = 100 W CW, and PAE = 48%.

MTTF calculator available at http:/www.freescale.com/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 23. MTTF versus Junction Temperature

GSM TEST SIGNAL

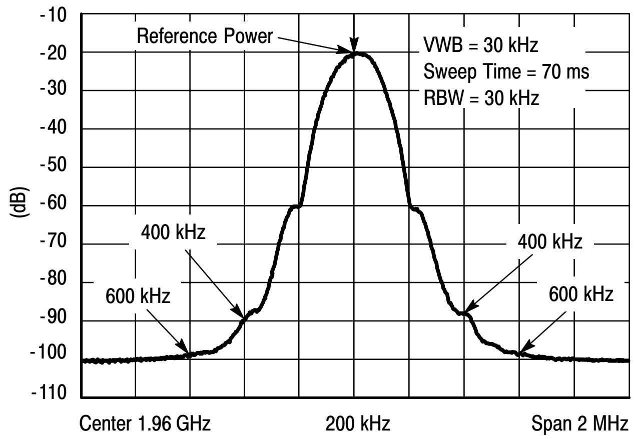
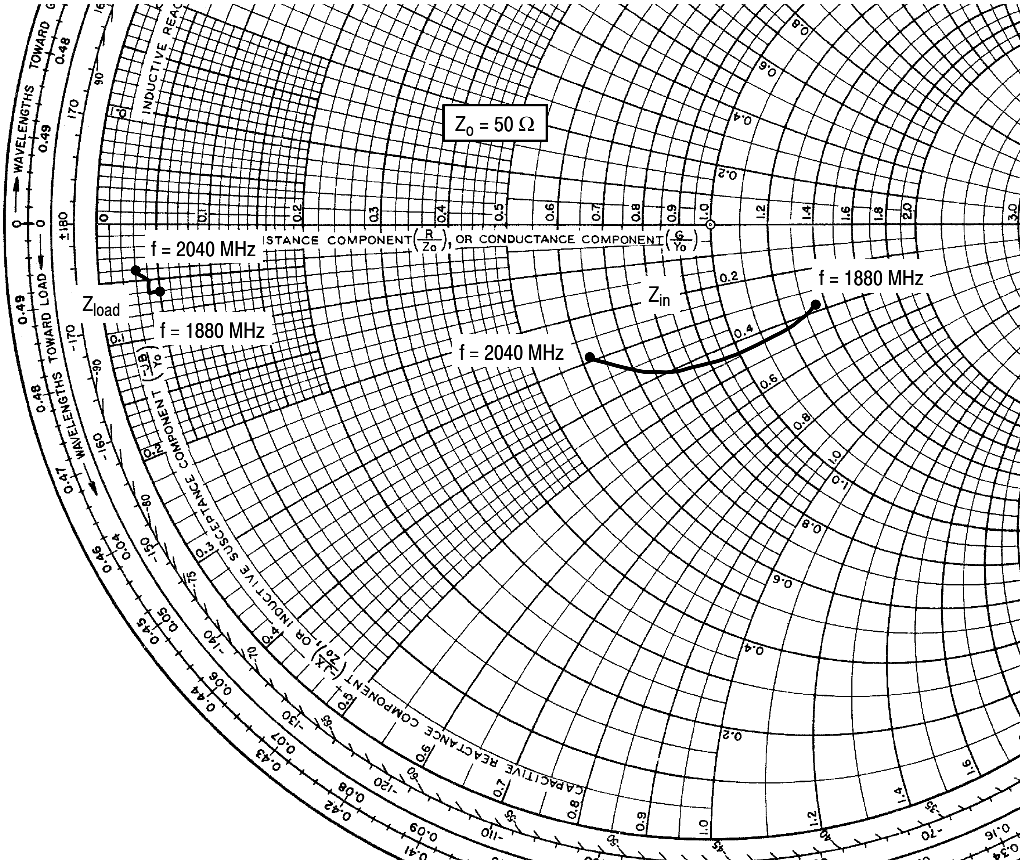


Figure 24. EDGE Spectrum



$V_{DD1} = V_{DD2}$ = 28 Vdc, I_{DQ1} = 180 mA, I_{DQ2} = 1000 mA, P_{out} = 100 W CW

f MHz	Z_{in} Ω	Z_{load} Ω
1880	67.48 - j17.89	2.324 - j3.239
1900	60.03 - j20.86	2.234 - j3.105
1920	53.65 - j21.94	2.135 - j2.965
1940	48.13 - j21.94	2.037 - j2.818
1960	43.52 - j21.22	1.936 - j2.666
1980	39.60 - j20.00	1.851 - j2.509
2000	36.14 - j18.52	1.765 - j2.355
2020	33.19 - j16.57	1.669 - j2.193
2040	30.96 - j14.58	1.559 - j2.012

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

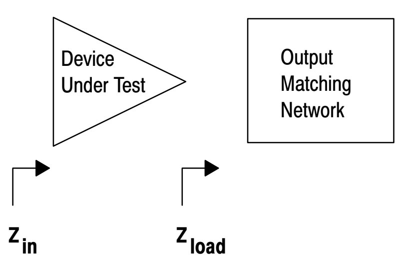
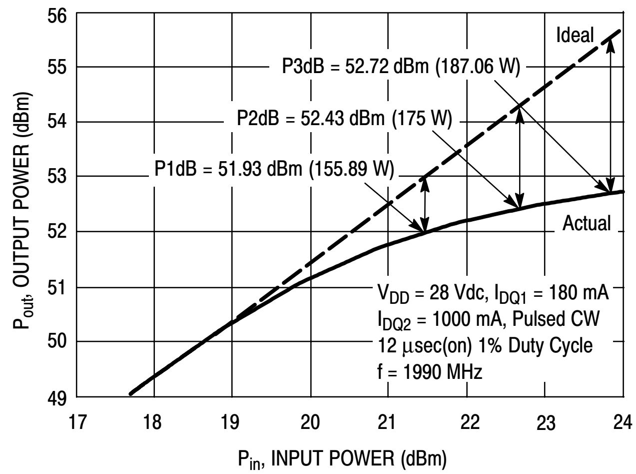


Figure 25. Series Equivalent Input and Load Impedance — 1900 MHz

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 180 mA, I_{DQ2} = 1000 mA, T_C = 25°C, 50 Ohm System)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1500	0.612	118.5	6.369	69.06	0.002	102.9	0.615	47.74
1550	0.557	104.3	11.42	18.29	0.003	85.09	0.666	-41.54
1600	0.491	88.33	16.92	-34.34	0.005	59.06	0.844	-113.4
1650	0.410	70.24	23.21	-84.03	0.005	28.40	0.931	-163.4
1700	0.313	48.99	30.49	-135.7	0.006	7.983	0.887	155.6
1750	0.216	21.99	32.64	168.8	0.007	-15.63	0.700	120.3
1800	0.131	-22.83	32.93	114.0	0.006	-35.27	0.475	95.71
1850	0.117	-95.13	32.62	65.01	0.006	-53.22	0.332	82.10
1900	0.185	-146.3	32.58	20.45	0.006	-77.03	0.252	68.30
1950	0.253	-177.3	32.45	-22.53	0.007	-98.93	0.165	47.02
2000	0.303	160.4	32.41	-65.29	0.007	-108.4	0.052	8.742
2050	0.328	139.5	32.33	-108.6	0.006	-127.3	0.070	-154.8
2100	0.331	117.9	32.50	-152.7	0.008	-145.8	0.161	179.9
2150	0.273	91.65	32.84	160.2	0.008	-169.1	0.257	165.7
2200	0.141	64.27	32.52	109.2	0.008	162.7	0.424	150.3
2250	0.050	172.7	28.92	56.72	0.009	138.3	0.641	123.4
2300	0.194	163.4	21.30	8.112	0.007	112.6	0.804	91.99
2350	0.270	139.7	14.62	-34.53	0.007	97.74	0.879	62.03
2400	0.288	118.9	9.878	-72.70	0.007	84.37	0.910	34.57
2450	0.274	100.6	6.771	-107.5	0.007	70.79	0.911	8.878
2500	0.236	83.35	4.579	-141.3	0.007	55.31	0.903	-16.73

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS — 1900 MHz

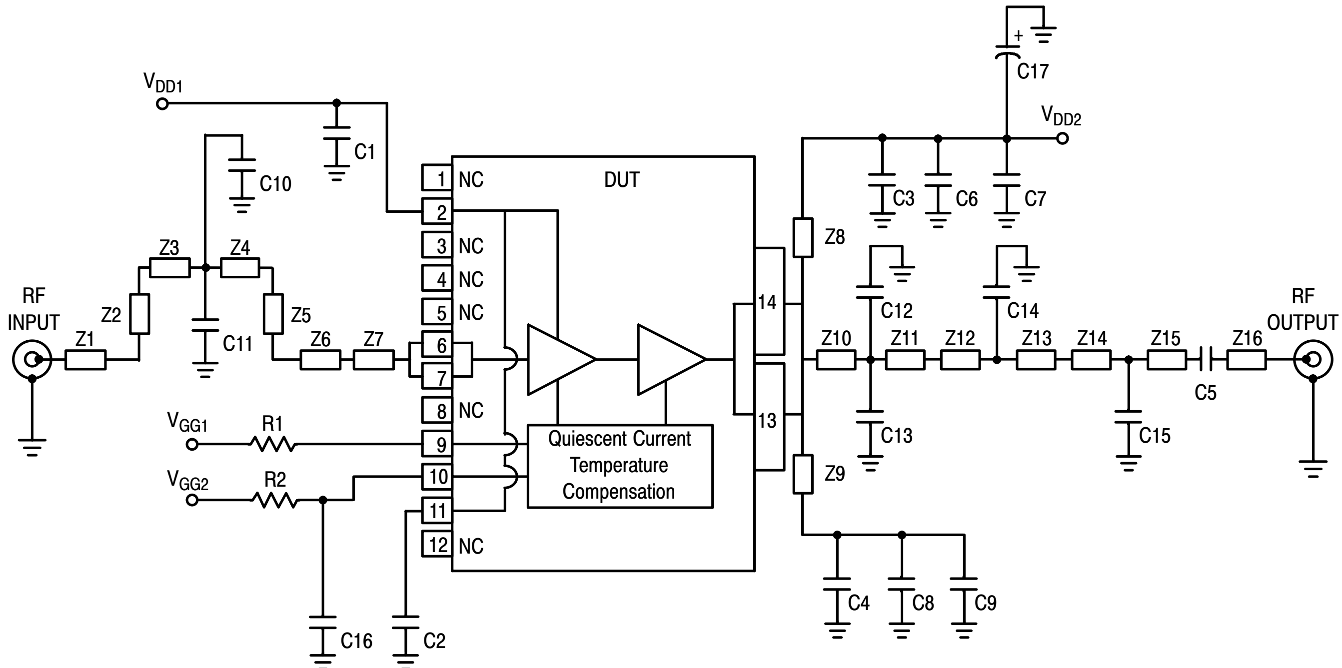


NOTE: Load Pull Test Fixture Tuned for Peak Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	40.2 - j30.91	0.96 - j3.14

Figure 26. Pulsed CW Output Power versus Input Power @ 28 V



Z1	0.083″ x 0.505″ Microstrip	Z11	0.880″ x 0.256″ Microstrip
Z2, Z5	0.083″ x 0.552″ Microstrip	Z12	0.215″ x 0.138″ Microstrip
Z3	0.083″ x 0.252″ Microstrip	Z13	0.215″ x 0.252″ Microstrip
Z4	0.083″ x 0.174″ Microstrip	Z14	0.083″ x 0.298″ Microstrip
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Z8, Z9	0.080″ x 1.569″ Microstrip	PCB	Arlon AD250, 0.030″, ε_r = 2.5
Z10	0.880″ x 0.224″ Microstrip		

Figure 27. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Schematic — 1800 MHz

Table 8. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1800 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C6, C7, C8, C9	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C10, C11	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C12, C13	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
C14	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
C15	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C16	2.2 μF, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C17	470 μF, 63 V Electrolytic Capacitor, Radial	477KXM063M	Illinois Capacitor
R1, R2	10 KΩ, 1/4 W Chip Resistors	CRCW12061001FKTA	Vishay

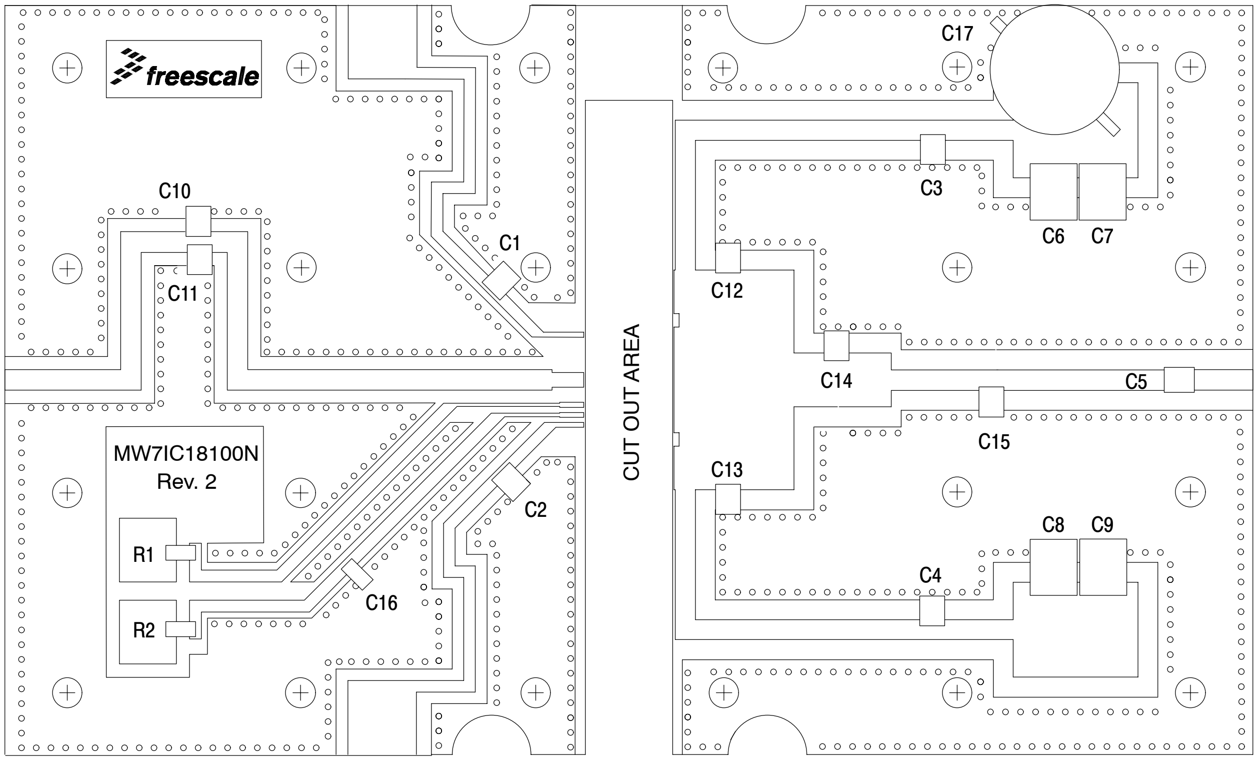


Figure 28. MW7IC18100NR1(GNR1)(NBR1) Test Circuit Component Layout — 1800 MHz

TYPICAL CHARACTERISTICS — 1800 MHz

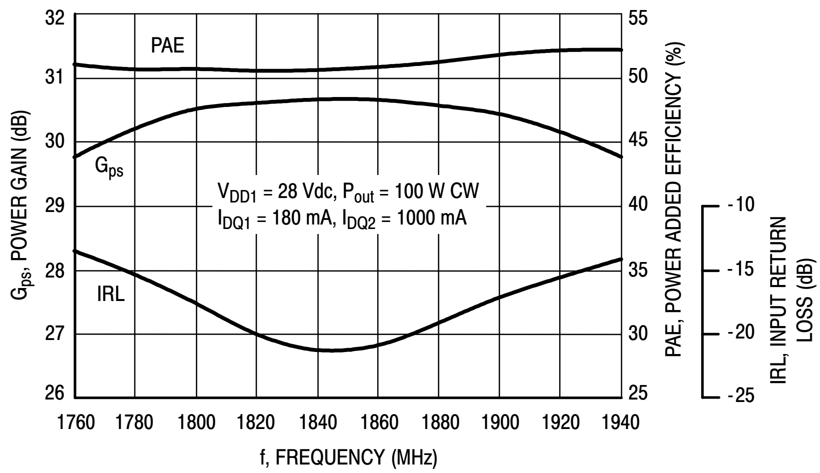


Figure 29. Power Gain, Input Return Loss and Power Added Efficiency versus Frequency @ P_{out} = 100 Watts CW

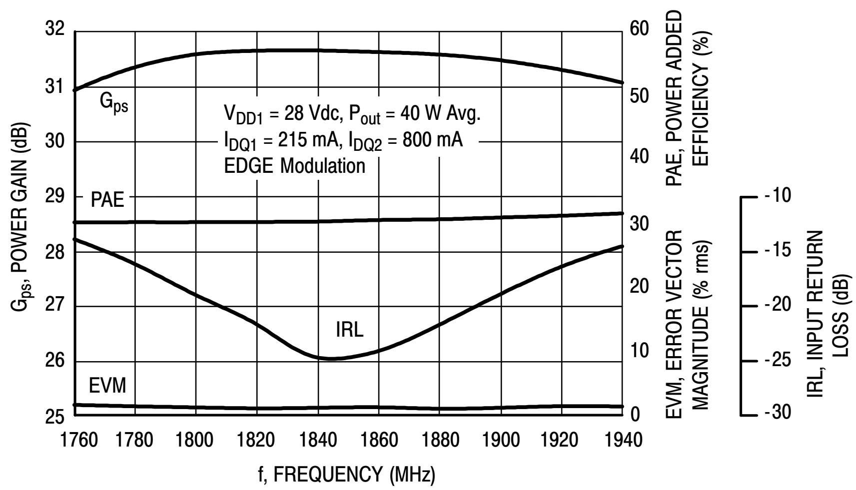


Figure 30. Power Gain, Input Return Loss, EVM and Power Added Efficiency versus Frequency @ P_{out} = 40 Watts Avg.

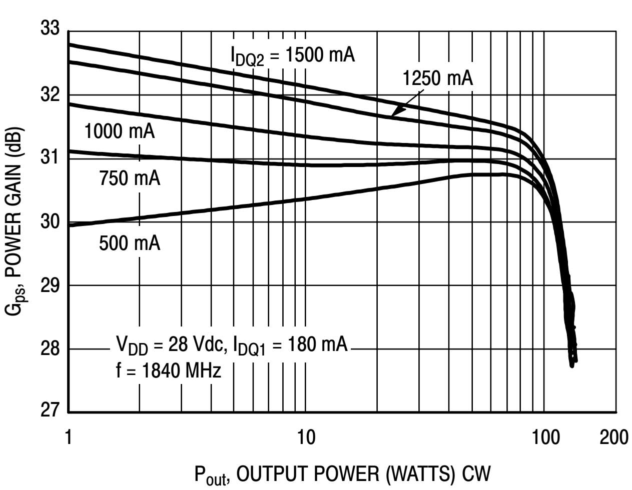


Figure 31. Two-Tone Power Gain versus Output Power @ I_{DQ1} =180 mA

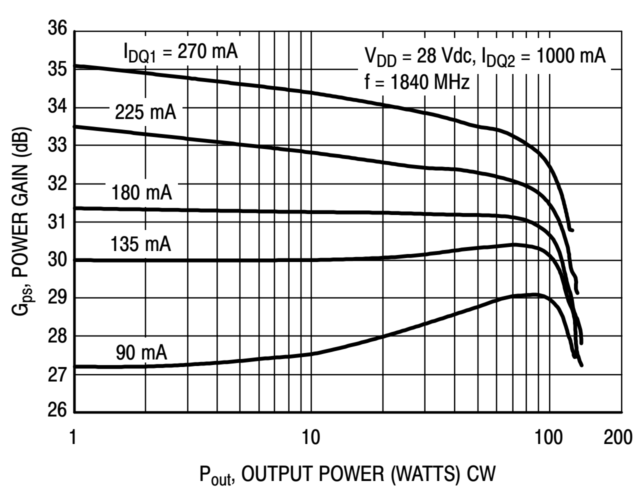


Figure 32. Two-Tone Power Gain versus Output Power @ I_{DQ2} = 1000 mA

TYPICAL CHARACTERISTICS — 1800 MHz

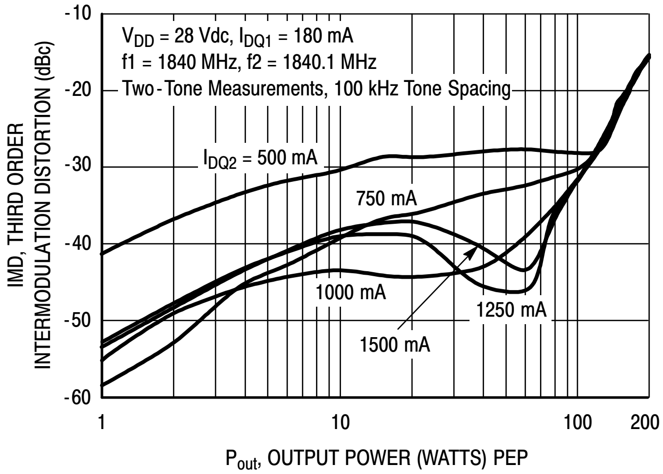


Figure 33. Third Order Intermodulation Distortion versus Output Power @ I_{DQ1} = 180 mA

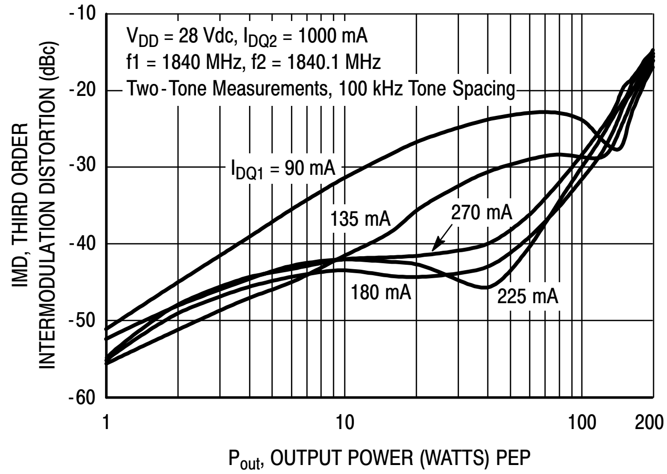


Figure 34. Third Order Intermodulation Distortion versus Output Power @ I_{DQ2} = 1000 mA

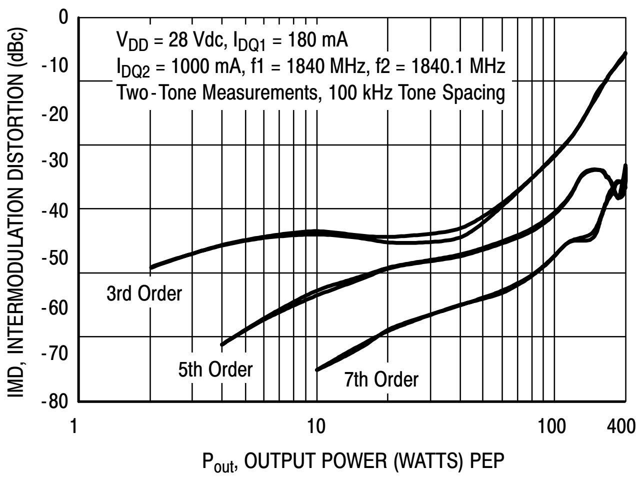


Figure 35. Intermodulation Distortion Products versus Output Power

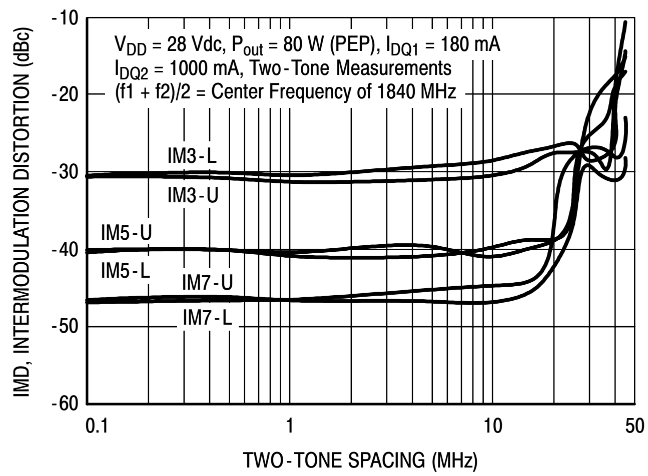


Figure 36. Intermodulation Distortion Products versus Tone Spacing

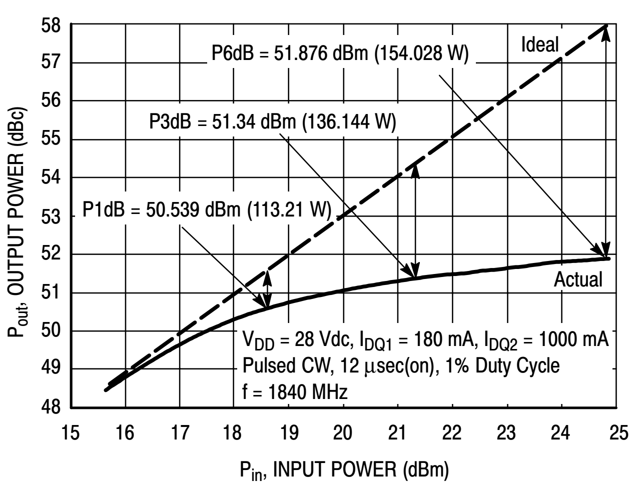


Figure 37. Pulsed CW Output Power versus Input Power

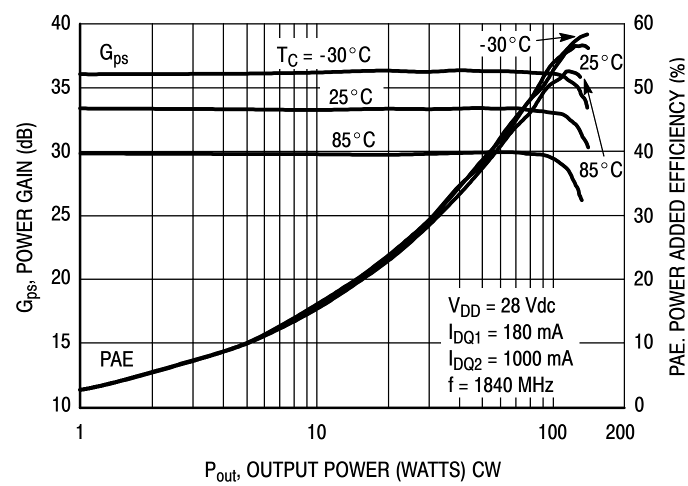


Figure 38. Power Gain and Power Added Efficiency versus Output Power

TYPICAL CHARACTERISTICS — 1800 MHz

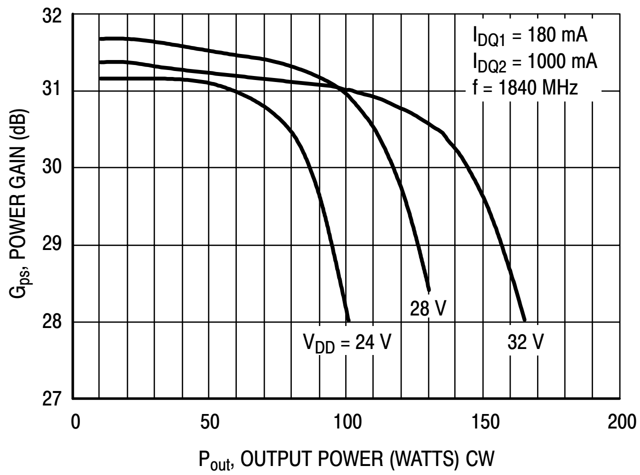


Figure 39. Power Gain versus Output Power

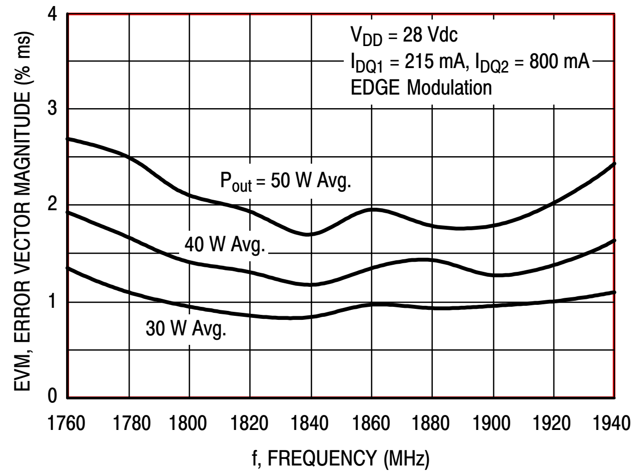


Figure 40. EVM versus Frequency

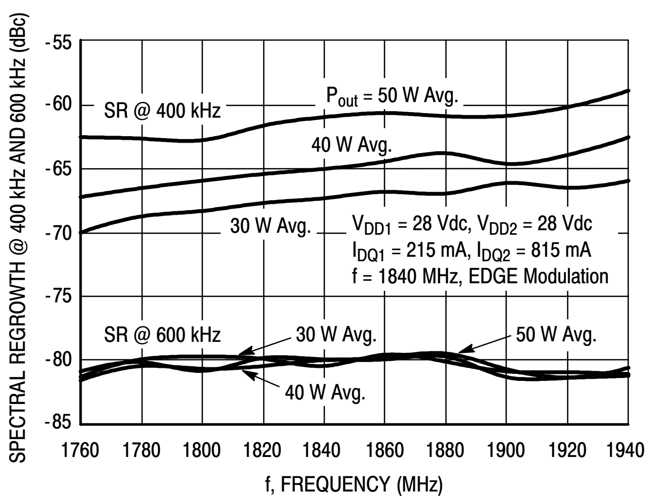


Figure 41. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency

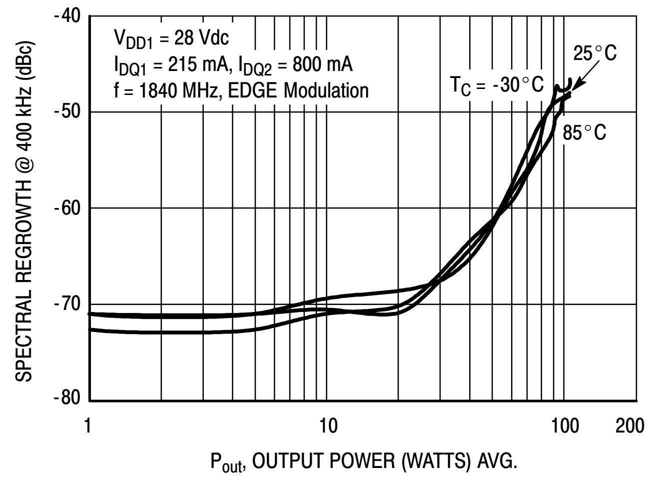


Figure 42. Spectral Regrowth at 400 kHz versus Output Power

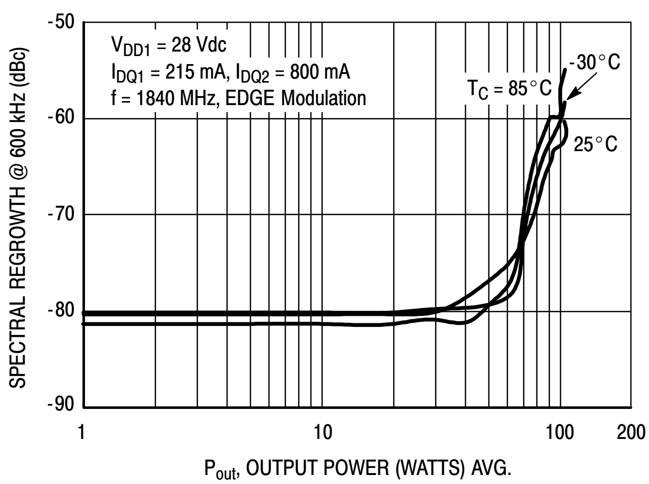


Figure 43. Spectral Regrowth at 600 kHz versus Output Power

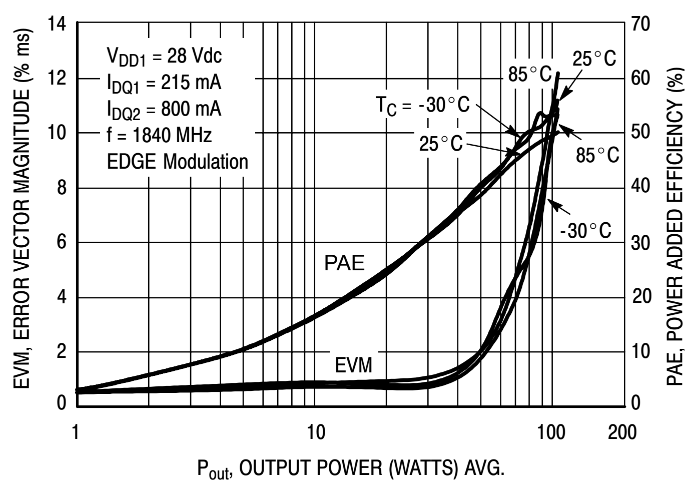


Figure 44. EVM and Power Added Efficiency versus Output Power

TYPICAL CHARACTERISTICS — 1800 MHz

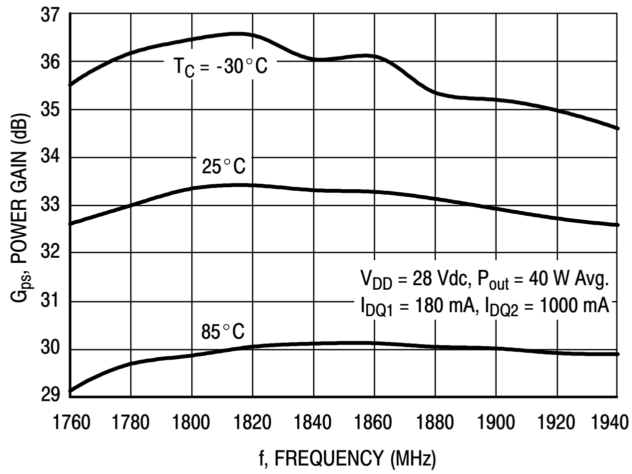
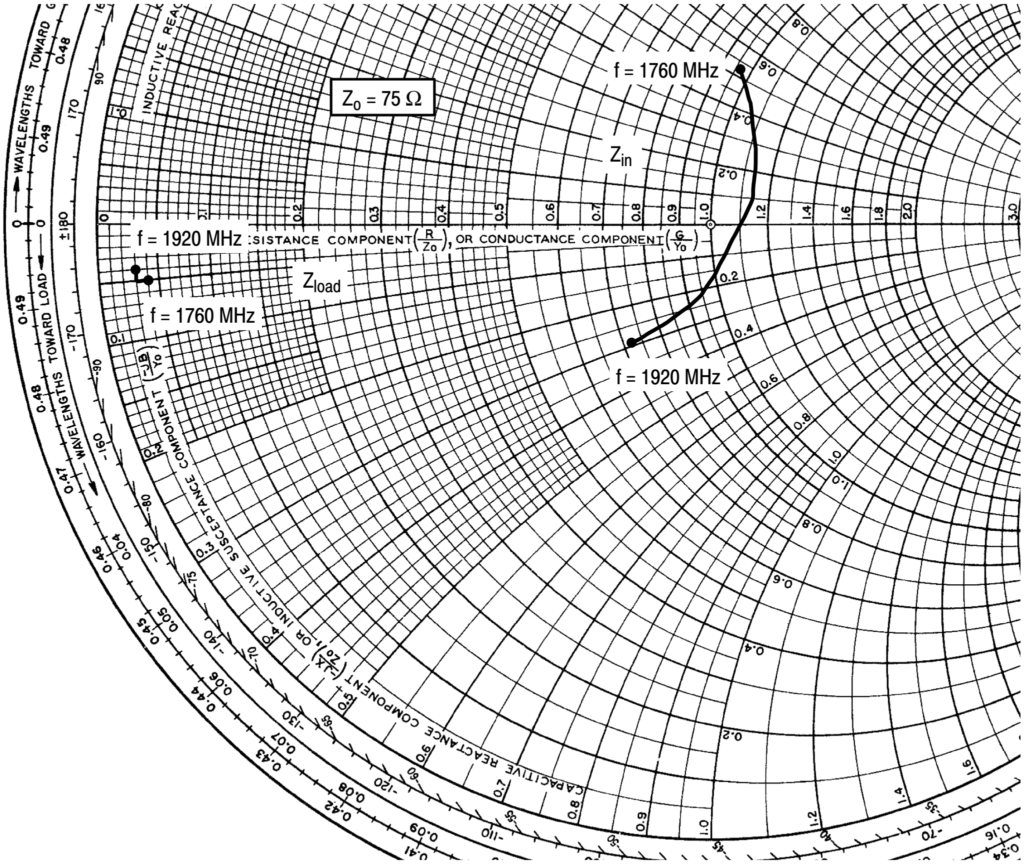


Figure 45. Power Gain versus Frequency



$V_{DD1} = V_{DD2} = 28$ Vdc, $I_{DQ1} = 180$ mA, $I_{DQ2} = 1000$ mA, $P_{out} = 100$ W CW

f MHz	Z_{in} Ω	Z_{load} Ω
1760	71.78 + j40.05	2.983 - j3.974
1780	79.83 + j31.13	2.872 - j3.861
1800	84.35 + j19.44	2.757 - j3.745
1820	84.75 + j7.234	2.636 - j3.639
1840	81.21 - j4.076	2.535 - j3.506
1860	74.76 - j12.32	2.434 - j3.376
1880	67.49 - j17.89	2.324 - j3.239
1900	60.03 - j20.86	2.234 - j3.105
1920	53.65 - j21.94	2.135 - j2.965

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

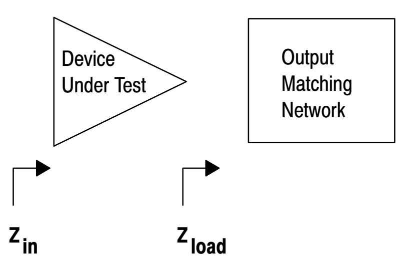
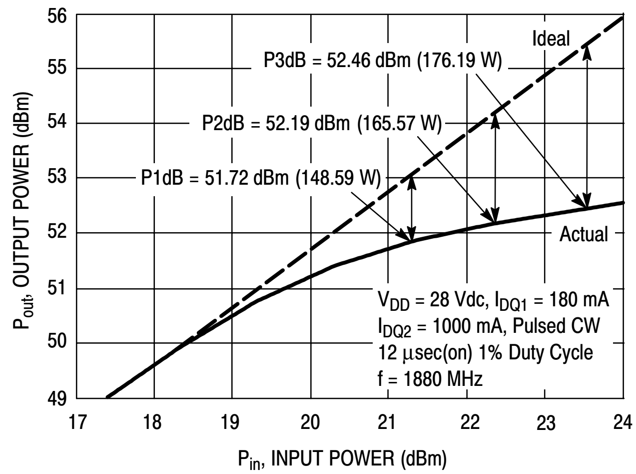


Figure 46. Series Equivalent Input and Load Impedance — 1800 MHz

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS — 1800 MHz



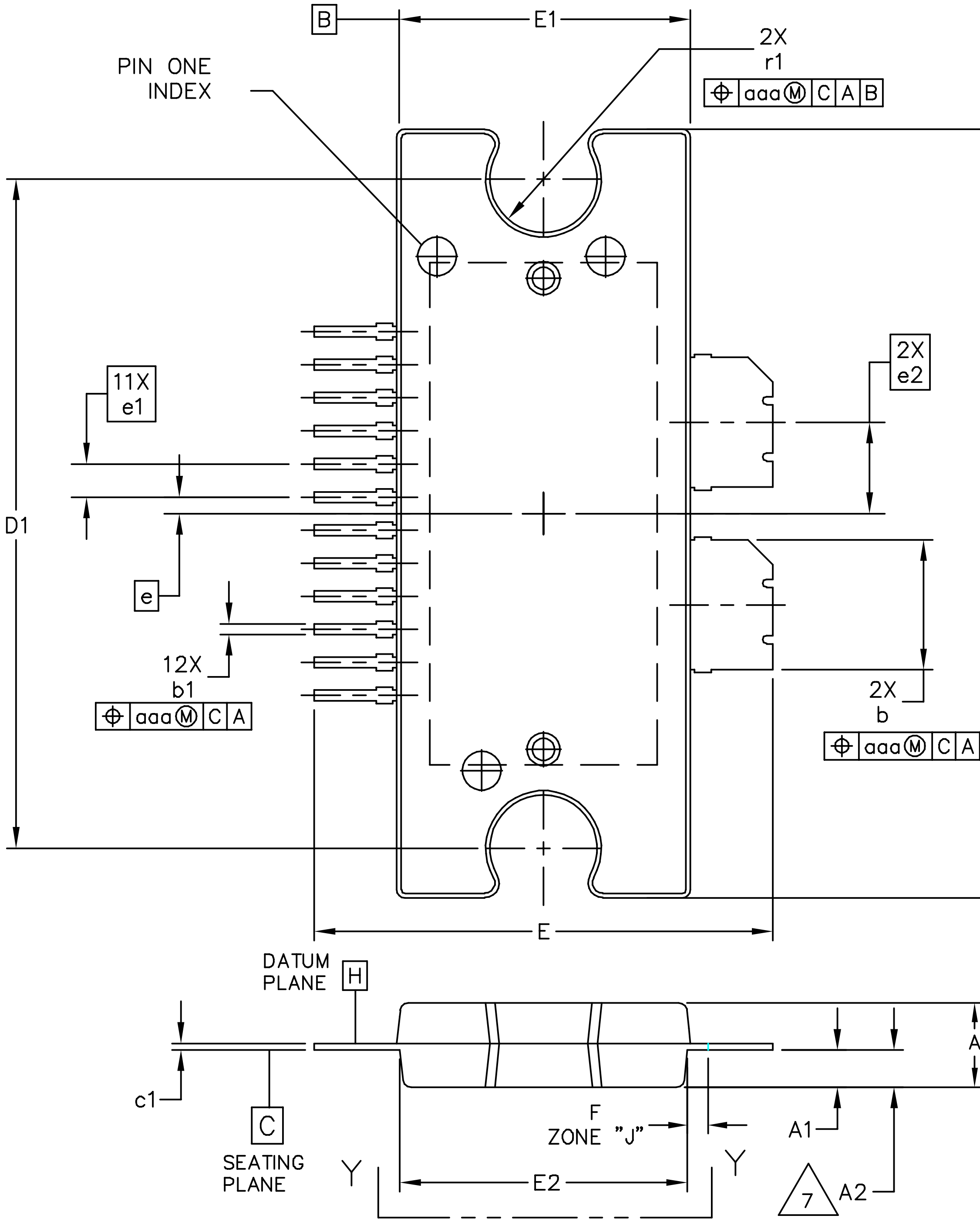
NOTE: Load Pull Test Fixture Tuned for Peak Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P3dB	83.04 - j2.44	1.36 - j3.19

Figure 47. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS



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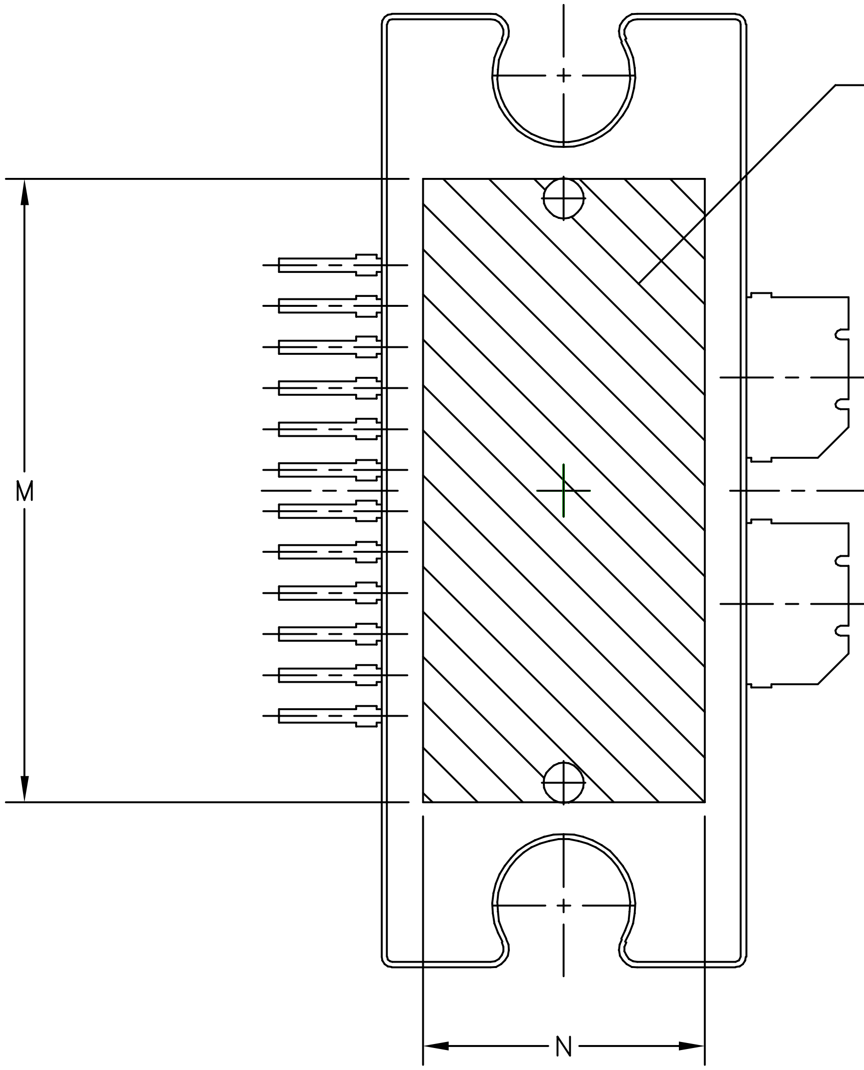
TITLE: TO-272 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10649D		REV: 0
	CASE NUMBER: 1617-01		23 NOV 2005
	STANDARD: NON-JEDEC		



VIEW Y–Y

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	CASE NUMBER: 1617–01	23 NOV 2005
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.96	1.12	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC		aaa	.004		.10	
M	.600	----	15.24	----					
N	.270	----	6.86	----					

MECHANICAL OUTLINE

PRINT VERSION NOT TO SCALE

TITLE:
TO–272 WIDE BODY
14 LEAD

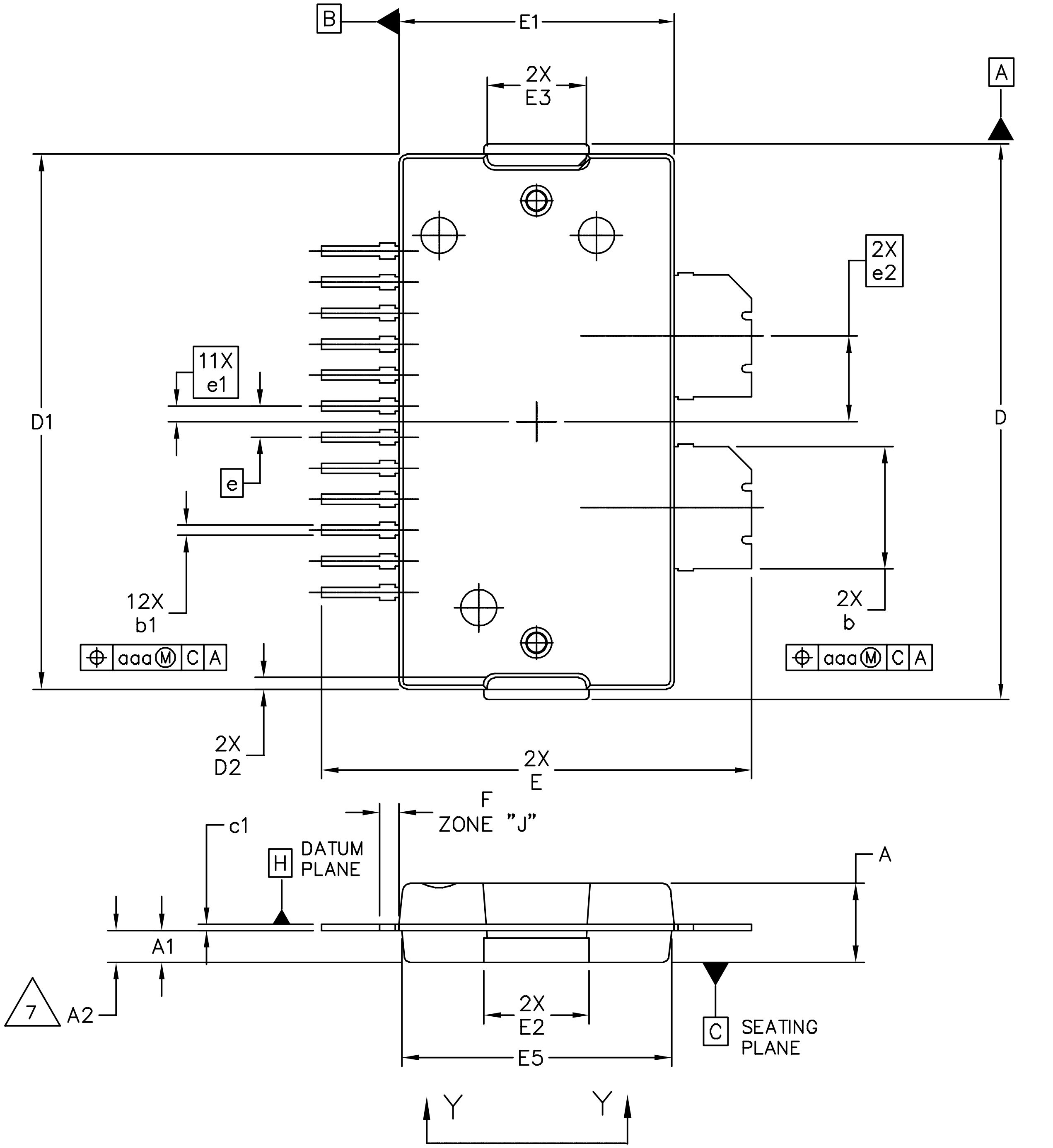
DOCUMENT NO: 98ASA10649D

REV: 0

CASE NUMBER: 1617–01

23 NOV 2005

STANDARD: NON–JEDEC



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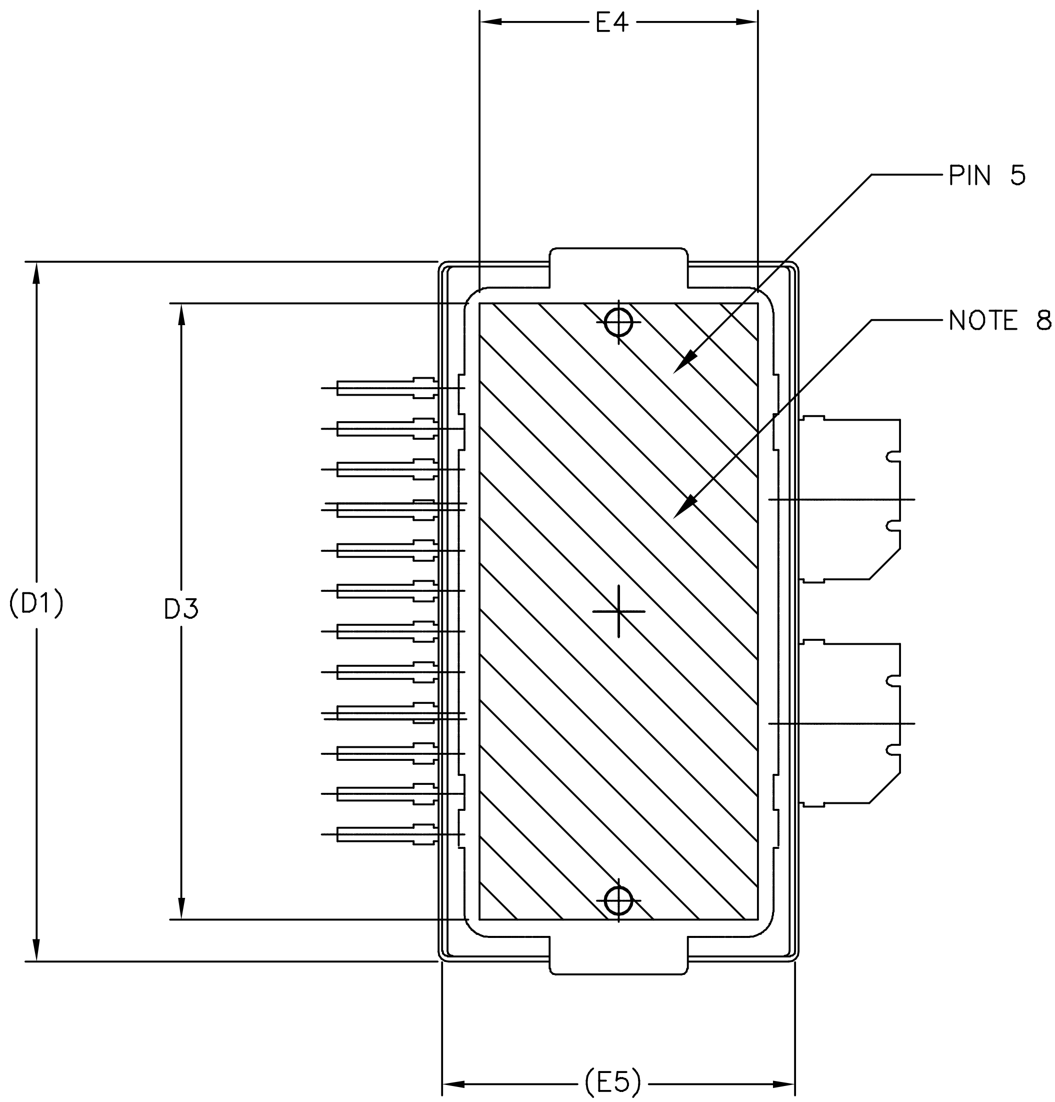
TITLE: TO−270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: 0
	CASE NUMBER: 1618−01	29 SEP 2005
	STANDARD: NON−JEDEC	



MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE
TITLE: TO–270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: 0
	CASE NUMBER: 1618–01	29 SEP 2005
	STANDARD: NON–JEDEC	

NOTES:

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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE

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14 LEAD

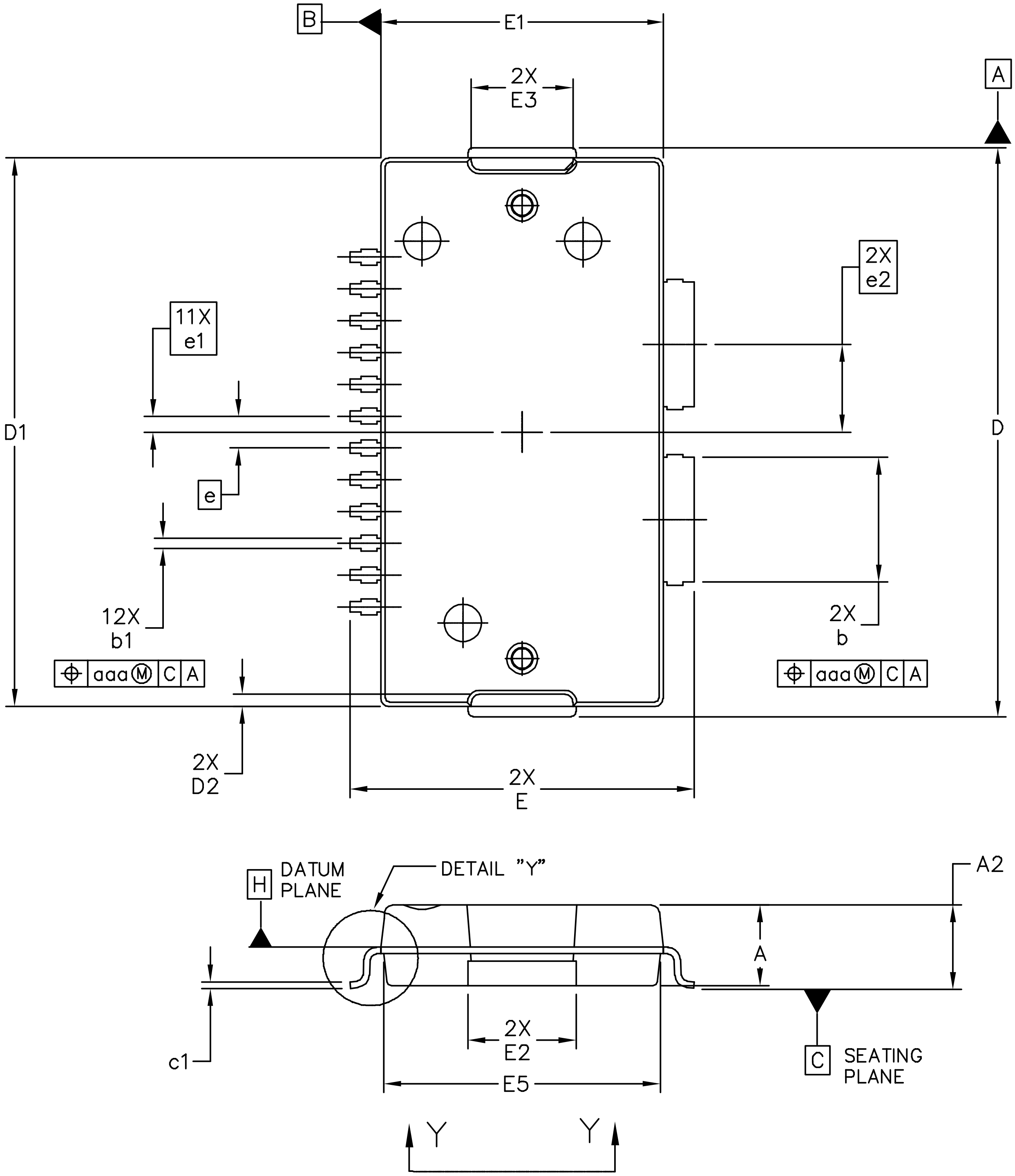
DOOUMENT NO: 98ASA10650D

REV: 0

CASE NUMBER: 1618–01

29 SEP 2005

STANDARD: NON–JEDEC



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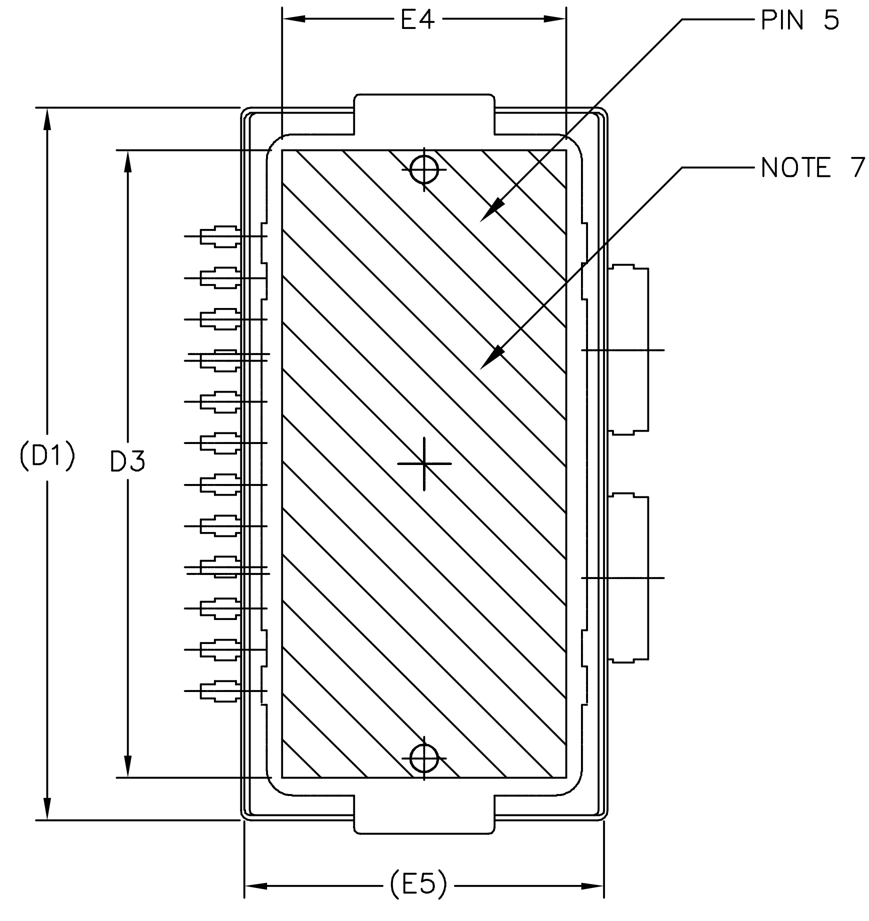
	CASE NUMBER: 1621-01	30 SEP 2005
	STANDARD: NON-JEDEC	



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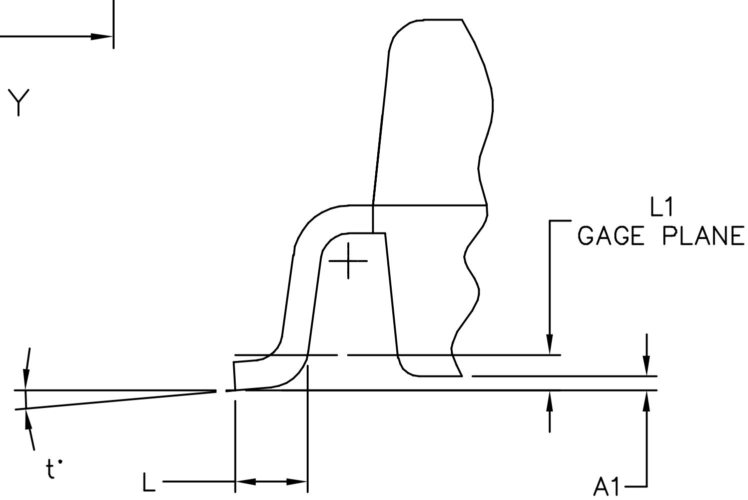

DETAIL "Y"

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5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.040 BSC		1.02 BSC	
D3	.600	−−−	15.24	−−−	e1	.020 BSC		0.51 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

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TITLE: TO−270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: 0
	CASE NUMBER: 1621−01	30 SEP 2005
	STANDARD: NON−JEDEC	

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2007	• Initial Release of Data Sheet
1	June 2007	• Removed Case Operating Temperature from Maximum Ratings table, p. 2. Case Operating Temperature rating will be added to the Maximum Ratings table when parts' Operating Junction Temperature is increased to 225°C.

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