

SN74LS253

Dual 4-Input Multiplexer with 3-State Outputs

The LSTTL/MSI SN74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (\bar{E}_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all ON Semiconductor TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

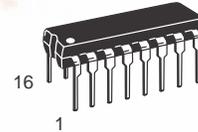
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	4.75	5.0	5.25	V
T _A	Operating Ambient Temperature Range	0	25	70	°C
I _{OH}	Output Current – High			-2.6	mA
I _{OL}	Output Current – Low			24	mA



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**LOW
POWER
SCHOTTKY**



**PLASTIC
N SUFFIX
CASE 648**



**SOIC
D SUFFIX
CASE 751B**

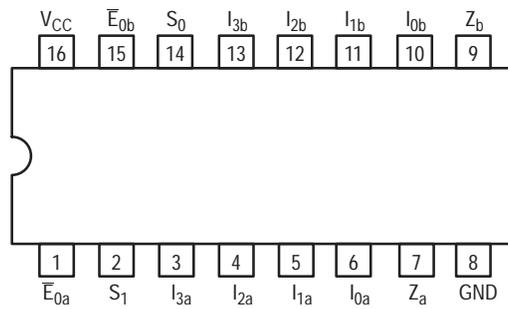
ORDERING INFORMATION

Device	Package	Shipping
SN74LS253N	16 Pin DIP	2000 Units/Box
SN74LS253D	16 Pin	2500/Tape & Reel



SN74LS253

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S_0, S_1 Common Select Inputs

Multiplexer A

\bar{E}_{0a} Output Enable (Active LOW) Input

$I_{0a} - I_{3a}$ Multiplexer Inputs

Z_a Multiplexer Output

Multiplexer B

\bar{E}_{0b} Output Enable (Active LOW) Input

$I_{0b} - I_{3b}$ Multiplexer Inputs

Z_b Multiplexer Output

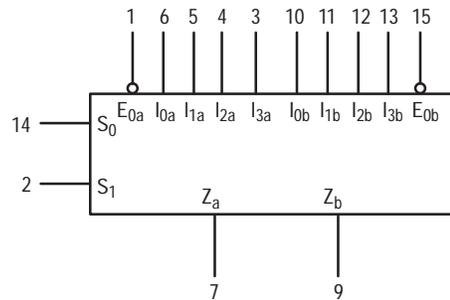
LOADING (Note a)

	HIGH	LOW
S_0, S_1	0.5 U.L.	0.25 U.L.
\bar{E}_{0a}	0.5 U.L.	0.25 U.L.
$I_{0a} - I_{3a}$	0.5 U.L.	0.25 U.L.
Z_a	65 U.L.	15 U.L.
\bar{E}_{0b}	0.5 U.L.	0.25 U.L.
$I_{0b} - I_{3b}$	0.5 U.L.	0.25 U.L.
Z_b	65 U.L.	15 U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

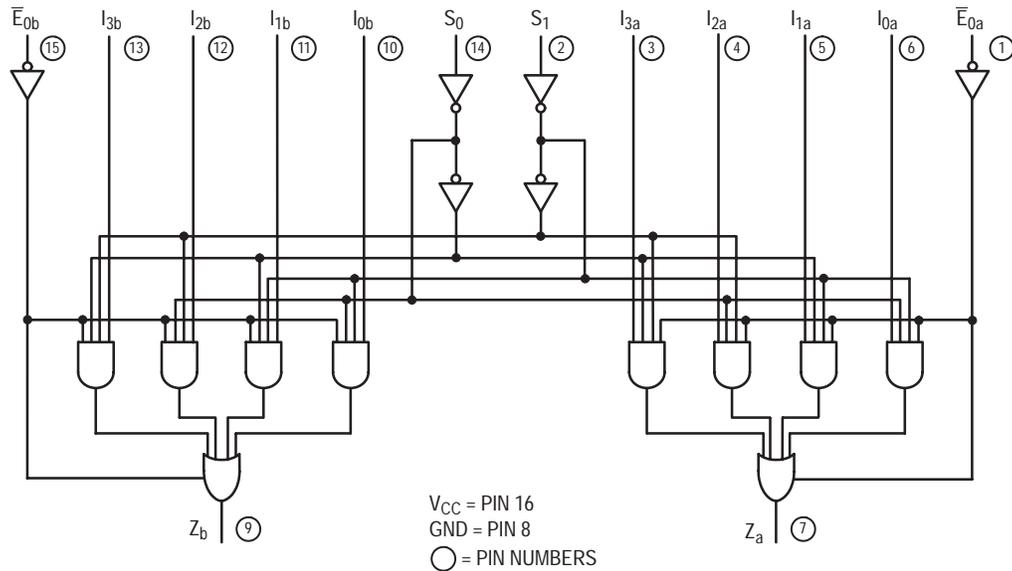
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN74LS253

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\bar{E}_{0a}, \bar{E}_{0b}$) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	\bar{E}_0	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level

L = LOW Level

X = Irrelevant

(Z) = High Impedance (off)

Address inputs S_0 and S_1 are common to both sections.

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	2.4	3.1		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 12 \text{ mA}$	$V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
			0.35	0.5	V	$I_{OL} = 24 \text{ mA}$	
I_{OZH}	Output Off Current HIGH			20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 2.7 \text{ V}$	
I_{OZL}	Output Off Current LOW			-20	μA	$V_{CC} = \text{MAX}$, $V_{OUT} = 0.4 \text{ V}$	
I_{IH}	Input HIGH Current			20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
				0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Short Circuit Current (Note 1)	-30		-130	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			12	mA	$V_{CC} = \text{MAX}$, $\overline{V_E} = 0 \text{ V}$	
				14	mA	$V_{CC} = \text{MAX}$, $\overline{V_E} = 4.5 \text{ V}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

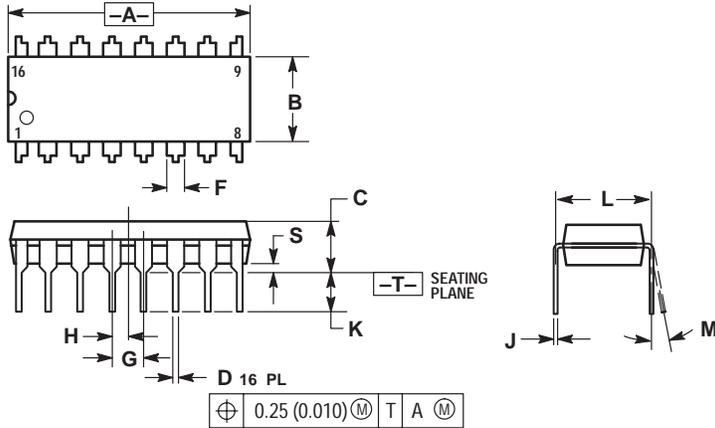
AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$) See SN74LS251 for Waveforms

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		17 13	25 20	ns	Figure 1	$C_L = 45 \text{ pF}$, $R_L = 667 \Omega$
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		30 21	45 32	ns	Figure 1	
t_{PZH} t_{PZL}	Output Enable Time		15 15	28 23	ns	Figures 4, 5	
t_{PHZ} t_{PLZ}	Output Disable Time		27 18	41 27	ns	Figures 3, 5	

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PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



NOTES:

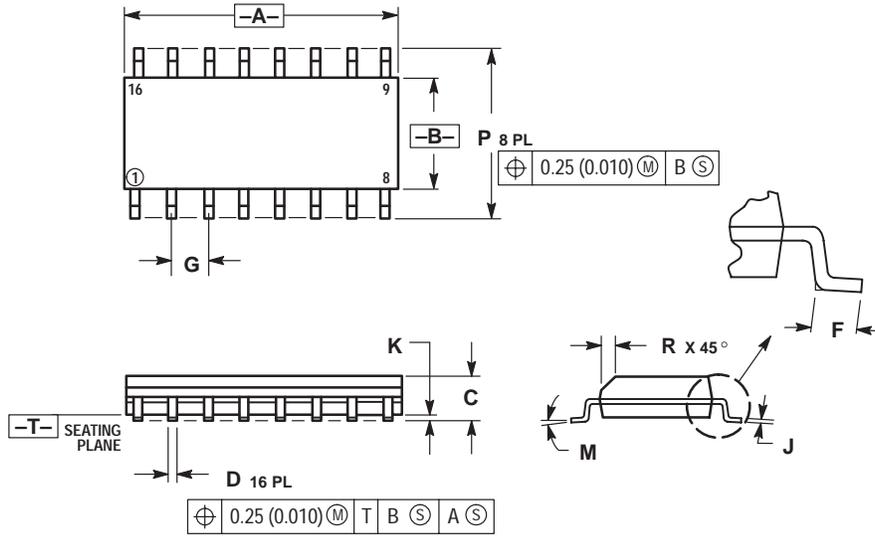
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05
ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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Notes

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