

TOSHIBA

TMP86CH06

CMOS 8-Bit Microcontroller

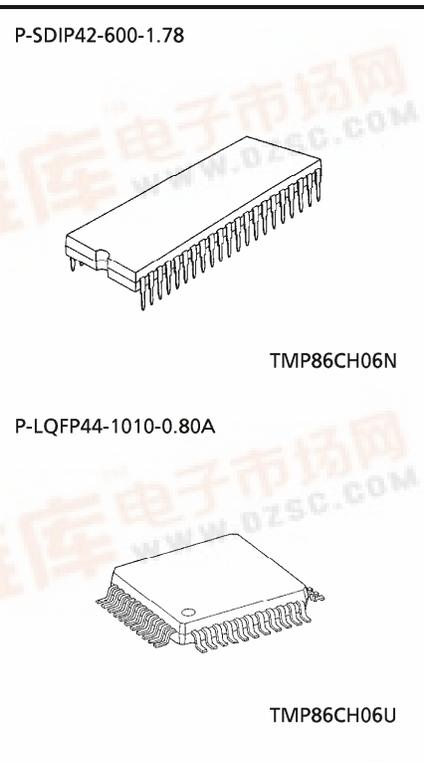
TMP86CH06N/TMP86CH06U

The TMP86CH06 is the 8-bit single chip microcomputer, which contains ROM, RAM, multi-function timer/counters, serial interface (UART/SIO) with high speed, high performance and low power consumption.

Product No.	ROM	RAM	Package	OTP MCU
TMP86CH06N	16K x 8-bit	512 x 8-bit	P-SDIP42-600-1.78	TMP86PH06N
TMP86CH06U			P-LQFP44-1010-0.80A	TMP86PH06U

Features

- ◆ 8-bit single chip microcomputer TLCS-870/C Series
- ◆ Minimum Instruction execution time: 0.25 μ s (at 16.0 MHz)
 - Power consumption is reducible by means of conversion of instruction execution time
0.25 μ s, 0.50 μ s, 1.0 μ s, 2.0 μ s, 4.0 μ s, 8.0 μ s, 122 μ s (at 16.0 MHz, 32.768 kHz operation)
- ◆ External Bus Interface
 - up to 64 Kbytes (for both Program and Data memory)
 - Multiplexed between Lower Address-bus and Data-bus
- ◆ 21 Interrupt factors (6 for External, 15 for Internal)
- ◆ Input/Output Ports: 35 pins
 - High-Current Output (Typ. 20 mA, LED direct drive): 8 pins
- ◆ 16-bit Timer/Counter: 1 channel
 - Timer, Event counter, Pulse Width measurement and External-triggered timer



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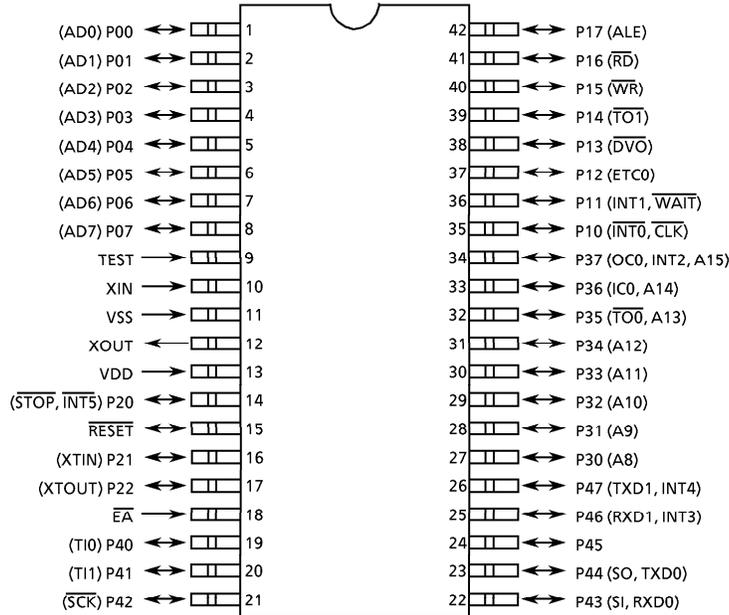
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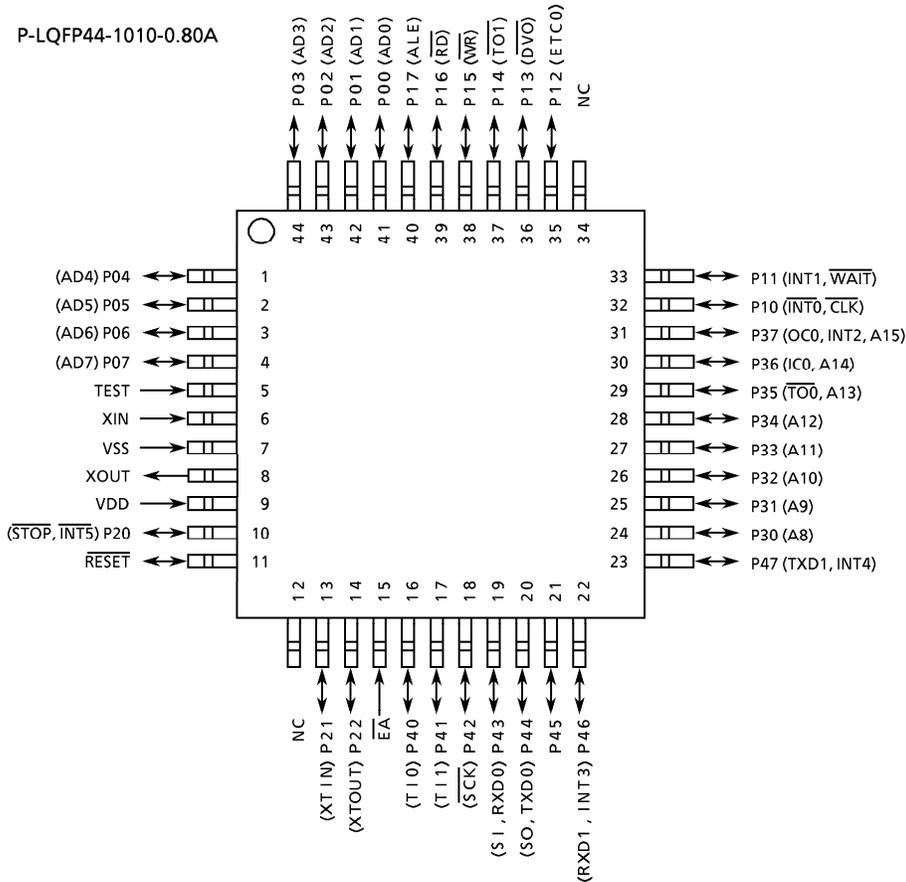
- ◆ 8-bit Timer/Counter: 2 channels
 - Available for 16-bit timer by cascade connection
 - Timer, Event counter, Pulse Width Modulation, Programmed Pulse Generator and Programmable Divider Output, Warming-up Counter
- ◆ Serial Interface
 - 8-bit UART: 2 channels
 - 8-bit SIO (synchronized): 1 channel
- ◆ Clock Oscillation circuit: 2 units
 - For Single or Dual clock mode
- ◆ Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCCR < TBTCK > setting.
 - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
 - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
 - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by falling edge of TBTCCR < TBTCK > setting.
 - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
 - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- ◆ Operating Voltage: 4.5 to 5.5 V at 16.0 MHz/32.768 kHz, 2.7 to 5.5 V at 8 MHz/32.768 kHz, 1.8 to 5.5 V at 4.2 MHz/32.768 kHz.

Pin Assignments (Top View)

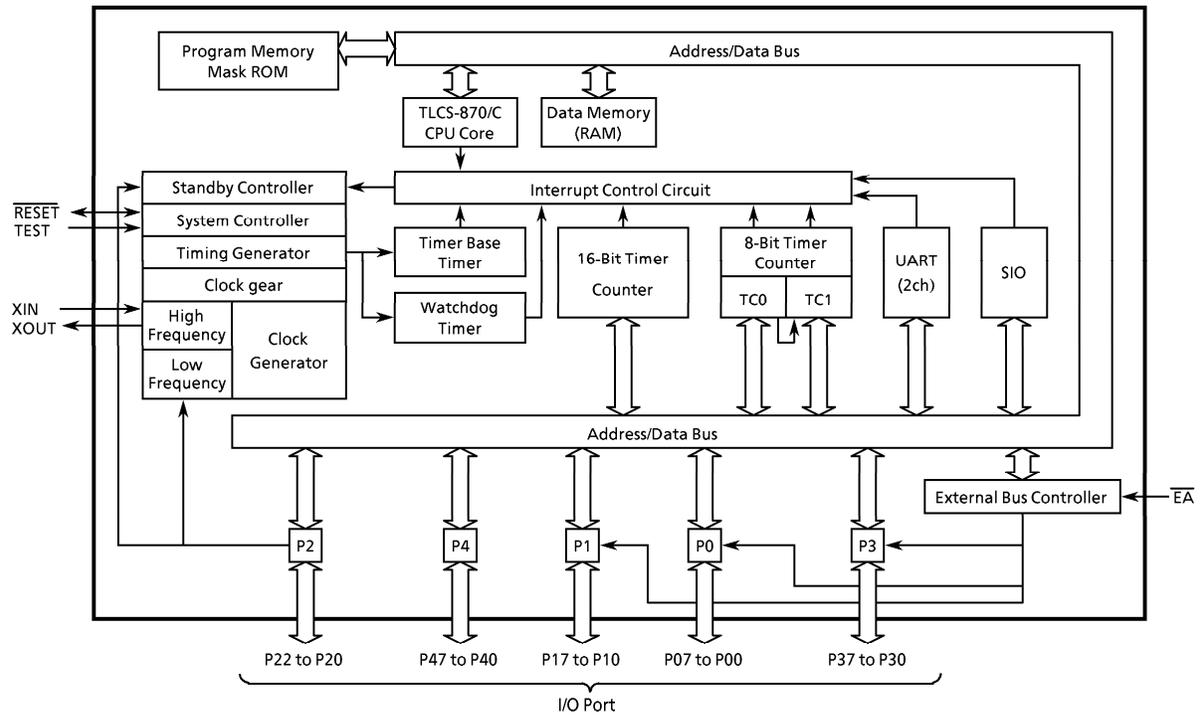
P-SDIP42-600-1.78



P-LQFP44-1010-0.80A



Block Diagram



Pin Names And Functions (1/3)

Pin Name	No. of Pins	Input/Output	Functions
P00 to P07 AD0 to AD7	8	I/O 3-states	Port 0: 8-bit I/O port that allows selection of input/output on bit basis. Address/Data bus: Functions as 8-bit bidirectional address/data bus for external memory (TTL input).
P10 $\overline{\text{INT0}}$ CLK	1	I/O Input Output	Port 10: I/O port that allows selection of input/output on bit basis. } (Schmidt Input) External Interrupt Request 0 Clock: Clock output
P11 INT1 $\overline{\text{WAIT}}$	1	I/O Input Input	Port 11: I/O port that allows selection of input/output on bit basis. } (Schmidt Input) External Interrupt Request 1 Wait: Wait request from external Memory
P12 ETC0	1	I/O Input	Port 12: I/O port that allows selection of input/output on bit basis. } (Schmidt Input) Extended Timer Input 0
P13 $\overline{\text{DVO}}$	1	I/O Output	Port 13: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Divider Output
P14 $\overline{\text{TO1}}$	1	I/O Output	Port 14: I/O port that allows selection of input/output on bit basis. (Schmidt Input) 8-bit Timer 1 Output
P15 $\overline{\text{WR}}$	1	I/O Output	Port 15: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Write: Generates strobe signal to write data on External Memory.
P16 $\overline{\text{RD}}$	1	I/O Output	Port 16: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Read: Generates strobe signal to read data from External Memory.
P17 ALE	1	I/O Output	Port 17: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Address Latch Enable: The negative edge of ALE supplies an address latch timing on AD0 to AD7 for External Memory.
P20 $\overline{\text{STOP}}$ $\overline{\text{INT5}}$	1	I/O Input Input	Port 20: I/O port that allows selection of input/output on bit basis. Open-Drain Output. } (Schmidt Input) STOP Releasing: The rising edge or High Level Releases STOP mode. External Interrupt Request 5
P21 XTIN	1	I/O Input	Port 21: I/O port that allows selection of input/output on bit basis. Open-Drain Output. } (Schmidt Input) Low Frequency Clock Input
P22 XTOUT	1	I/O Output	Port 22: I/O port that allows selection of input/output on bit basis. Open-Drain Output. } (Schmidt Input) Low Frequency Clock Output
P30 to P34 A8 to A12	5	I/O Output	Port 30 to 34: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Address Bus 8 to 12

Pin Names And Functions (2/3)

Pin Name	No. of Pins	Input/Output	Functions
P35 $\overline{TO0}$ A13	1	I/O Output Output	Port 35: I/O port that allows selection of input/output on bit basis. (Schmidt Input) 8-bit Timer Output 0 Address Bus 13
P36 IC0 A14	1	I/O Input Output	Port 36: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Capture Input 0 for Extended Timer Address Bus 14
P37 OC0 INT2 A15	1	I/O Output Input Output	Port 37: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Output Compare 0 for Extended Timer External Interrupt Request 2 (Schmidt Input) Address Bus 15
P40 TI0	1	I/O Input	Port 40: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. (Schmidt Input) 8-bit Timer Input 0
P41 TI1	1	I/O Input	Port 41: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. (Schmidt Input) 8-bit Timer Input 1
P42 \overline{SCK}	1	I/O I/O	Port 42: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. (Schmidt Input) Clock input/output for SIO
P43 SI, RXD0	1	I/O Input	Port 43: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. (Schmidt Input) Data Input for UART/SIO channel 0
P44 \overline{SO} , TXD0	1	I/O Output	Port 44: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Data Output for UART/SIO channel 0. Programmable Open-Drain Output.
P45	1	I/O	Port 45: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output.
P46 RXD1 INT3	1	I/O Input Input	Port 46: I/O port that allows selection of input/output on bit basis. Programmable Open-Drain Output. (Schmidt Input) Data Input for UART channel 1 External Interrupt Request 3
P47 TXD1 INT4	1	I/O Output Input	Port 47: I/O port that allows selection of input/output on bit basis. (Schmidt Input) Data Output for UART channel 1. Programmable Open-Drain Output. External Interrupt Request 4 (Schmidt Input)

Pin Names And Functions (3/3)

Pin Name	No. of Pins	Input/Output	Functions
\overline{EA}	1	Input	External Access: Fix to HIGH level to utilize internal ROM. Fix to LOW level to utilize external memory.
TEST	1	Input	to be fixed to LOW level
\overline{RESET}	1	I/O	RESET signal input or watchdog timer output/address trap output/system-clock-reset-output
XIN/XOUT	2	I/O	High-frequency resonator is to be connected.
VSS	1	Input	Ground
VDD	1	Input	Power Supply

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Maps

The TMP86CH06 memory consists of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64K-byte address space. Figure 1-1 shows the TMP86CH06 memory address maps. The general-purpose register banks are not assigned to the RAM address space.

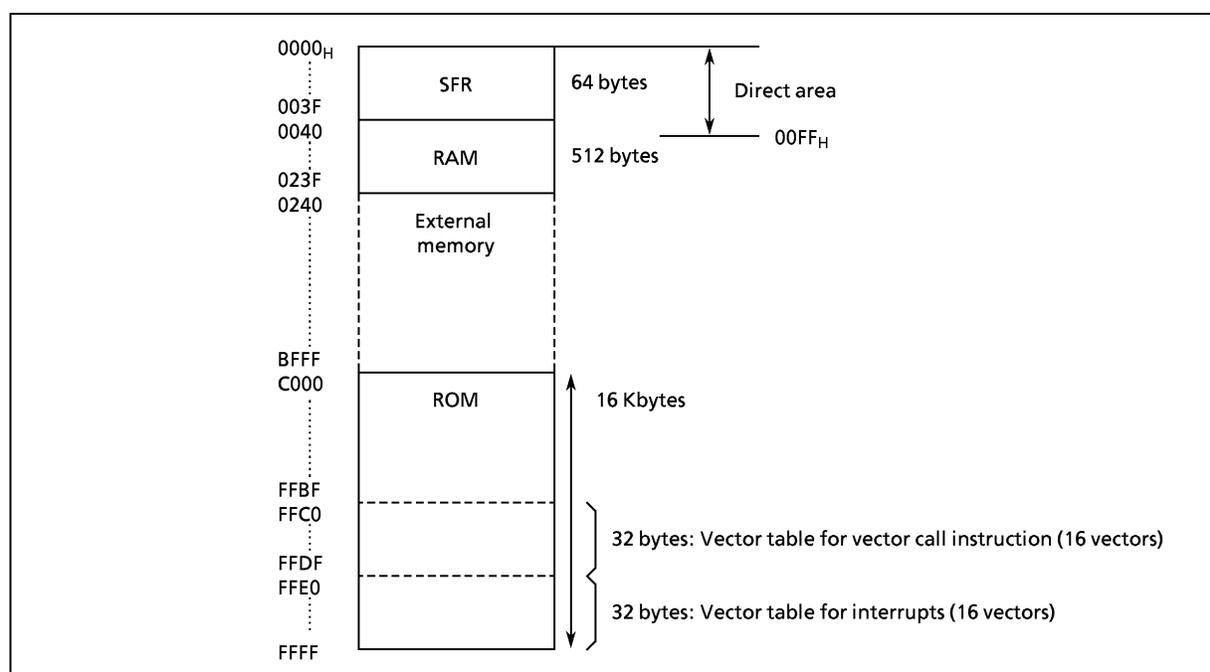


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CH06 can address up to 64 Kbytes of external program memory space except the SFR area and the internal RAM. However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap). The TMP86CH06 contains a 16-Kbyte program memory (mask ROM) at addresses from C000_H to FFFF_H.

1.3 Data Memory (RAM)

The TMP86CH06 is available up to 64 Kbytes of data memory area. Data memory consists of internal data memory (internal ROM or RAM) and external data memory (ROM or RAM). The TMP86CH06 has 512 bytes of internal RAM. The first 192 bytes (0040_H to 00FF_H) of the internal RAM are located in the direct area; instructions with shorten operations are available against such an area.

Electrical Characteristics

Absolute Maximum Rating

 $(V_{SS} = 0\text{ V})$

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		- 0.3 to 6.5	V
Input Voltage	V_{IN}		- 0.3 to $V_{DD} + 0.3$	
Output Voltage	V_{OUT}		- 0.3 to $V_{DD} + 0.3$	
Output Current	I_{OUT1}	P1 to P4	3.2	mA
	I_{OUT3}	P0	30	
Output Current	ΣI_{OUT1}		80	
	ΣI_{OUT3}		120	
Power Dissipation ($T_{opr} = 85^{\circ}\text{C}$)	PD	TMP86CH06N	600	mW
		TMP86CH06U	350	
Soldering Temperature (Time)	T_{sld}		260 (10 s)	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		- 55 to 125	
Operating Temperature	T_{opr}		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = - 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit	
Supply Voltage	V _{DD}		f _c = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			f _c = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			f _c = 4.2 MHz	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
f _s = 32.768 kHz	SLOW1, 2 mode	1.8					
	SLEEP0, 1, 2 mode						
		STOP mode	1.8				
Input High Voltage	V _{IH1}	Except hysteresis and TTL input	V _{DD} ≥ 4.5 V	V _{DD} × 0.70	V _{DD}	V	
	V _{IH2}	Hysteresis input		V _{DD} × 0.75			
	V _{IH3}	Except TTL input	V _{DD} < 4.5 V	V _{DD} × 0.90			
	V _{IH4}	TTL input (Data bus)	V _{DD} = 5 V	2.2			
	V _{IH5}		V _{DD} = 1.8 V	V _{DD} - 0.2			
Input Low Voltage	V _{IL1}	Except hysteresis and TTL input	V _{DD} ≥ 4.5 V	0	V _{DD} × 0.30	V	
	V _{IL2}	Hysteresis input		V _{DD} × 0.25			
	V _{IL3}	Except TLL input	V _{DD} < 4.5 V	V _{DD} × 0.10			
	V _{IL4}	TTL input (Data bus)	V _{DD} = 5 V	0.8			
	V _{IL5}		V _{DD} = 1.8 V	0.2			
Clock Frequency	f _c	XIN, XOUT	V _{DD} = 4.5 V to 5.5 V	1.0	16	MHz	
			V _{DD} = 2.7 V to 5.5 V		8		
			V _{DD} = 1.8 V to 5.5 V		4.2		
	f _s	XTIN, XTOUT		30.0	34.0	kHz	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock Frequency f_c; The condition of supply voltage range is the value under NORMAL1/2 and IDLE0/1/2 mode.

Note 3: The minimum f_c with clock gear is calculated as following formula with the ratio on divider n.
(Min f_c) = (ratio on divider n) × 1 [MHz]

DC Characteristics

(V_{SS} = 0 V, T_{opr} = -40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input		-	0.9	-	V
Input Current	I _{IN1}	TEST, \overline{EA}	V _{DD} = 5.5 V V _{IN} = 5.5 V/0 V	-	-	± 2	μA
	I _{IN2}	Sink Open Drain, Tri-state Port					
	I _{IN3}	RESET, \overline{STOP}					
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
	R _{IN3}	TEST		-	70	-	
OSC. Feedback Resistance	R _{fx}	XIN-XOUT		-	1.2	-	MΩ
	R _{fxT}	XTIN-XTOUT		-	6	-	
Output Leakage Current	I _{LO1}	Sink Open Drain Port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	-	-	2	μA
	I _{LO2}	Tri-state Port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	-	-	± 2	
"H" Output Voltage	V _{OH2}	Tri-state Port	V _{DD} = 4.5 V, I _{OH} = -0.7 mA	4.1	-	-	V
"L" Output Voltage	V _{OL3}	Except P0 and XOUT	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	-	-	0.4	V
"L" Output Current	I _{OL1}	Except P0 and XOUT	V _{DD} = 4.5 V, V _{OL} = 0.4 V	1.6	-	-	mA
	I _{OL3}	P0	V _{DD} = 4.5 V, V _{OL} = 1.0 V	-	20	-	
Supply Current under NORMAL1, 2 mode	I _{DD}		V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	5.5	7.0	mA
Supply Current under IDLE1, 2 mode			f _c = 16 MHz f _s = 32.768 kHz	-	2.8	3.5	
Supply Current under NORMAL1, 2 mode			V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	4.0	5.0	mA
Supply Current under IDLE1, 2 mode			f _c = 8 MHz f _s = 32.768 kHz	-	2.0	2.5	
Supply Current under SLOW1 mode			V _{DD} = 3.0 V V _{IN} = 2.8 V/0.2 V f _s = 32.768 kHz	-	14	25	μA
Supply Current under SLEEP1 mode				-	7.0	15	μA
Supply Current under SLEEPO mode				-	6.0	15	μA
Supply Current under STOP mode			V _{DD} = 5.5 V V _{IN} = 5.3 V/0.2 V	-	0.5	10	μA

Note 1: Typical values are shown under T_{opr} = 25°C, V_{DD} = 5 V, while conditions are not stated.

Note 2: Input current I_{IN1}, I_{IN3}: The current through pull-up or pull-down resistor is not included.

AC Characteristics

(1) (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = -40 to 85°C)

① CLOCK

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL1, 2 mode	0.25	-	4	μs
		IDLE0, 1, 2 mode				
		SLOW1, 2 mode	117.6	-	133.3	
		SLEEPO, 1, 2 mode				
High Level Clock Pulse Width	t _{WCH}	External clock operation (XIN input)	25	-	-	ns
Low Level Clock Pulse Width	t _{WCL}	f _c = 16 MHz				
High Level Clock Pulse Width	t _{WSH}	External clock operation (XTIN input)	14.7	-	-	μs
Low Level Clock Pulse Width	t _{WSL}	f _s = 32.768 kHz				

② External Memory Interface (Multiplexed Bus) at $V_{DD} = 4.5$ to 5.5

No.	Symbol	Parameter	Variable		16 MHz		Unit
			Min	Max	Min	Max	
1	t_{AL}	A7 to 0 effective \rightarrow ALE	0.5t – 15		16		ns
2	t_{LA}	ALE fall \rightarrow A7 to 0 hold	0.5t – 20		11		ns
3	t_{LL}	ALE pulse width	t – 40		22		ns
4	t_{LC}	ALE fall \rightarrow \overline{RD} , \overline{WR} fall	0.5t – 25		6		ns
5	t_{CL}	\overline{RD} , \overline{WR} rise \rightarrow ALE rise	0.5t – 20		11		ns
6	t_{ACL}	A7 to 0 effective \rightarrow \overline{RD} , \overline{WR} fall	t – 25		37		ns
7	t_{ACH}	A15 to 8 effective \rightarrow \overline{RD} , \overline{WR} fall	1.5t – 25		68		ns
8	t_{CA}	\overline{RD} , \overline{WR} rise \rightarrow A15 to 8 hold	0.5t – 20		11		ns
9	t_{ADL}	A7 to 0 effective \rightarrow D7 to 0 input		3t – 55		132	ns
10	t_{ADH}	A15 to 8 effective \rightarrow D7 to 0 input		3.5t – 65		153	ns
11	t_{RD}	\overline{RD} fall \rightarrow D7 to 0 input		2t – 60		65	ns
12	t_{RR}	\overline{RD} pulse width	2t – 40		85		ns
13	t_{HR}	\overline{RD} rise \rightarrow D7 to 0 hold	0		0		ns
14	t_{RAE}	\overline{RD} rise \rightarrow A7 to 0 effective	t – 15		47		ns
15	t_{WV}	\overline{WR} pulse width	2t – 40		85		ns
16	t_{DW}	D7 to 0 effective \rightarrow \overline{WR} rise	2t – 40		85		ns
17	t_{WD}	\overline{WR} rise \rightarrow D7 to 0 hold	0.5t – 15		16		ns

Note: $t = t_{cy}/4$ ($t = 62.5$ ns at $f_{cgck} = 16$ MHz)

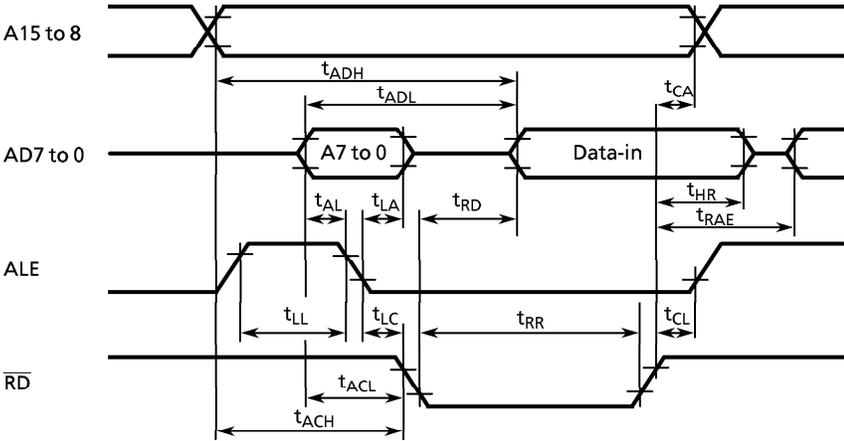
A.C. Measurement Condition

Output Level: High 2.2 V/Low 0.8 V, CL = 50 pF

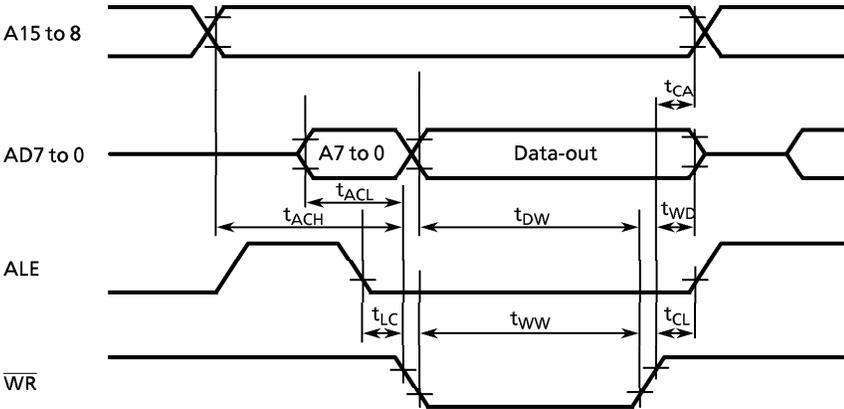
Input Level: High 2.4 V/Low 0.4 V (D7 to D0)

High 0.8 VDD/Low 0.2 VDD (Except D7 to D0)

Read Cycle



Write Cycle



Recommended Oscillating Conditions - 1

($V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF		
		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF

Recommended Oscillating Conditions - 2

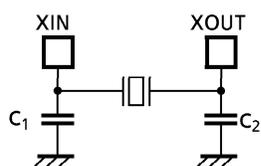
($V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		

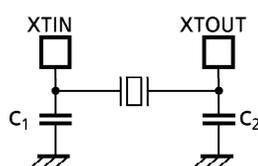
Recommended Oscillating Conditions - 3

($V_{SS} = 0\text{ V}$, $V_{DD} = 1.8\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

<http://www.murata.co.jp/search/index.html>

