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ApNote AP1616

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Software Modifications of Register WDTCON

The time period which is monitored by the Watchdog Timer is programmable via register WDTCON in two ways...

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Software Modifications of Register WDTCON

The time period which is monitored by the Watchdog Timer is programmable via register WDTCON in two ways:

- bit **WDTIN** allows selection of the prescaler factor for the input clock to the Watchdog Timer
- bit field **WDTREL** in the high byte of WDTCON represents the 8-bit reload value for the high byte of the Watchdog Timer Register WDT

This results in the following range for the monitored time period:

	Monitored Time Period in TCL / @ 20 MHz	
Reload Value WDTREL	WDTIN = 0	WDTIN = 1
0FFh	1024 TCL / 25.6 µs	64 * 1024 TCL = 65536 TCL / 1.6 ms
00h	256 * 1024 TCL = 262144 TCL / 6.55 ms	64 * 256 * 1024 TCL = 16 777 216 TCL / 419 ms

Software modifications of register WDTCON may be performed at any time during program execution, however, modifications of WDTIN and WDTREL will become effective at different times:

A change of bit **WDTIN** will immediately (at the end of the execute phase of the instruction which writes to WDTCON) switch the clock input for the Watchdog Timer to the selected prescaled CPU clock. This means that when changing WDTIN from 0 to 1 (fast to slow clock), the Watchdog Timer will get the next clock tick within the next 0 .. 1024 TCL. When changing WDTIN from 1 to 0 (slow to fast clock), the Watchdog Timer will get the next clock tick within the next 0 .. 4 TCL.

When bit field **WDTREL** is modified, the new value will not be transferred into the high byte of WDT until either the Watchdog Timer overflows or the SRVWDT (Service Watchdog Timer) instruction is executed. Therefore, if an immediate transfer of WDTREL into the high byte of WDT is desired, SRVWDT must be executed after WDTREL has been written to WDTCON.