PROGRAMMABLE PORT CONTROLLER (PORT EXPANDER WITH BUILT-IN E^2PROM CIRCUIT)

S-7750B

The S-7750B is a programmable port controller IC comprising E^2PROM, a data output controller, a circuit to prevent malfunction during low supply voltage, etc.
It operates at 400 kHz and interfaces with external devices via the I^2CBUS. High and low of the 8-channel digital output, and the delay time of each channel can be controlled by serial signals.
Initial value, and reverse delay time can be set for the 8-channel digital output pins, respectively for each port. This is effective for controlling turning on or off the voltage regulator in mobile phones.
The built-in E^2PROM allows the initial value of each control setting to be retained when power is off.

■ Features

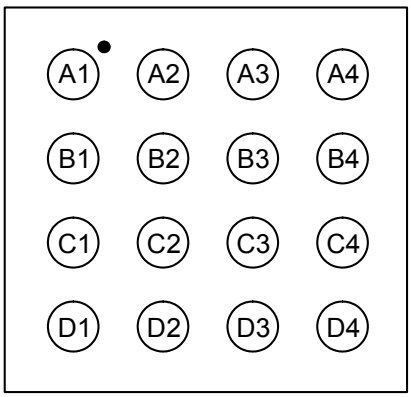
- Operating voltage range: 2.3 V to 4.5 V
- 8-channel digital output
- Operating frequency: 400 kHz
- Malfunction prevention function at low supply voltage
- Low current consumption During standby: 3.0 μA max. (V_{CCH} = 4.5 V)
- Built-in E^2PROM circuit
- E^2PROM endurance: 10^5 cycles (at −40 to +85°C)
- E^2PROM write protect function
- Lead-free products

■ Package

Package Name	Drawing Code		
	Package	Tape	Reel
WLP-16A	HA016-A	HA016-A	HA016-A

■ Pin Assignments

WLP-16A
Bottom view



(1.93×2.07×0.6 max.)

Figure 1

Table 1

Pin Number	Pin Name	Function	Pin Number	Pin Name	Function
A1	CLK	External clock input	C1	DO6	Output port 6
A2	SCL	Serial clock input	C2	TIMEN	Timer enable input
A3	WP	Write protect input	C3	DO3	Output port 3
A4	VCCH	Power supply	C4	DO1	Output port 1
B1	DO7	Output port 7	D1	DO5	Output port 5
B2	VSS	Ground	D2	DO4	Output port 4
B3	SDA	Serial data I/O	D3	VCCL	Power supply for output port
B4	DO0	Output port 0	D4	DO2	Output port 2

■ Block Diagram

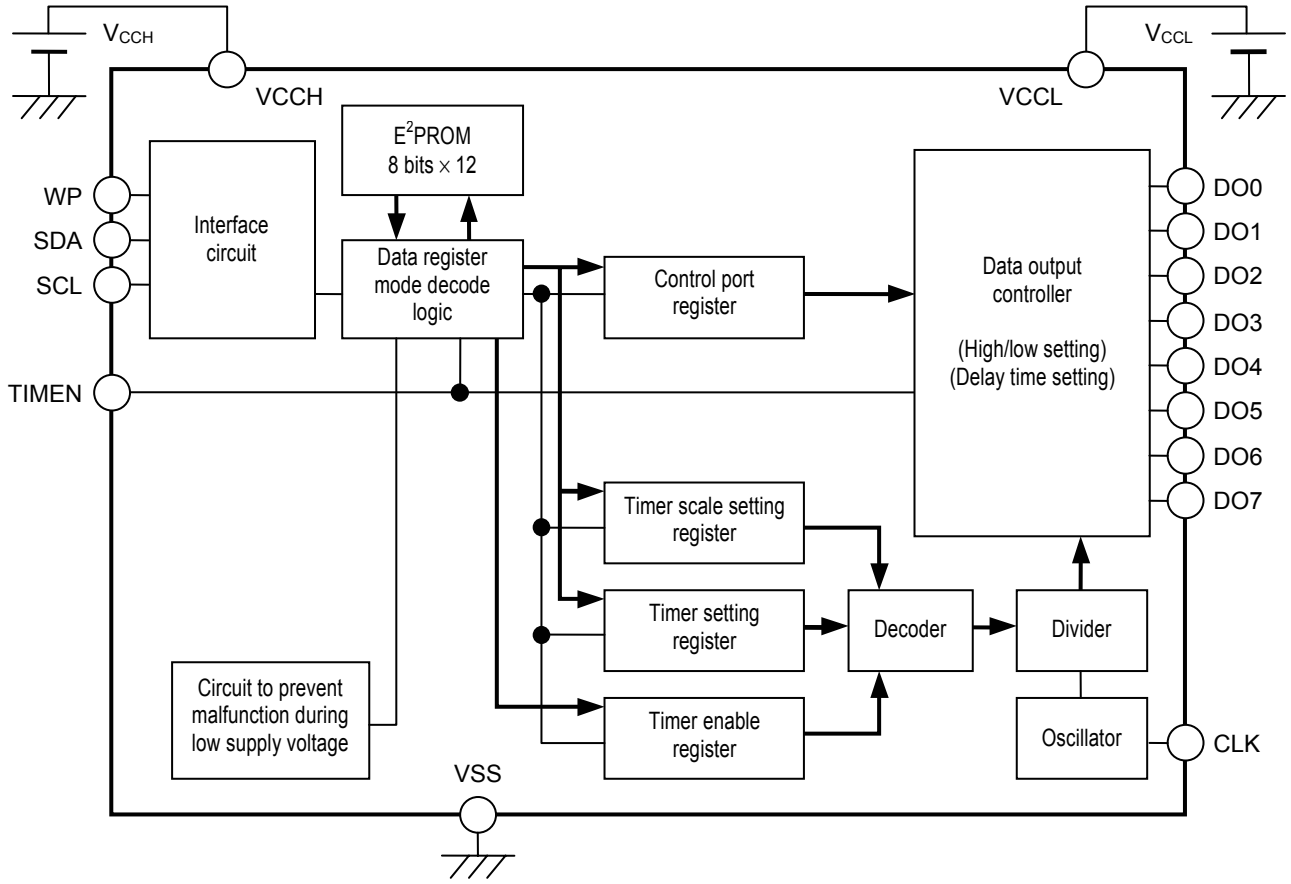


Figure 2

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage1	V_{CCH}	−0.3 to +7.0	V
Power supply voltage2	V_{CCL}	−0.3 to V_{CCH}	V
Input voltage	V_{IN}	−0.3 to V_{CCH} + 0.3	V
Output voltage (SDA)	V_{OUT1}	−0.3 to V_{CCH}	V
Output voltage (DO)	V_{OUT2}	−0.3 to V_{CCL}	V
Operating ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable Pin
Supply voltage 1	V_{CCH}	Write and read	2.3*1	—	4.5	V	VCCH
Supply voltage 2	V_{CCL}	—	1.5	—	V_{CCH}*2	V	VCCL
High-level input voltage	V_{IH}	V_{CCH} = 2.3 to 4.5 V	0.7 × V_{CCH}	—	V_{CCH}	V	WP, TIMEN, SDA, SCL, CLK
Low-level input voltage	V_{IL}	V_{CCH} = 2.3 to 4.5 V	0.0	—	0.3 × V_{CCH}	V	WP, TIMEN, SDA, SCL, CLK

***1.** V_{CCH} must be 2.5 V or higher if VCCH and TIMEN are input simultaneously.
***2.** The voltage of VCCL must be that of V_{CCH} or lower.

■ Pin Capacitance

Table 4

(Ta = 25°C, f = 1.0 MHz, V_{CCH} = 3 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, WP, TIMEN, CLK)	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA, DO)	—	—	10	pF

■ Endurance

Table 5

Parameter	Symbol	Operating Temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^5	—	—	Cycles/word

■ DC Electrical Characteristics

Table 6

Parameter	Symbol	V_{CCH} = 2.3 V to 4.5 V f = 400 kHz			Unit
		Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	—	—	0.8	mA
Current consumption (WRITE)	I_{CC2}	—	—	4.0	mA
Current consumption while internal oscillator is operating	I_{CC3}	—	—	0.8	mA

Table 7

Parameter	Symbol	Condition	V_{CCH} = 2.3 V to 4.5 V			Unit
			Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CCH} or GND	—	—	3.0	µA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CCH}	—	0.1	1.0	µA
Output leakage current (SDA)	I_{LO}	V_{OUT} = GND to V_{CCH}	—	0.1	1.0	µA
Low-level output voltage (SDA)	V_{OL1}	I_{OL} = 3.2 mA	—	—	0.4	V
		I_{OL} = 1.5 mA	—	—	0.3	V
Low-level output voltage (DO)	V_{OL2}	I_{OL} = 100 µA V_{CCL} = V_{CCH} to 1.5V	—	—	0.1	V
High-level output voltage (DO)	V_{OH2}	V_{CCL} = V_{CCH} to 2.0V I_{OH} = −100 µA	V_{CCL} − 0.3	—	—	V
		V_{CCL} = V_{CCH} to 1.5V I_{OH} = −10 µA	V_{CCL} − 0.3	—	—	V

■ AC Electrical Characteristics

Table 8 Measurement Conditions

Input pulse voltage	$0.1\times V_{CCH}$ to $0.9\times V_{CCH}$
Input pulse rising / falling time	20 ns
Output judgment voltage	$0.5\times V_{CCH}$
Output load	100 pF+ Pull-up resistor 1.0 kΩ

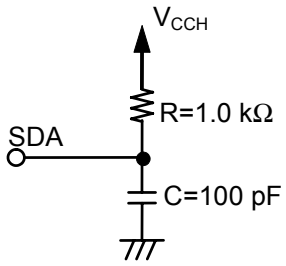


Figure 3 Output Load Circuit

Table 9

Parameter	Symbol	V_{CCH} = 2.3 V to 4.5 V			Unit
		Min.	Typ.	Max.	
SCL, CLK clock frequency	f_{SCL}	0	—	400	kHz
SCL, CLK clock time “L”	t_{LOW}	1.0	—	—	µs
SCL clock time “H”	t_{HIGH}	0.9	—	—	µs
SDA output delay time	t_{AA}	—	—	0.9	µs
SDA output hold time	t_{DH}	50	—	—	ns
Start condition setup time	$t_{SU.STA}$	0.6	—	—	µs
Start condition hold time	$t_{HD.STA}$	0.6	—	—	µs
Data input setup time	$t_{SU.DAT}$	100	—	—	ns
Data input hold time	$t_{HD.DAT}$	0	—	—	ns
Stop condition setup time	$t_{SU.STO}$	0.6	—	—	µs
SCL, SDA, CLK rise time	t_R	—	—	0.3	µs
SCL, SDA, CLK fall time	t_F	—	—	0.3	µs
Bus release time	t_{BUF}	1.3	—	—	µs
Noise suppression time	t_I	—	—	50	ns

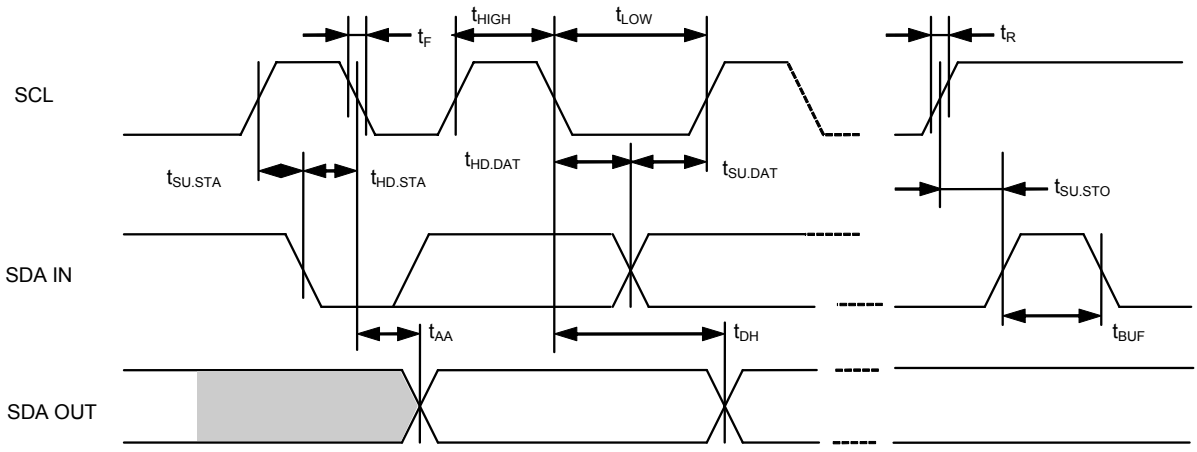


Figure 4 Bus Timing

Table 10

Parameter	Symbol	Min.	Typ.	Max.	Unit
E²PROM Write time	t_{WR}	—	2.0	5.0	ms
Delay time accuracy (short time setting)*1	t_{DLY1}	0.8 × T	T	1.2 × T	μs
Delay time accuracy (long time setting)*1	t_{DLY2}	0.8 × LT	LT	1.2 × LT	μs
Timeout*1	t_{TOUT}	—	9 × LT	—	μs

***1.** Refer to **Timer Setting Registers 7 to 0 (Figure 12).**
T indicates the minimum delay time of the short time setting (5 μs (typ.) or 10 μs (typ.) by optional switching when internal CLK is used).
LT indicates the minimum delay time of the long time setting (320 μs (typ.) or 640 μs (typ.) by optional switching when internal CLK is used).

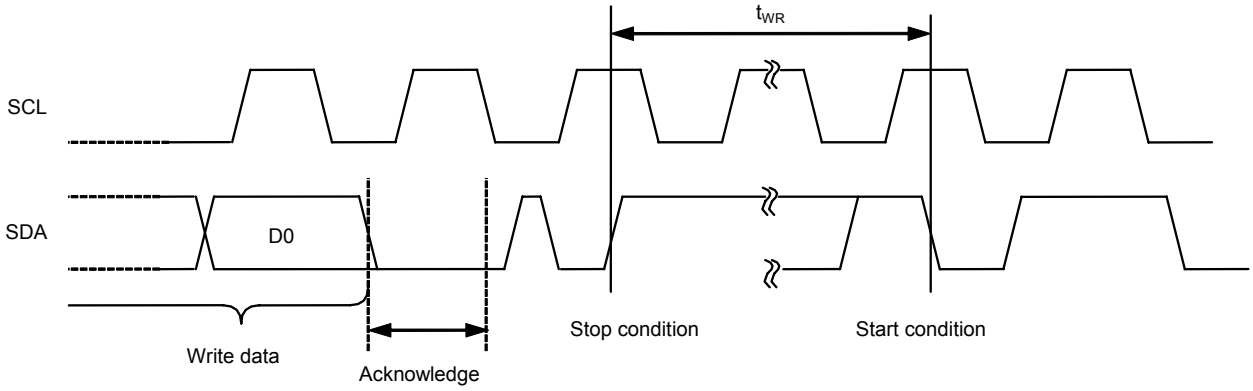


Figure 5 Write Cycle Timing

■ Pin Functions

1. SDA (serial data I/O) pin

The SDA pin is used for bidirectional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
The SDA line is usually pulled up to the V_{CCH} potential via a resistor, and OR-wired with other open-drain or open-collector output devices.

2. SCL (serial clock input) pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rise time and fall time to ensure that they conform to the specifications.

3. WP pin

The WP pin is used to write-protect the E²PROM. (There is no write protection function for registers.)
The write protection function is enabled by connecting the WP pin to the V_{CCH} potential. When there is no need for write protection, connect the WP pin to GND.

4. TIMEN pin

The TIMEN pin is used to enable or disable the output reverse function of the DO pin by setting the timer. When this pin is set to the V_{CCH} potential, the DO pin is reversed after the time set in the timer has elapsed. V_{CCH} must be 2.5 V or higher if VCCH and TIMEN are input simultaneously.

5. CLK pin

The clock for the oscillator can be optionally set whether to be internally generated or input from an external source. When the clock is input from an external source, it is input via the CLK pin. When this pin is not used, connect it to VCCH or GND.

■ Operation

1. Start condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E^2PROM initiates a write cycle.

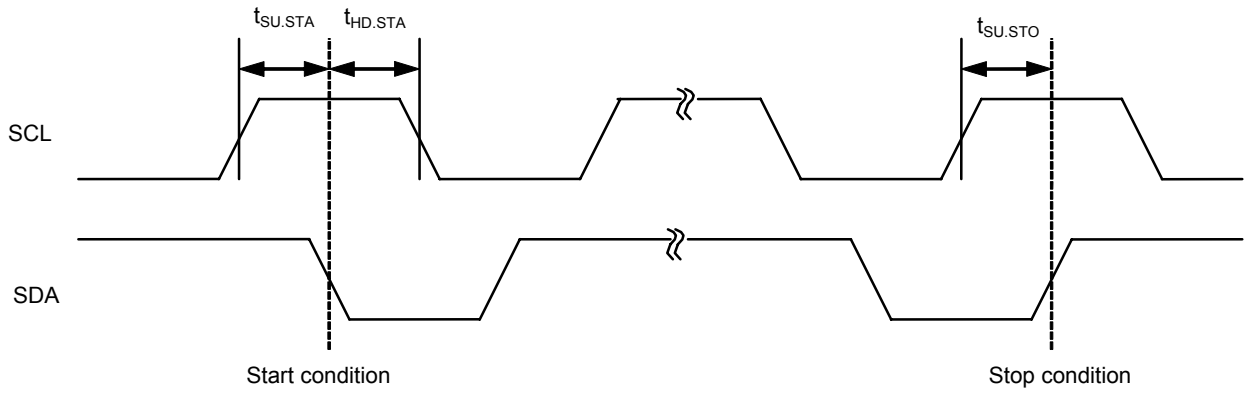


Figure 6 Start/Stop Conditions

3. Data transfer

Data is transferred by changing the SDA line while the SCL line is low.
A start or stop condition is recognized by changing the SDA line while the SCL line is high.

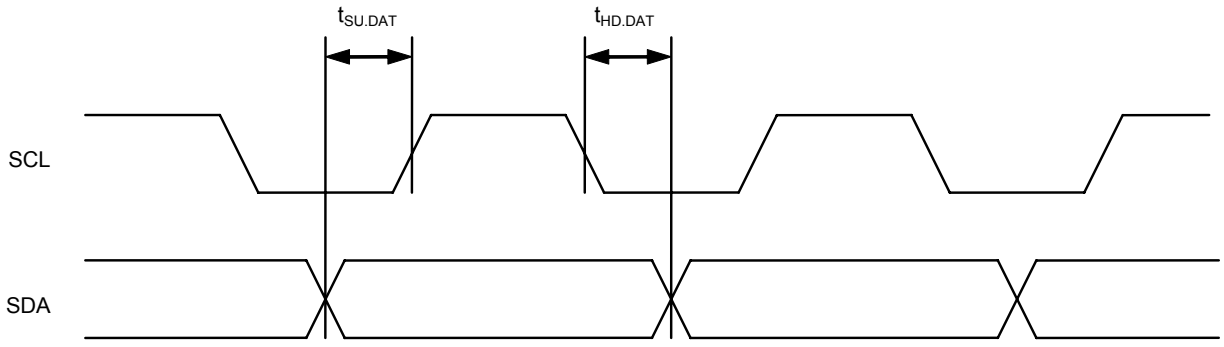


Figure 7 Data Transfer Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge signal.

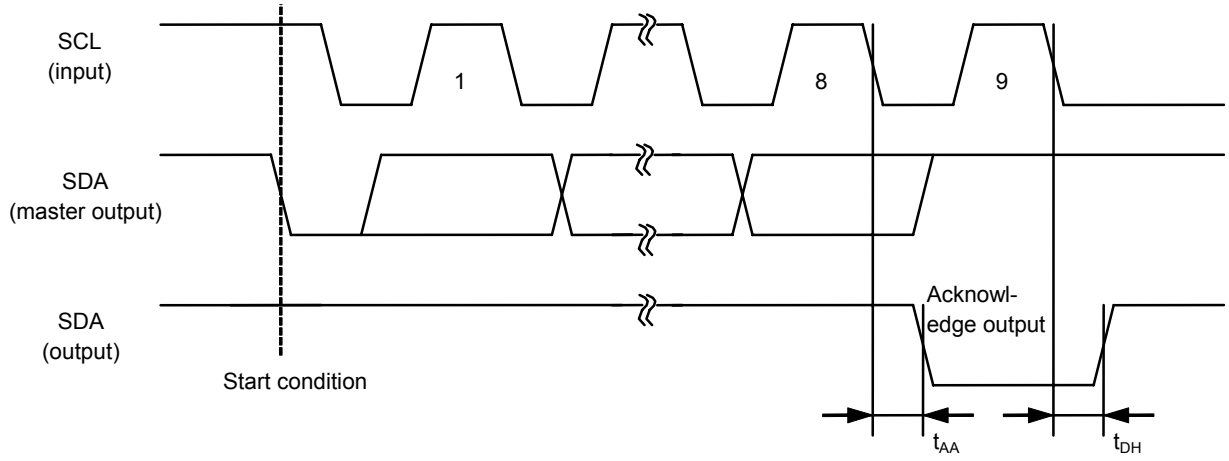


Figure 8 Acknowledge Output Timing

■ Device Addressing

The master device on the system sends the slave device a start condition to perform communication. After that, the master device transmits a 7-bit device address and 1-bit read/write code on the SDA bus.
The higher three bits (DC2, DC1, DC0) of the device address represent the device code.
The next higher bit (TA/$\overline{C}$) represents whether the timer address is set or the command is switched. When this bit is 1, the timer setting register is accessed. When this bit is 0, the bit is recognized as a command.
The next higher three bits (C2, C1, C0) indicate the address of the timer setting register or command. If the timer address setting/command switch bit (TA/$\overline{C}$) is 1, these three bits are used to select one of the eight timer setting registers. If the timer address setting/command switch bit (TA/$\overline{C}$) is 0, a command is selected. In this IC, any of eight device codes (000, 001, 010, 011, 100, 101, 110, 111) can be optionally selected.

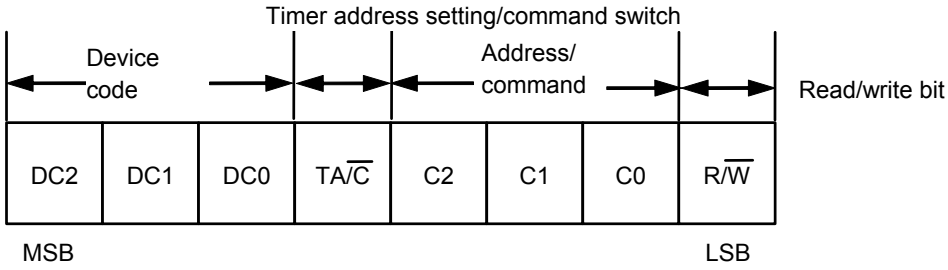


Figure 9 Device Address

■ Command Configuration

If the timer address setting/command switch bit (TA/$\overline{C}$) is 0, the address/command (C2, C1, C0) is recognized as a command. The following eight commands are used to read or write registers. If the timer address setting/command switch bit (TA/$\overline{C}$) is 1, the timer setting register of each port is accessed.

Table 11 Command List

TA/$\overline{C}$	C2	C1	C0	Function	CLK	Access	
						Register	E^2PROM
0	0	0	0	Reload (R/$\overline{W}$ fixed to 0)*1	9	—	—
0	0	0	1	Register/E^2PROM access switch*2	9	—	—
0	0	1	0	Timer enable register access*3	18	W	—
0	0	1	1	Not used (do not access)	—	—	—
0	1	0	0	Free area access1 (E^2PROM)*4	18	R/W	R/W
0	1	0	1	Control port register access*4	18	R/W	R/W
0	1	1	0	Timer scale setting register access*4	18	R/W	R/W
0	1	1	1	Free area access2 (E^2PROM)*3	18	R/W	R/W
1	0	0	0	DO0 timer setting register access*4	18	R/W	R/W
1	0	0	1	DO1 timer setting register access*4	18	R/W	R/W
1	0	1	0	DO2 timer setting register access*4	18	R/W	R/W
1	0	1	1	DO3 timer setting register access*4	18	R/W	R/W
1	1	0	0	DO4 timer setting register access*4	18	R/W	R/W
1	1	0	1	DO5 timer setting register access*4	18	R/W	R/W
1	1	1	0	DO6 timer setting register access*4	18	R/W	R/W
1	1	1	1	DO7 timer setting register access*4	18	R/W	R/W

***1.** When the reload instruction is executed, all the registers are cleared to 0 once,and E^2PROM data is loaded to registers. However, the data in the E^2PROM does not change.

***2.** This command is used to switch between register access mode and E^2PROM access mode. When the R/$\overline{W}$ bit is 0, register access mode is selected, and when 1, E^2PROM access mode is selected. Also, immediately after power supply turning on, it becomes register access mode.

***3.** If the R/$\overline{W}$ bit for this command is 0, the timer enable register is written. If this bit is 1, no operation is performed because the register is write only.

***4.** The register/E^2PROM access switch command makes it possible to switch whether the register or E^2PROM is accessed. When the E^2PROM is rewritten, the register is rewritten at the same time.

■ Control Port Register

The control port register is an 8-bit register used to set the output data of the output ports (DO7 to DO0). All the bits are 0 in the initial status (before the data in E^{2}PROM is loaded). The data is reversed when the delay time set by the value of the timer setting register has elapsed.

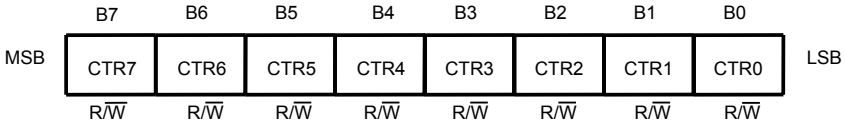


Figure 10 Control Port Register

■ Timer Scale Setting Register

The timer scale register is an 8-bit register used to select the scale of the timer setting register for each port (e.g., TS7 corresponds to DO7).
All the bits are set to the short time in the initial status (before the data in E^{2}PROM is loaded).

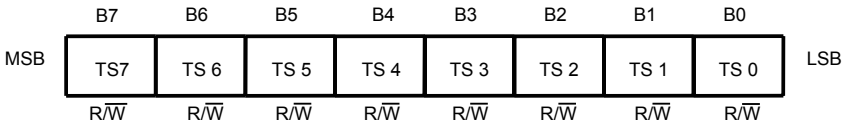


Figure 11 Timer Scale Setting Register

1: Short time is set
0: Long time is set

■ Timer Setting Registers 7 to 0

The timer setting registers are 8-bit registers that correspond the respective ports and are used to set the delay time of the output change of the output ports (DO7 to DO0). When the delay time set by setting the bit of each register has elapsed, the corresponding port (control port register) is reversed. (When the set bit is cleared to 0, the port is not reversed.) The set time can be switched to the short time setting or long time setting for each port by setting the timer scale register. Set only one bit to 1 for each port.

MSB	B7	B6	B5	B4	B3	B2	B1	B0	LSB
DO7	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO6	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO5	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO4	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO3	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO2	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO1	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
DO0	8 × T	7 × T	6 × T	5 × T	4 × T	3 × T	2 × T	1 × T	
	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	R/$\overline{W}$	

Figure 12 Timer Setting Registers 7 to 0

In **Figure 12**, each part is for short time setting. T changes to LT for the parts for long time setting.
The following options can be selected for setting the timer time.

- Switching of CLK for oscillation to internal generation or external input
- Delay time option setting (2 types)
  A: One time setting
  B: Twice setting
  <1> When internal CLK is used (Typ.)
  Option A: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (5 μs, 320 μs)
  Option B: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (10 μs, 640 μs)
  <2> When external CLK is used (CLK cycle input from CLK pin = T')
  Option A: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (T', 64 × T')
  Option B: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (2 × T', 128 × T')

For DO7, when the B6 bit is set to 1 in the timer setting register and the B7 bit is set to 1 in the timer scale register, DO7 is reversed after a delay time of 35 μs (7 × 5 μs). Other examples are shown in the figure below.

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 1-1	40 μs	35 μs	30 μs	25 μs	20 μs	15 μs	10 μs	5 μs
Example 1-2	2.56 ms	2.24 ms	1.92 ms	1.60 ms	1.28 ms	0.96 ms	0.64 ms	0.32 ms

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 2-1	160 μs	140 μs	120 μs	100 μs	80 μs	60 μs	40 μs	20 μs
Example 2-2	10.24 ms	8.96 ms	7.68 ms	6.40 ms	5.12 ms	3.84 ms	2.56 ms	1.28 ms

Example 1•••When internal CLK is used
Example 1-1. Timer scale register: 1 (Short time setting), Delay time option: A (One time setting) (T = 5 μs)
Example 1-2. Timer scale register: 0 (Long time setting), Delay time option: A (One time setting) (LT = 320 μs)

Example 2•••When external CLK (100 kHz, T' = 10 μs) is used
Example 2-1. Timer scale register: 1 (Short time setting), Delay time option: B (Twice setting) (T = 2 × T' = 20 μs)
Example 2-2. Timer scale register: 0 (Long time setting), Delay time option: B (Twice setting) (LT = 128 × T' = 1280 μs)

Figure 13 Usage Example of Timer Setting Registers 7 to 0

■ Timer Enable Register

The timer enable register is an 8-bit write-only register. When each bit of this register is set to 1, the oscillator starts operating and the outputs of the output ports (DO7 to DO0) are reversed after the time set by the timer setting register has elapsed. When the bits of this register are cleared to 0 or the timer setting register for DO is cleared to 0, the output ports do not change. Timer operation starts when all the data has been received during timer enable command transmission. After 1 is written to the timer enable register, the bit to which 1 is written is automatically cleared to 0, so rewriting is not required. This register cannot be written while the timer is operating; write to this register after timeout.

	B7	B6	B5	B4	B3	B2	B1	B0
MSB	TEN7	TEN 6	TEN 5	TEN 4	TEN 3	TEN 2	TEN 1	TEN 0 LSB
	W	W	W	W	W	W	W	W

Figure 14 Timer Enable Register

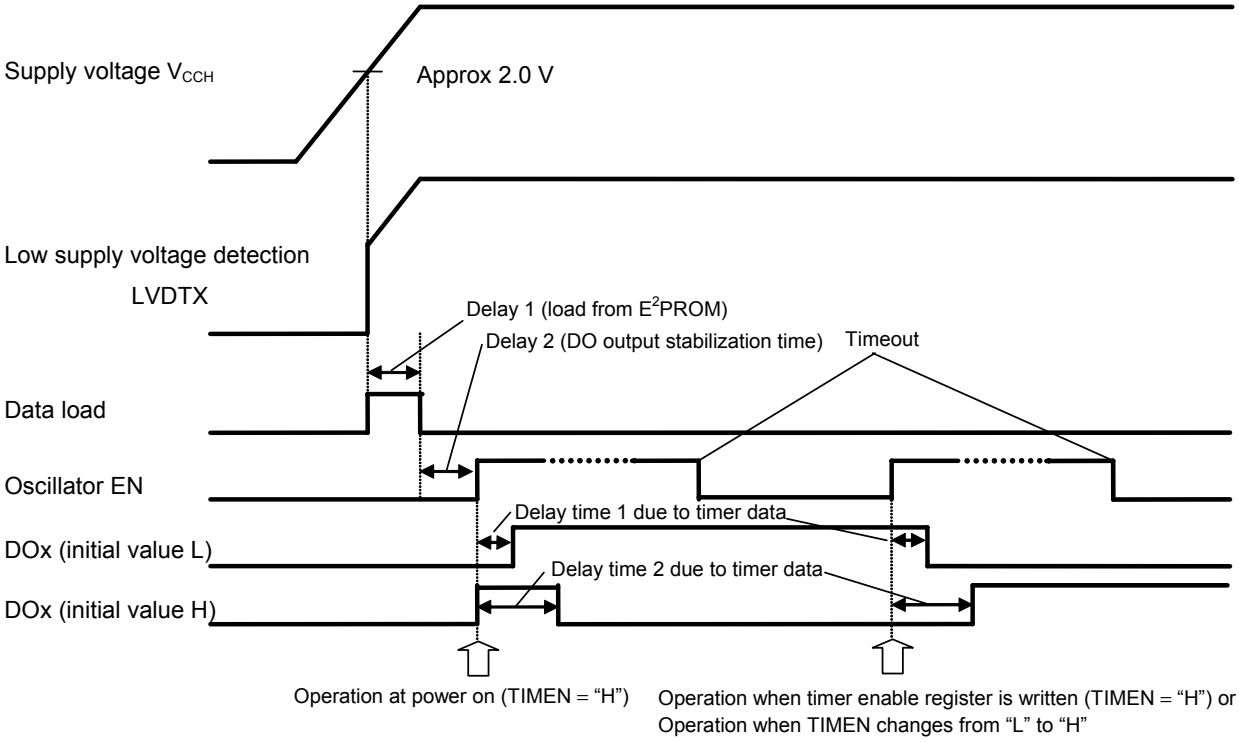
0: Output reverse disabled
1: Output reverse enabled

■ E²PROM Block

The S-7750B incorporates an E²PROM, and the following data hold the initial values when the power is off. The respective memory areas can be rewritten using a command.

- Data for control port register (1 byte)
  The data in the E²PROM is transferred to the control port register when power is applied.
- Data for timer setting register (DO7 to DO0) (1 byte for each port, total 8 bytes)
  The data in the E²PROM is transferred to the timer setting register when power is applied.
- Data for timer scale setting register (1 byte)
  The data in the E²PROM is transferred to the timer scale setting register when power is applied.
- Free area (2 bytes)
  This area can be used as a free area for user memory. This area does not affect other operations.

■ Timing of Loading Data from E²PROM



V_{CCH} must be 2.5 V or higher if VCCH and TIMEN are input simultaneously.

Figure 15

Data is loaded from the E²PROM to each register when power is applied or reload command is transmitted.
The output of the DO pin is reversed at the following timing according to the value of the timer data.

(a) When power is applied (when TIMEN = High)
(b) When the TIMEN pin changes from low to high
(c) When the timer enable register is being written

■ Operation Flowchart

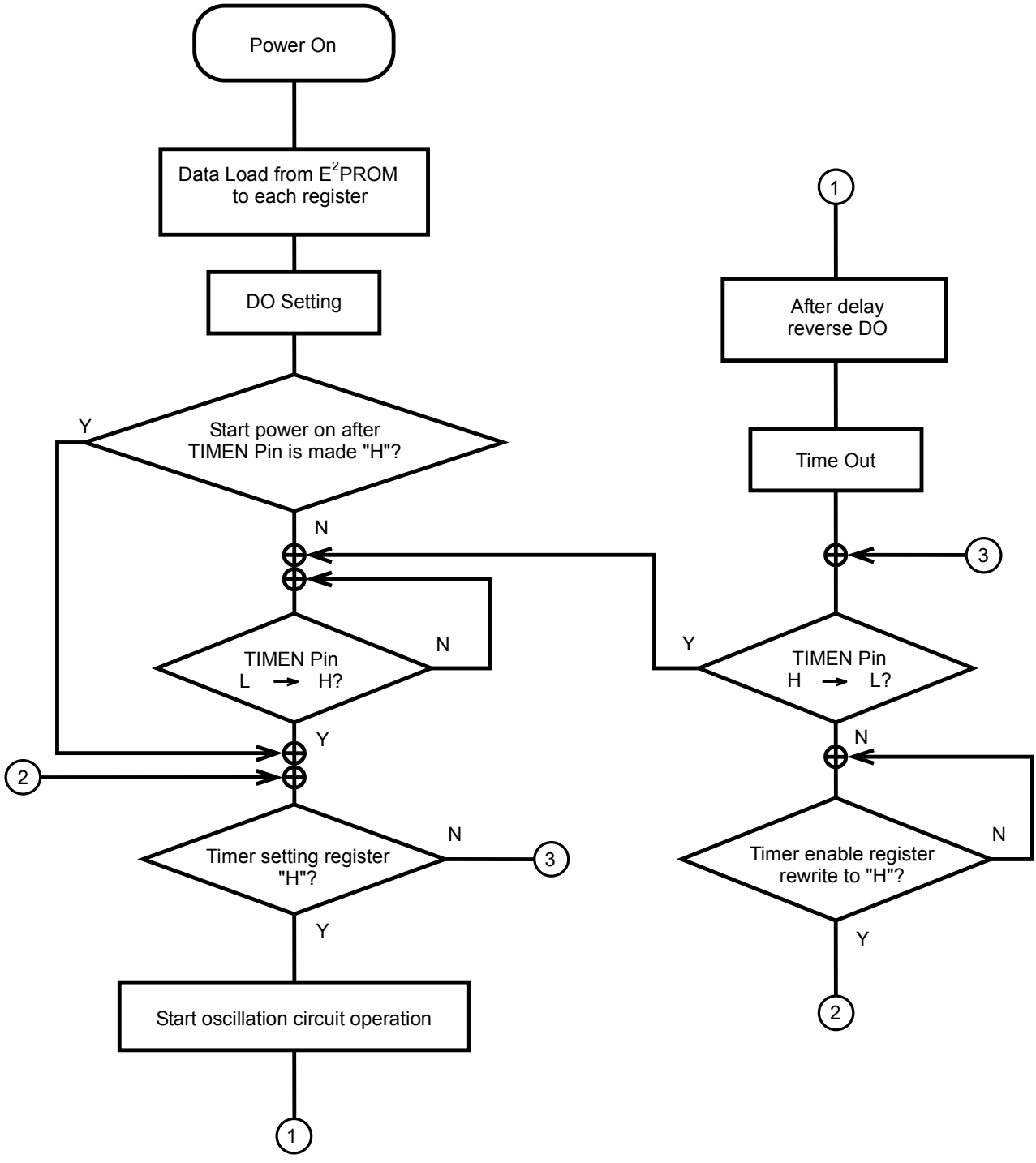
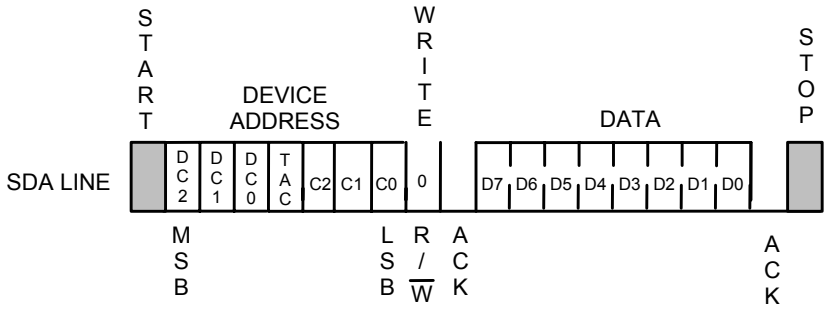


Figure 16 Operation Flowchart

■ Write Operation

1. Writing

When the S-7750B receives a 7-bit device address and 0 for the read/write instruction code following the start condition, an acknowledge signal is generated.
After 8-bit write data is subsequently received and an acknowledge signal is generated, a stop condition is received and a write operation starts.
While the S-7750B is being written, all operations are prohibited and no acknowledge signals are received.



* For reload command and register / E^{2}PROM access command, DATA (8-bit) and the following ACK are unnecessary.

Figure 17 Byte Write

2. Write Protection

Write protection is available in the S-7750B. When the WP pin is connected to the V_{CCH}, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (5 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.
If there is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.

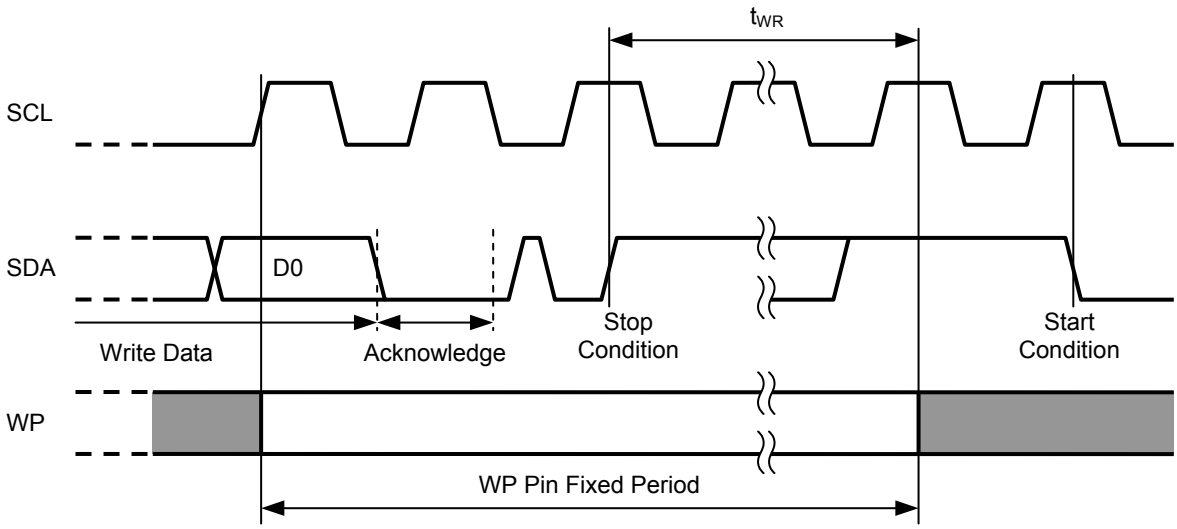


Figure 18 WP Pin Fixed Period

3. Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the S-7750B.
After the S-7750B receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the S-7750B by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the S-7750B (i.e., the slave device).
That is, if the S-7750B does not generate an acknowledge, the write cycle is in progress and if the S-7750B generates an acknowledge, the write cycle has been completed.
Keep the level of the WP pin fixed until acknowledge is confirmed.
It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

■ Read Operation

When the S-7750B receives a 7-bit device address and 1 for the read/write instruction code following the start condition, an acknowledge signal is generated.
After that, 8-bit write data is output from the S-7750B in synchronization with the SCL clock.
Subsequently, when the master device transmits a stop condition instead of outputting an acknowledge signal, the read operation is complete.

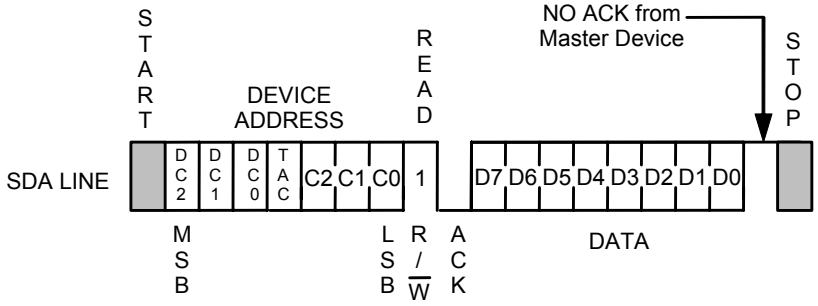


Figure 19 Read

■ Write Inhibition Function at Low Power Voltage

The S-7750B have a detection circuit for low power voltage. The detection circuit cancels a write instruction when the power voltage is low or the power switch is on. The detection voltage is 1.75 V typically and the release voltage is 2.05 V typically, the hysteresis of approximate 0.3 V thus exists. (refer to **Figure 20**.)
When a low power voltage is detected, a write instruction is canceled at the reception of a stop condition.
When the power voltage lowers during a data transmission or a write operation, the data at the address of the operation is not assured.

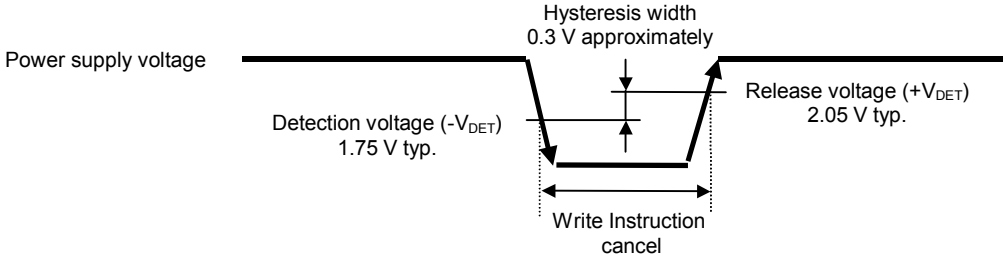


Figure 20 Operation at low power voltage

■ Using S-7750B

1. Adding pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 kΩ to 5 kΩ pull-up resistor to the SCL input pin*1 and the SDA I/O pin in order to enable the functions of the I^{2}CBUS protocol. Normal communication cannot be provided without a pull-up resistor.

***1.** When the SCL input pin of the S-7750B is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.
This protects the S-7750B from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

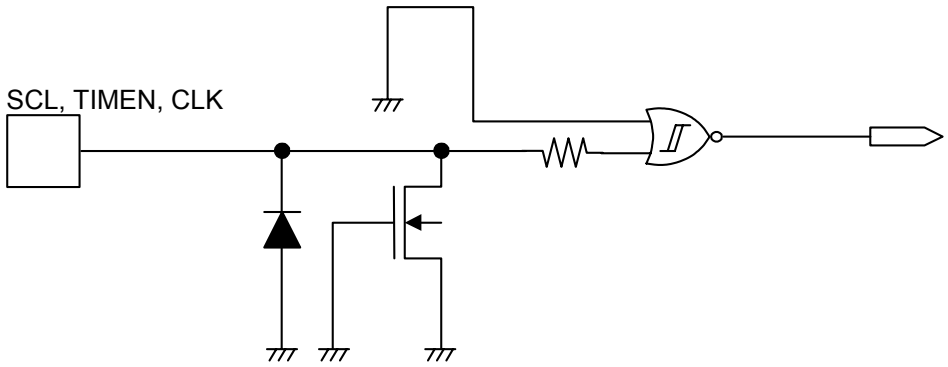


Figure 21 SCL, TIMEN, CLK Pin

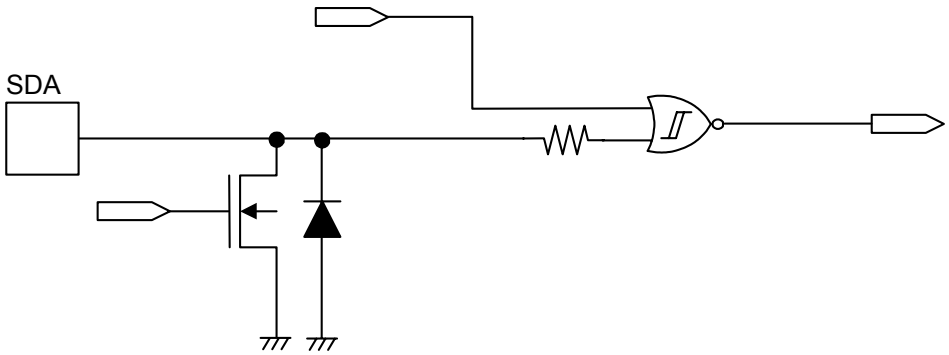


Figure 22 SDA Pin

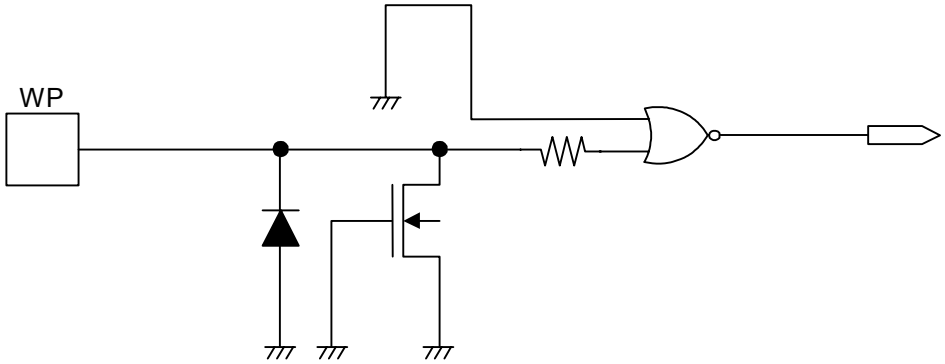


Figure 23 WP Pin

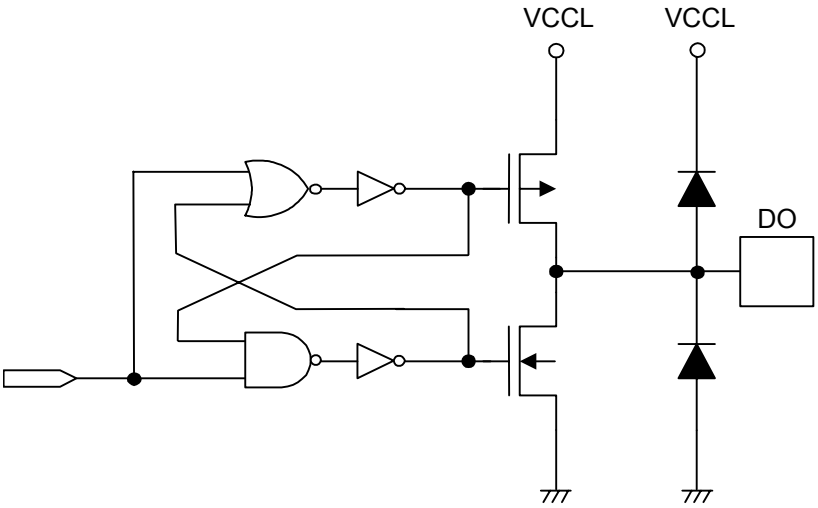


Figure 24 DO Pin

3. Matching phases while S-7750B is accessed

The S-7750B does not have a pin for resetting (the internal circuit), therefore, the S-7750B cannot be forcibly reset externally. If a communication interruption occurs in the S-7750B, it must be reset by software.
For example, even if a reset signal is input to the microprocessor, the internal circuit of the S-7750B is not reset as long as the stop condition is not input to the S-7750B. In other words, the S-7750B retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the S-7750B (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset S-7750B]

The S-7750B can be reset by the start and stop instructions. When the S-7750B is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 25** shows this procedure.
First, input the start condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the S-7750B interrupts the acknowledge output operation or data output, so input the start condition*1. When a start condition is input, the S-7750B is reset. To make doubly sure, input the stop condition to the S-7750B. Normal operation is then possible.

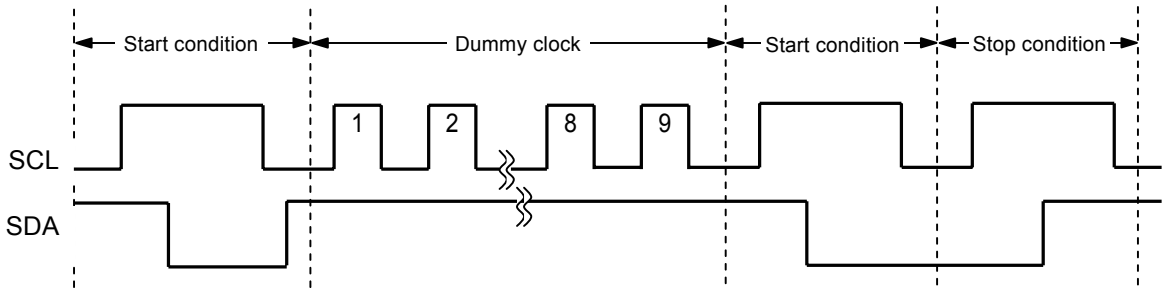


Figure 25 Resetting S-7750B

***1.** After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised. The S-7750B incorporates a low voltage detector that allows the S-7750B to be reset automatically.

4. Acknowledge check

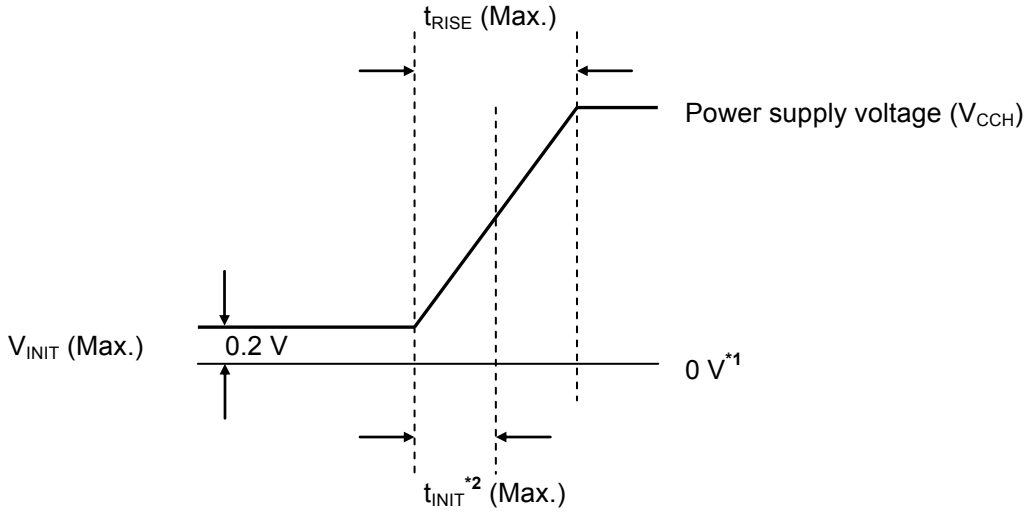
The I²CBUS protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and the S-7750B. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

5. Built-in power-on-clear circuit

S-7750B has a built-in power-on-clear circuit that initializes the S-7750B when starting power supply. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

5. 1 Raising power supply voltage

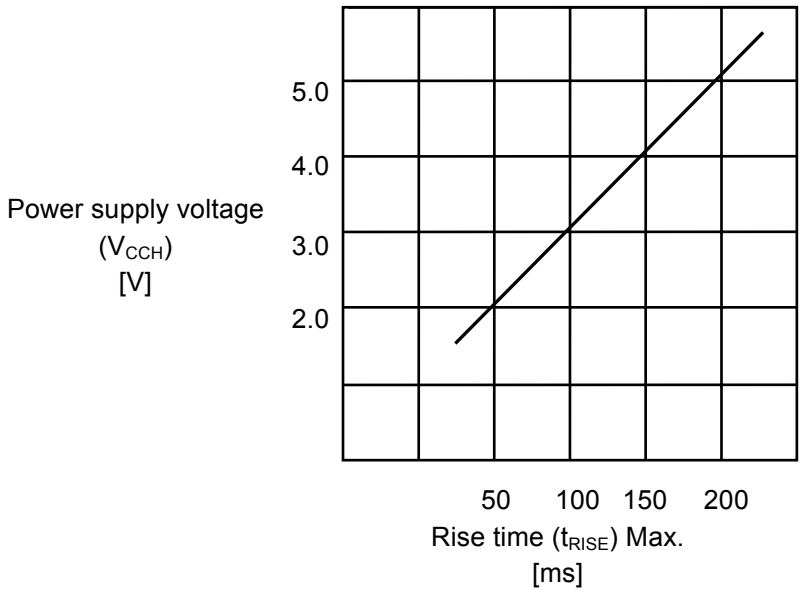
Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 26**.
For example, when the power supply voltage to be used is 3.0 V, t_{RISE} is 100 ms as shown in **Figure 27**. The power supply voltage must be raised within 100 ms.



***1.** 0 V means there is no difference in potential between the VCCH pin and the VSS pin of the S-7750B.

***2.** t_{INIT} is the time required to initialize the S-7750B. No instructions are accepted during this time.

Figure 26 Raising Power Supply Voltage



For example:
If your S-7750B supply voltage = 3.0 V, raise the power supply voltage to 3.0 V within 100 ms.

Figure 27 Raising Time of Power Supply Voltage

When initialization is successfully completed via the power-on-clear circuit, the S-7750B enters the standby status.

If the power-on-clear circuit does not operate, the followings are the possible causes.

(1) Because the S-7750B has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
(2) The voltage may have dropped due to power off while the S-7750B is being accessed. Even if the microprocessor is reset due to the low power voltage, the S-7750B may malfunction unless the power-on-clear operation conditions of S-7750B are satisfied. For the power-on-clear operation conditions of S-7750B, refer to **5. 1 Raising power supply voltage**.

5. 2 Wait for the initialization sequence to end

The S-7750B executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 28**.

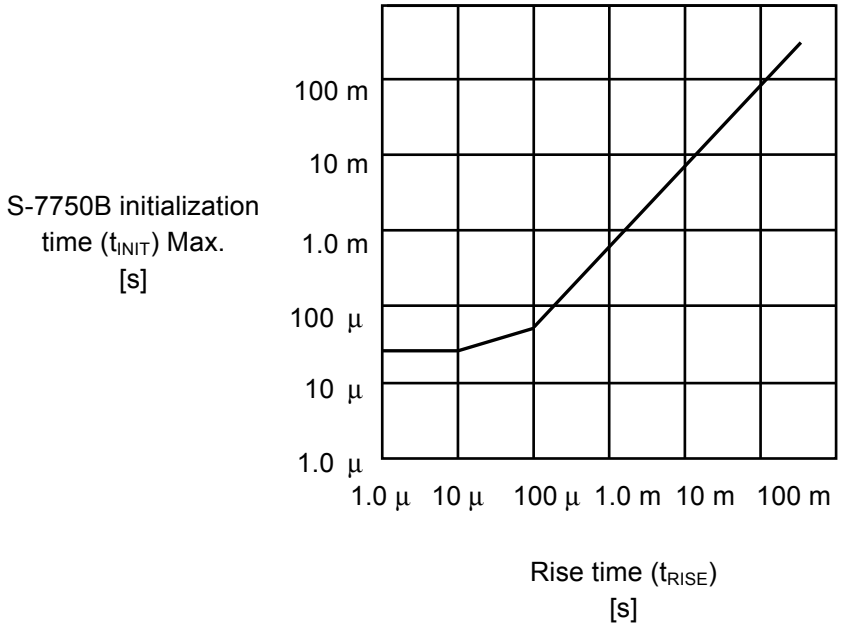


Figure 28 Initialization Time of S-7750B

6. Data hold time ($t_{HD.\ DAT}$ = 0 ns)

If SCL and SDA of the S-7750B are changed at the same time, it is necessary to prevent the start/stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the S-7750B enters the standby status.
It is recommended that SDA is delayed from the falling edge of SCL by 0.3 µs minimum in the S-7750B. This is to prevent a time lag caused by the load of the bus line from generating the stop (or start) condition.

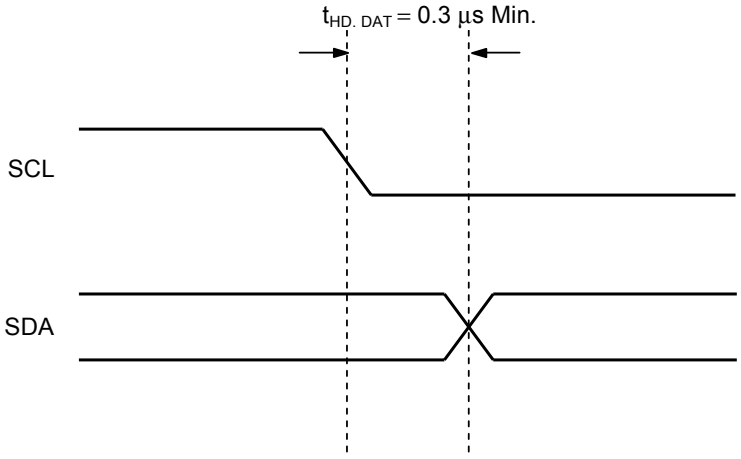


Figure 29 S-7750B Data Hold Time

7. SDA pin and SCL pin noise elimination time

The S-7750B includes a built-in low-pass filter to eliminate noise at the SDA and SCL pins. This means that if the power supply voltage is 3.0 V, noise with a pulse width of 130 ns or less can be eliminated. (refer to **Figure 30**.)
For details of the guaranteed values, refer to noise suppression time (t_I) in **Table 9**.

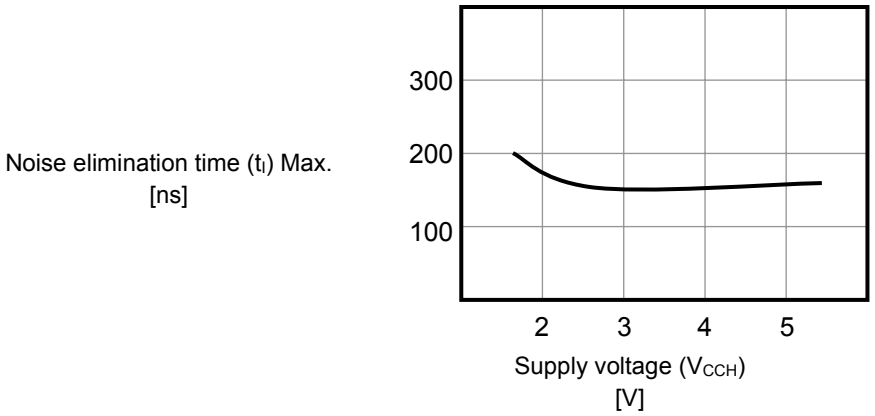


Figure 30 Noise Elimination Time for SDA and SCL Pins

8. S-7750B operation when stop condition is received during write operation before receiving defined data value (less than 8 bits) at SCL pin

When the S-7750B receives the stop condition signal forcibly while receiving 1 byte of write data, the write operation is aborted.

9. Precautions

- Semiconductor devices must be used within the absolute maximum rating. Special caution is required for the supply voltage. A momentary surge voltage exceeding the rated value may cause latch-up and malfunction. Confirm the detailed usage conditions required for each parameter by referring to the data sheet before use.
- If the S-7750B operates with moisture remaining in the circuits, a short circuit may occur between pins, causing a malfunction. When the S-7750B is taken out of the constant-low-temperature bath during evaluation, the pins of the S-7750B may be frosted. Note that, if the S-7750B is operated with the pins frosted, the pins may be short-circuited by moisture, causing a malfunction.
  The same applies when the S-7750B is used in an environment where condensation may occur, so care is required.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Precautions for WLP Package

- The device's silicon substrate side is exposed to the marking side of the device package. Since this portion has a lower strength against mechanical stress than a standard plastic package, take sufficient care to avoid chips and cracks when handling the package. Moreover, the exposed side of the silicon has the electrical potential of the device substrate, and needs to be kept out of contact with the external potential.
- In this package, the transistor area side is overcoated with a translucent resin. Keep in mind that the characteristics of the package may be affected if the device is exposed under an intensive light source.

■ I^{2}C Bus License

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Please note that a product or a system incorporating this IC may infringe upon the Philips I^{2}C Patent Rights depending upon its configuration. In the event of such infringement, Seiko Instruments Inc., shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

■ Options

In the S-7750B, the following options can be selected.

- Switching device codes (8 types)
  (000, 001, 010, 011, 100, 101, 110, 111)
- Switching of CLK for oscillation to internal generation or external input
- Delay time option setting (2types)
  A: One time setting
  B: Twice setting
  <1> When internal CLK is used (Typ.)
  Option A: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (5 μs, 320 μs)
  Option B: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (10 μs, 640 μs)
  <2> When external CLK is used (CLK cycle input from CLK pin = T')
  Option A: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (T', 64 × T')
  Option B: (Delay time of short time setting, Delay time of long time setting) = (T, LT) = (2 × T', 128 × T')

■ Option List

The following provides lists and descriptions of three options that can be selected in the S-7750B. Appropriately specify the desired option referring to the following.

(1) Switching device codes (8 types)

Any device address codes can be specified (refer to **Figure 9**).

Table 12 Device Code Option List

No.	C2	C1	C0
⓪	0	0	0
①	0	0	1
②	0	1	0
③	0	1	1
④	1	0	0
⑤	1	0	1
⑥	1	1	0
⑦	1	1	1

(2) Switching of CLK for oscillation to internal generation or external input

The S-7750B incorporates an oscillator for generating delay time. Instead of using the oscillator, an external oscillation CLK can be used for the delay time.

Table 13 Oscillation CLK Option List

No.	Internal/External
①	Use internal oscillator
②	Use external oscillation input

(3) Switching of delay time option (2 types)

The delay time can be selected between A: One time and B: Twice time. (T': Oscillation CLK cycle (5 μs when the internal oscillator is used).).

Table 14 Delay Time Option List

No.	Delay Selection	Timer Scale Setting Register	
		1: Short Time Setting Delay Time (T)	0: Long Time Setting Delay Time (LT)
A	One time	T'	T' × 64
B	Twice	T' × 2	T' × 128

■ Format for Selecting Options

To specify options, complete the following tables and submit them to SII.

(1) Switching device codes

No.	C2	C1	C0

(2) Switching of CLK for oscillation to internal generation or external input

No.	Internal/External

(3) Switching of delay time option

No.	One time / Twice

■ List of Data to Be Written to E²PROM

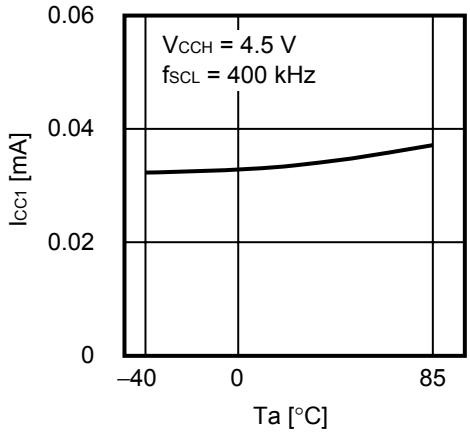
To specify the data to be written to the E²PROM, complete the following table and submit it to SII.

E²PROM (Command Code)	Write Data	Default	Remark
Free area1 (0100)		FFH	—
Control port (0101)		00H	—
Timer scale setting (0110)		FFH	1: Short time, 0: Long time
Free area2 (0111)		FFH	—
D0 timer setting (1000)		00H	1 for selected time, otherwise 0
D1 timer setting (1001)		00H	1 for selected time, otherwise 0
D2 timer setting (1010)		00H	1 for selected time, otherwise 0
D3 timer setting (1011)		00H	1 for selected time, otherwise 0
D4 timer setting (1100)		00H	1 for selected time, otherwise 0
D5 timer setting (1101)		00H	1 for selected time, otherwise 0
D6 timer setting (1110)		00H	1 for selected time, otherwise 0
D7 timer setting (1111)		00H	1 for selected time, otherwise 0

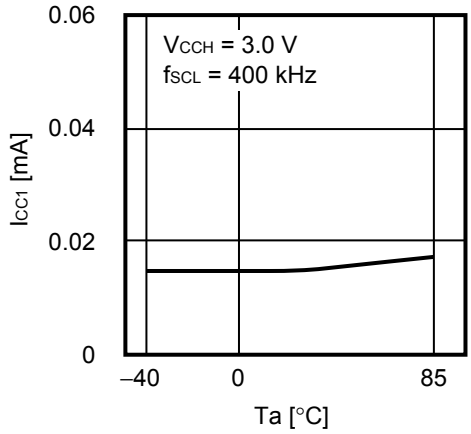
■ Typical Characteristics

1. DC Characteristics

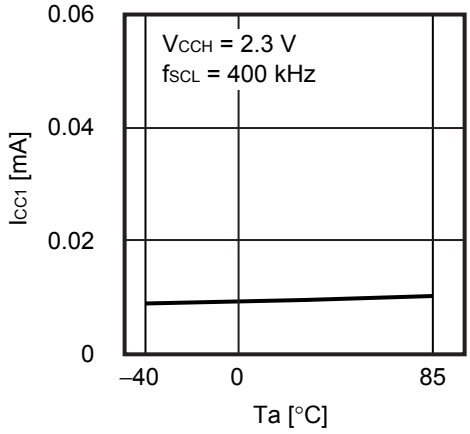
1.1 Current consumption (READ) I_{CC1}
— Ambient temperature Ta



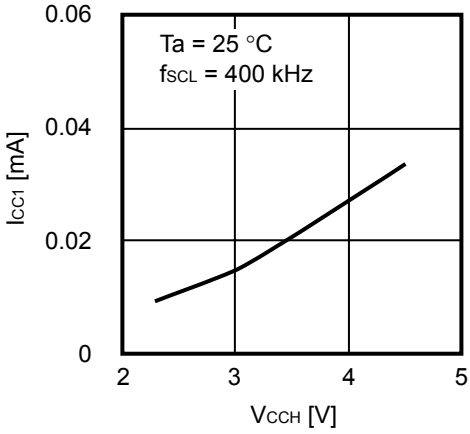
1.2 Current consumption (READ) I_{CC1}
— Ambient temperature Ta



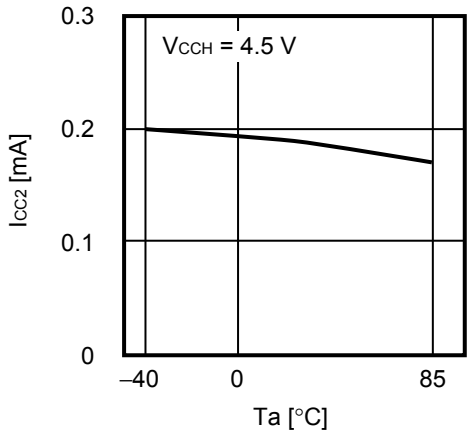
1.3 Current consumption (READ) I_{CC1}
— Ambient temperature Ta



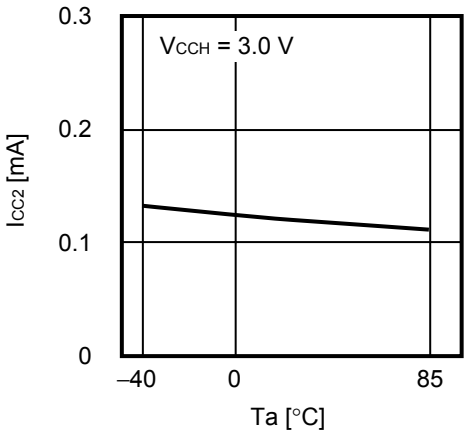
1.4 Current consumption (READ) I_{CC1}
— Power supply voltage V_{CCH}



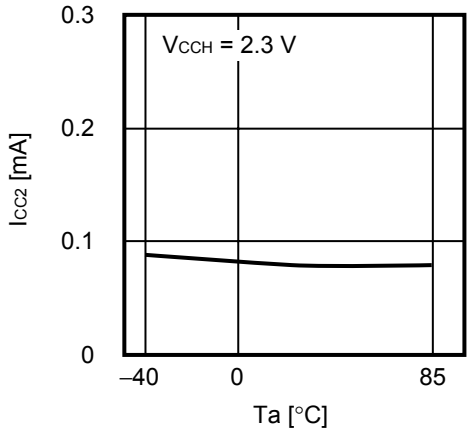
1.5 Current consumption (PROGRAM) I_{CC2}
— Ambient temperature Ta



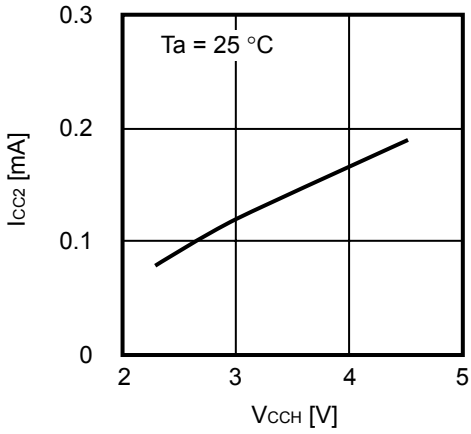
1.6 Current consumption (PROGRAM) I_{CC2}
— Ambient temperature Ta



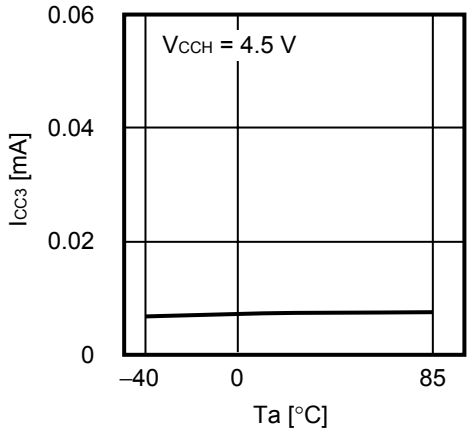
1.7 Current consumption (PROGRAM) I_{CC2} — Ambient temperature Ta



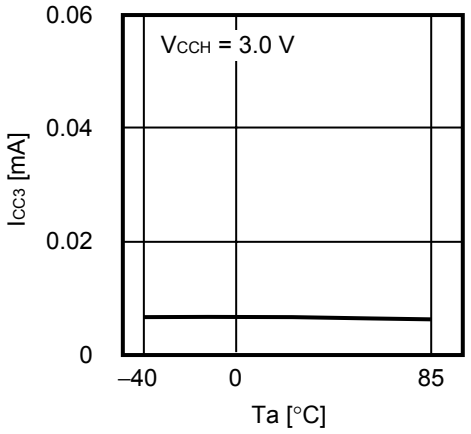
1.8 Current consumption (PROGRAM) I_{CC2} — Power supply voltage V_{CCH}



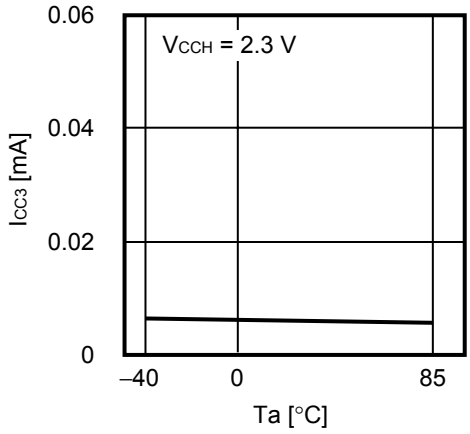
1.9 Internal oscillator current consumption during operation I_{CC3} — Ambient temperature Ta



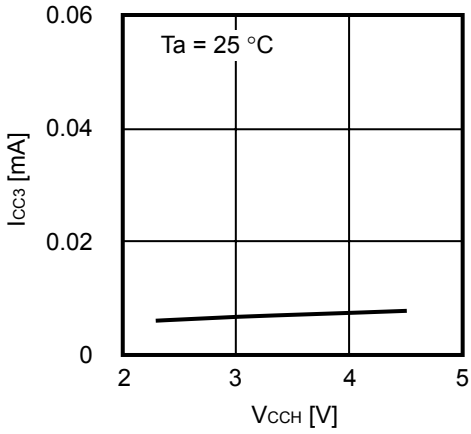
1.10 Internal oscillator current consumption during operation I_{CC3} — Ambient temperature Ta



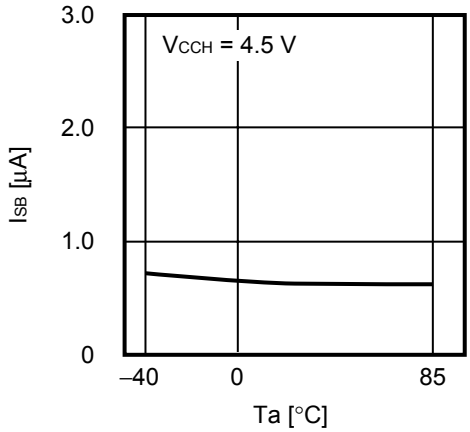
1.11 Internal oscillator current consumption during operation I_{CC3} — Ambient temperature Ta



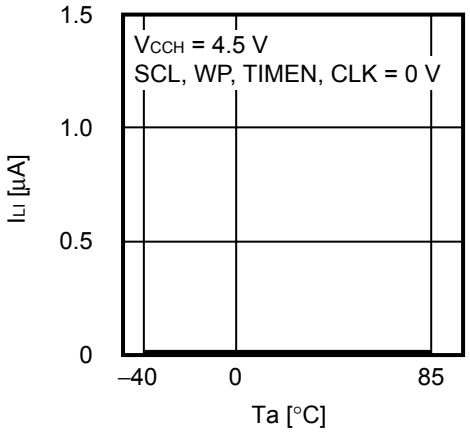
1.12 Internal oscillator current consumption during operation I_{CC3} — Power supply voltage V_{CCH}



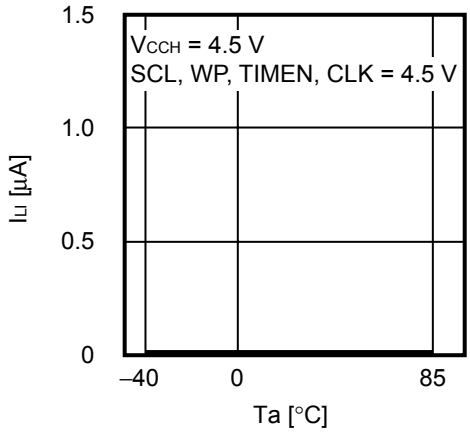
1.13 Standby current consumption I_{SB}
— Ambient temperature Ta



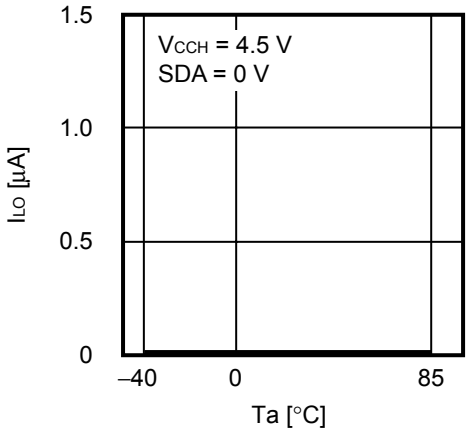
1.14 Input leakage current I_{LI}
— Ambient temperature Ta



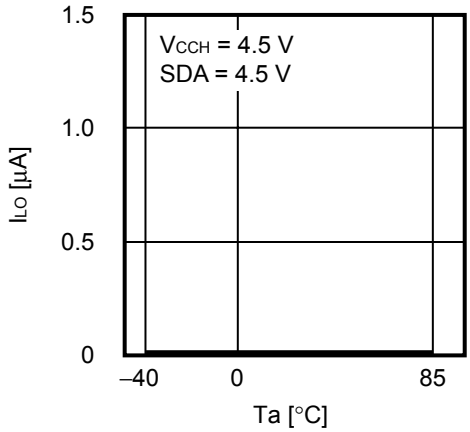
1.15 Input leakage current I_{LI}
— Ambient temperature Ta



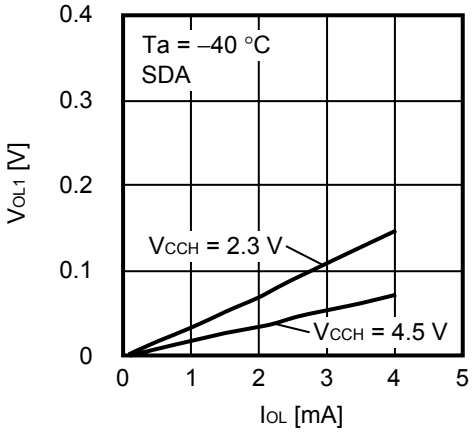
1.16 Output leakage current I_{LO}
— Ambient temperature Ta



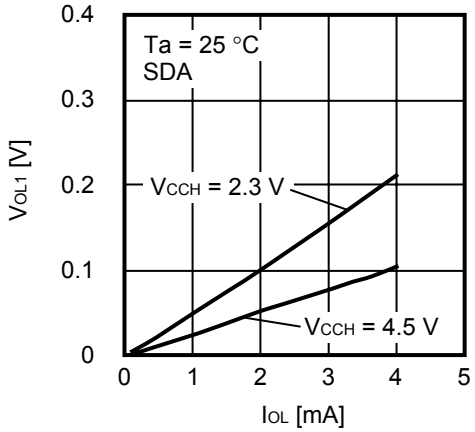
1.17 Output leakage current I_{LO}
— Ambient temperature Ta



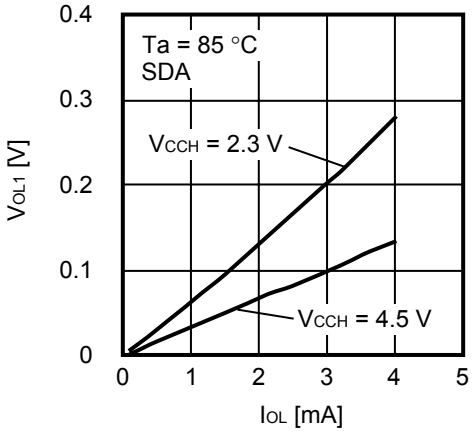
1.18 Low level output voltage V_{OL1}
— Low level output current I_{OL}



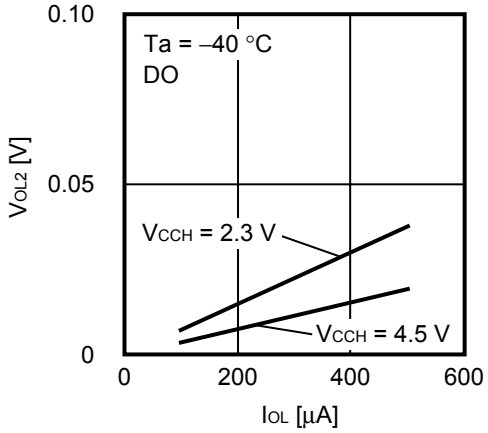
1.19 Low level output voltage V_{OL1} — Low level output current I_{OL}



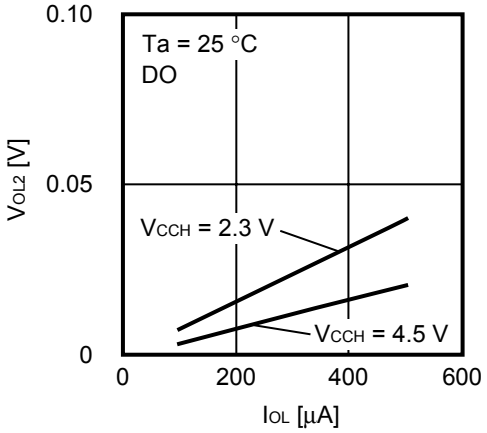
1.20 Low level output voltage V_{OL1} — Low level output current I_{OL}



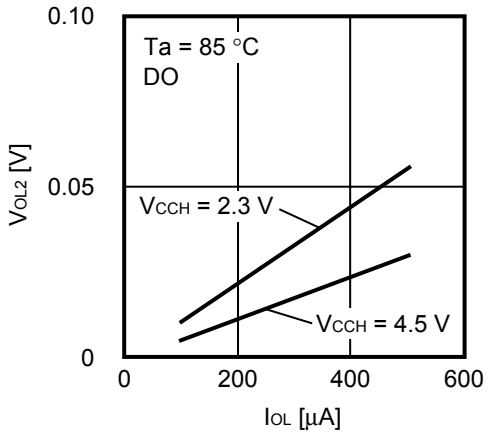
1.21 Low level output voltage V_{OL2} — Low level output current I_{OL}



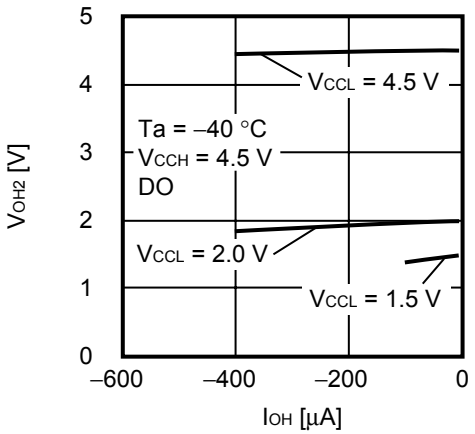
1.22 Low level output voltage V_{OL2} — Low level output current I_{OL}



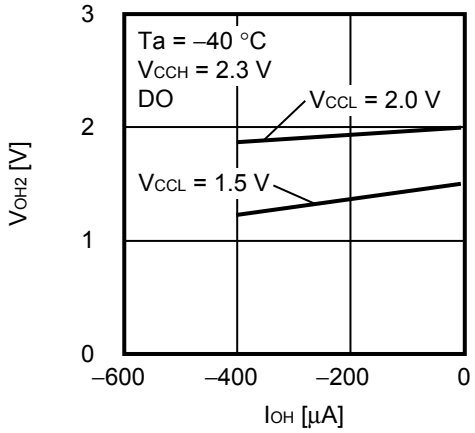
1.23 Low level output voltage V_{OL2} — Low level output current I_{OL}



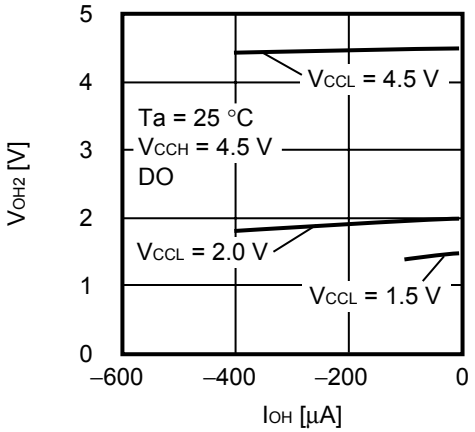
1.24 High level output voltage V_{OH2} — High level output current I_{OH}



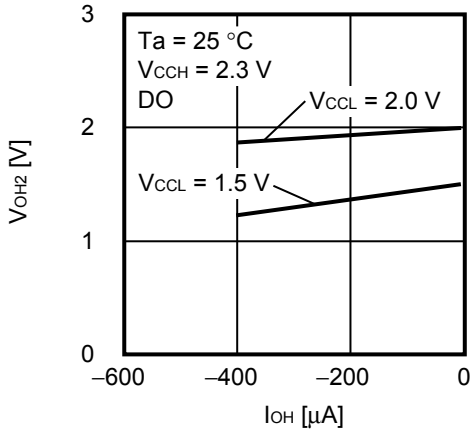
1.25 High level output voltage V_{OH2} — High level output current I_{OH}



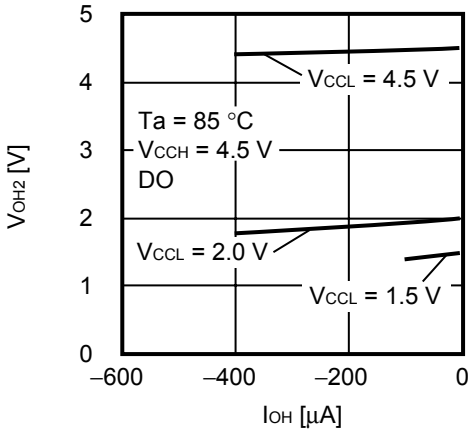
1.26 High level output voltage V_{OH2} — High level output current I_{OH}



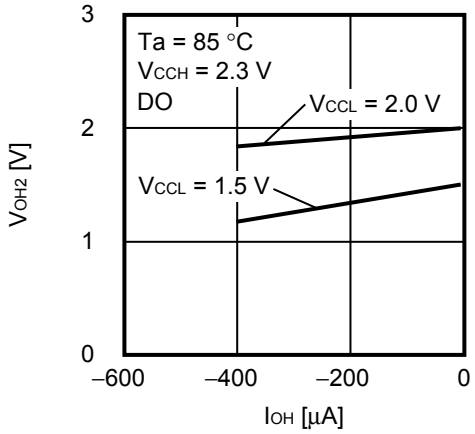
1.27 High level output voltage V_{OH2} — High level output current I_{OH}



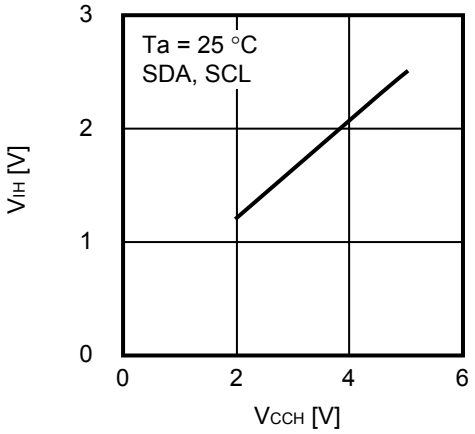
1.28 High level output voltage V_{OH2} — High level output current I_{OH}



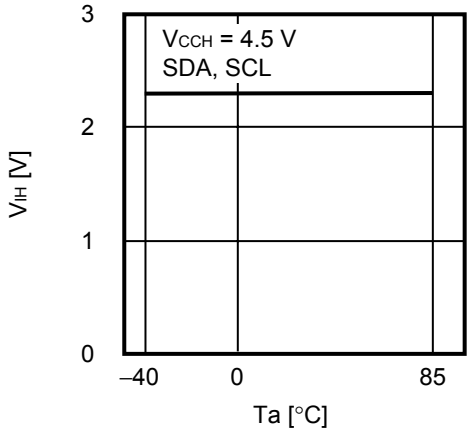
1.29 High level output voltage V_{OH2} — High level output current I_{OH}



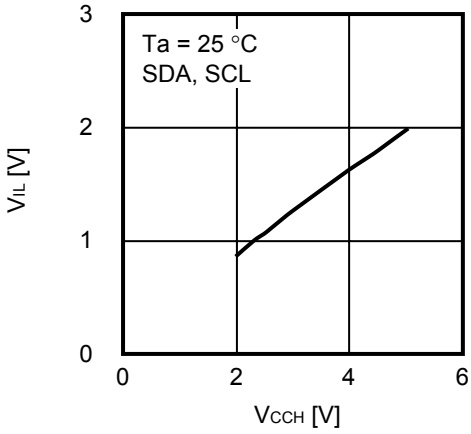
1.30 High input inversion voltage V_{IH} — Power supply voltage V_{CCH}



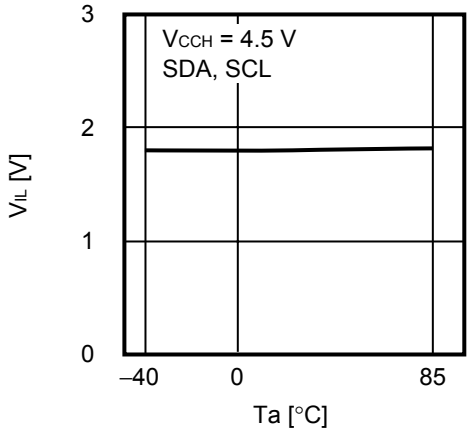
1.31 High input inversion voltage V_{IH}
— Ambient temperature Ta



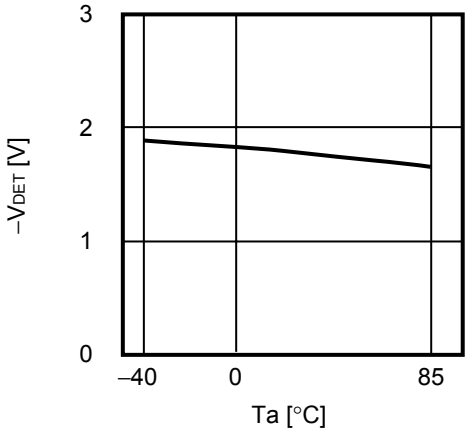
1.32 Low input inversion voltage V_{IL}
— Power supply voltage V_{CCH}



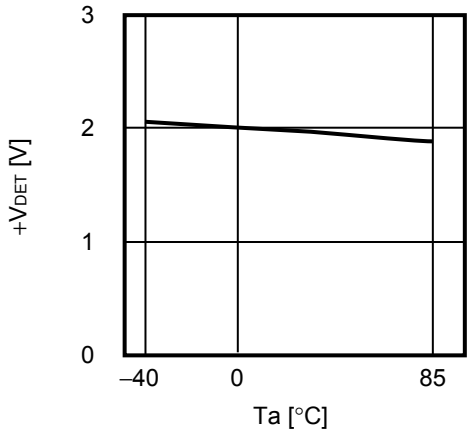
1.33 Low input inversion voltage V_{IL}
— Ambient temperature Ta



1.34 Low power supply detection voltage $-V_{DET}$
— Ambient temperature Ta

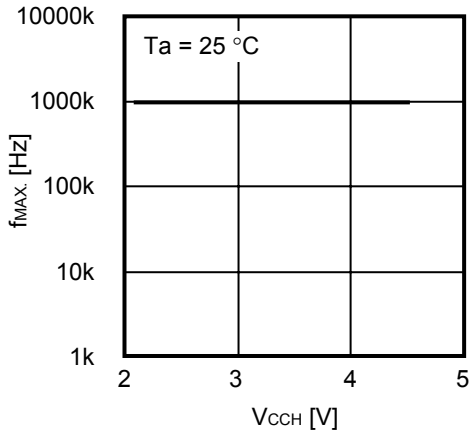


1.35 Low power supply release voltage $+V_{DET}$
— Ambient temperature Ta

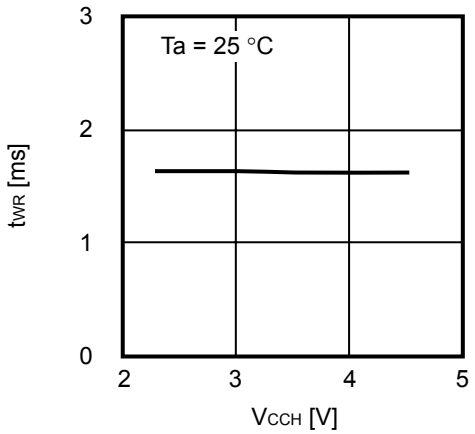


2. AC Characteristics

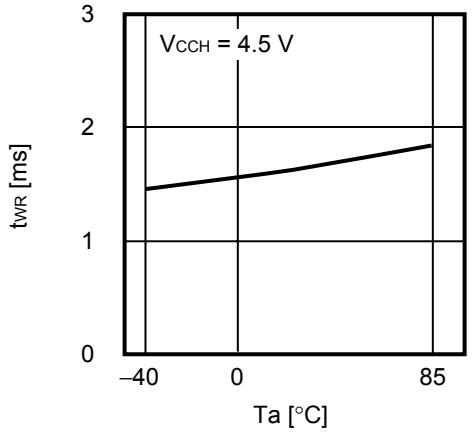
2.1 Maximum operating frequency $f_{MAX.}$ — Power supply voltage V_{CCH}



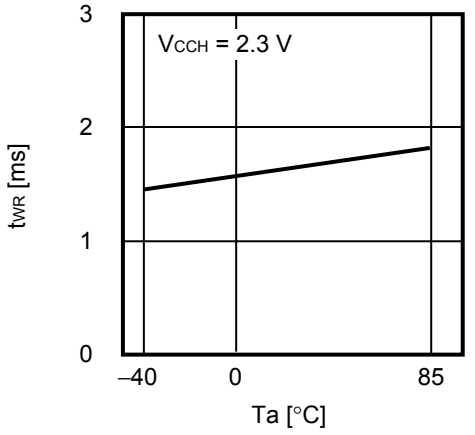
2.2 Write time t_{WR} — Power supply voltage V_{CCH}



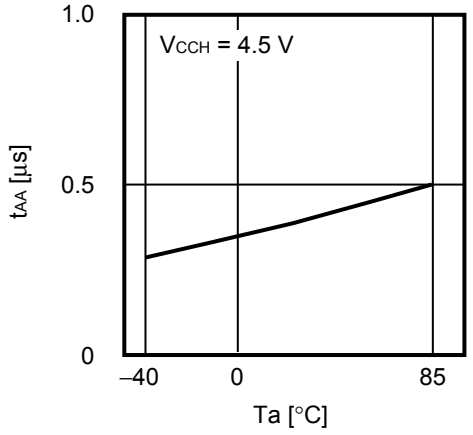
2.3 Write time t_{WR} — Ambient temperature Ta



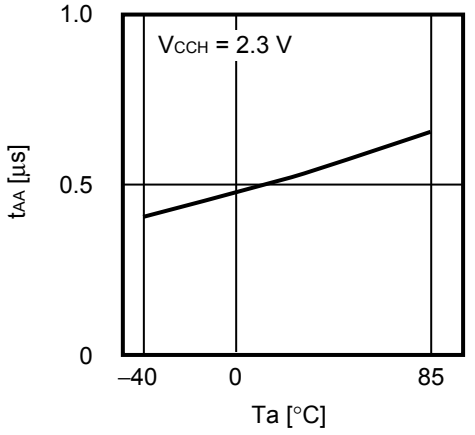
2.4 Write time t_{WR} — Ambient temperature Ta



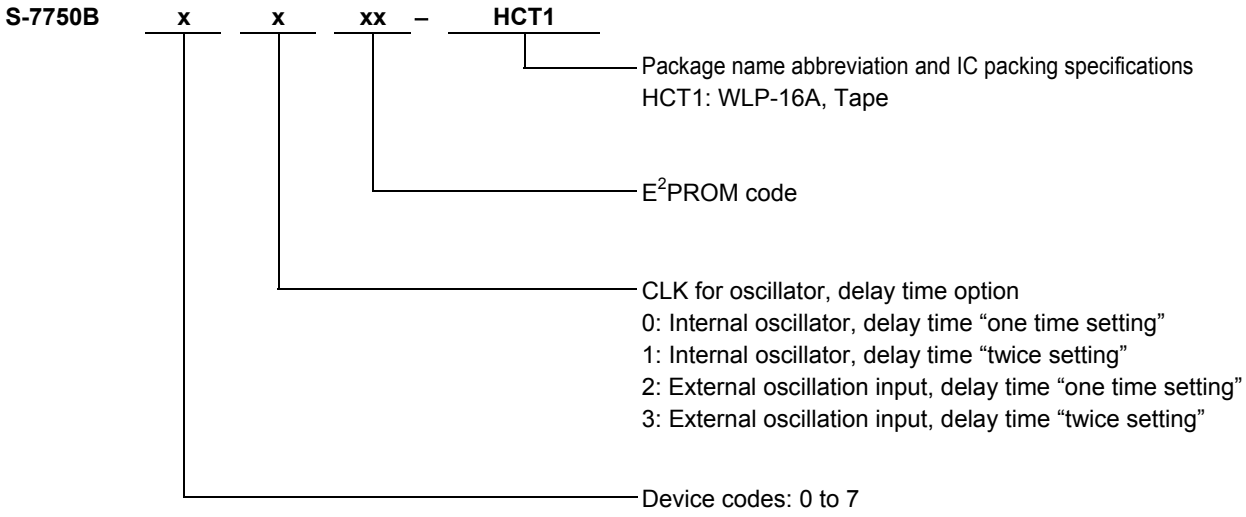
2.5 SDA output delay time t_{AA} — Ambient temperature Ta



2.6 SDA output delay time t_{AA} — Ambient temperature Ta

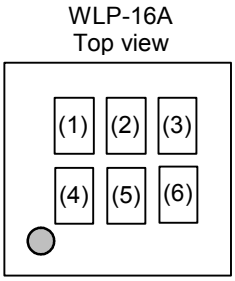


■ Product Name Structure



■ Marking Specifications

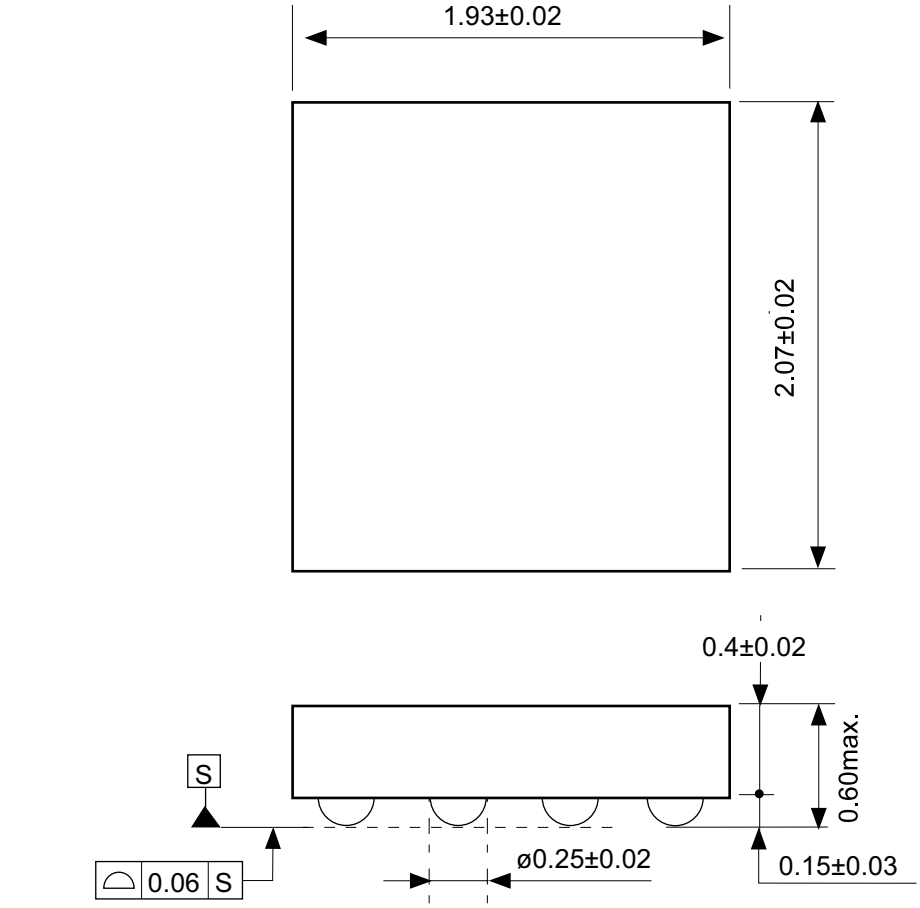
WLP-16A

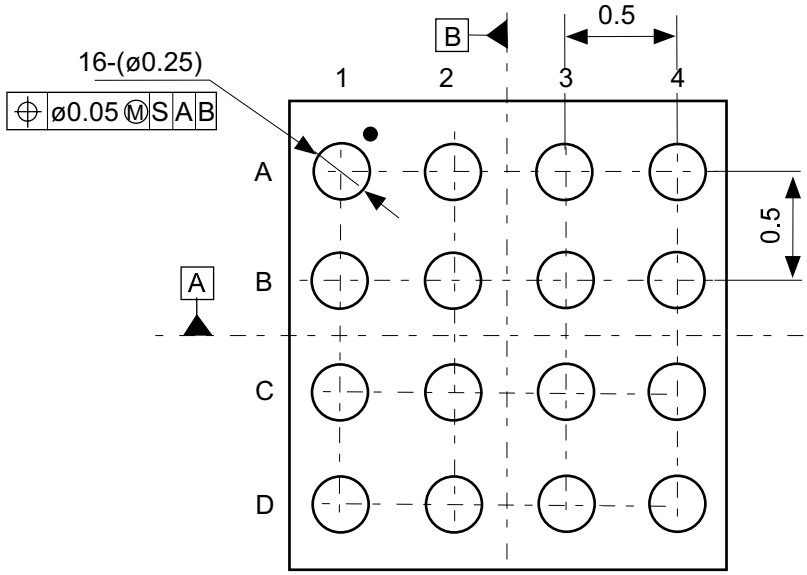


(1) to (4): Product abbreviation (refer to **Remark**)

(5) to (6): Lot number

Remark Please contact contact our sales office for the marking specifications of the product.

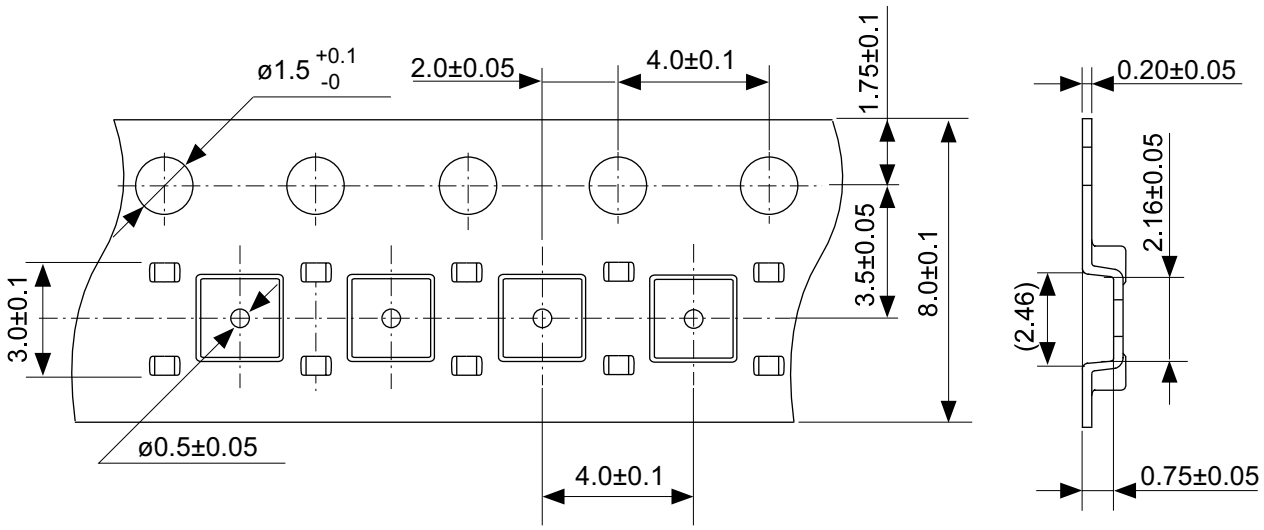


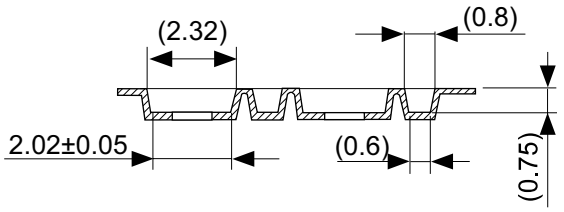


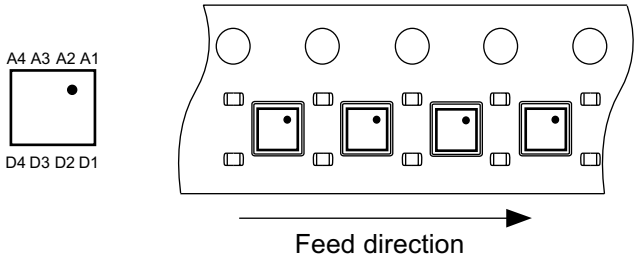
Pin No.	Pin name
A1	CLK
A2	SCL
A3	WP
A4	VCCH
B1	DO7
B2	VSS
B3	SDA
B4	DO0
C1	DO6
C2	TIMEN
C3	DO3
C4	DO1
D1	DO5
D2	DO4
D3	VCCL
D4	DO2

No. HA016-A-P-SD-1.0

TITLE	WLP-16A-A-PKG Dimensions
No.	HA016-A-P-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

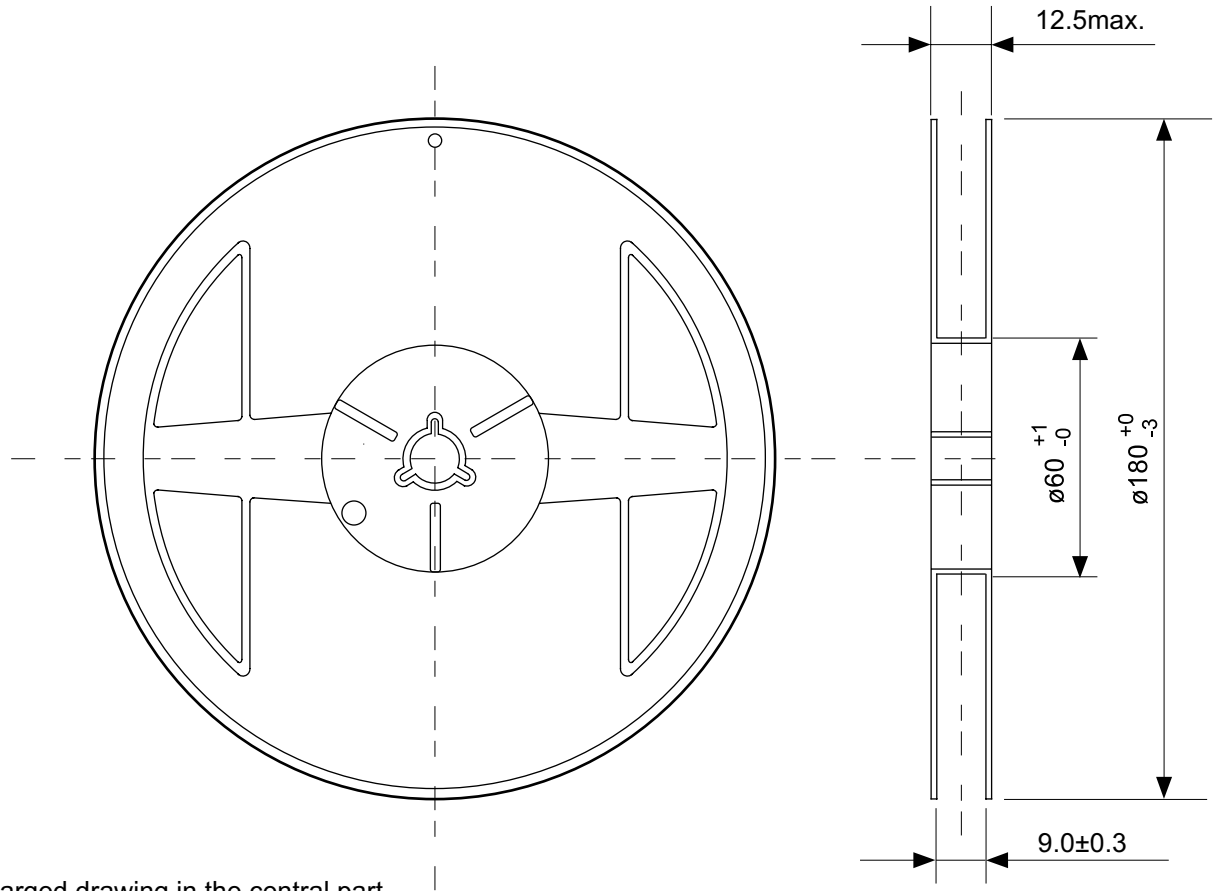




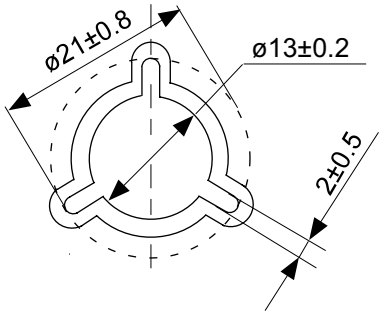


No. HA016-A-C-S1-1.0

TITLE	WLP-16A-A-Carrier Tape
No.	HA016-A-C-S1-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. HA016-A-R-SD-1.0

TITLE	WLP-16A-A-Reel		
No.	HA016-A-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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