VN5016AJ-E

SINGLE CHANNEL HIGH SIDE DRIVER WITH ANALOG CURRENT SENSE FOR AUTOMOTIVE APPLICATIONS

ADVANCE DATA

Table 1. General Features

TYPE	V_{CC}	$R_{DS(on)}$	I_D
VN5016AJ-E	41V	16mΩ	40A

- OUTPUT CURRENT: 40A
- 3.0V CMOS COMPATIBLE INPUT
- CURRENT SENSE DISABLE
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT AND POWER LIMITATION
- VERY LOW STAND-BY CURRENT
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW ELECTROMAGNETIC SUSCEPTIBILITY
- OPTIMIZED ELECTROMAGNETIC EMISSION
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package

PowerSSO-12

DESCRIPTION

The VN5016AJ-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open.
When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition.
Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-12	VN5016AJ-E	VN5016AJTR-E

Note: (*) See application schematic at page 8

Figure 2. Block Diagram

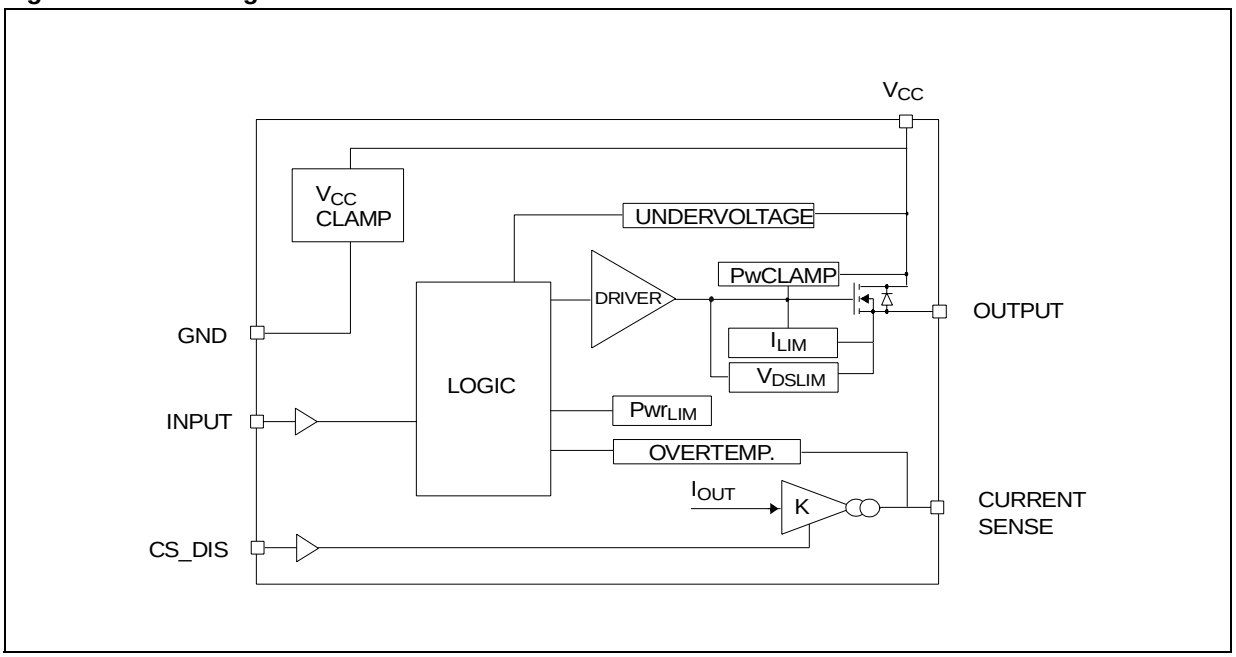


Table 3. Pin Function

Name	Function
V_{CC}	Battery connection
OUTPUT	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 3. Current and Voltage Conventions

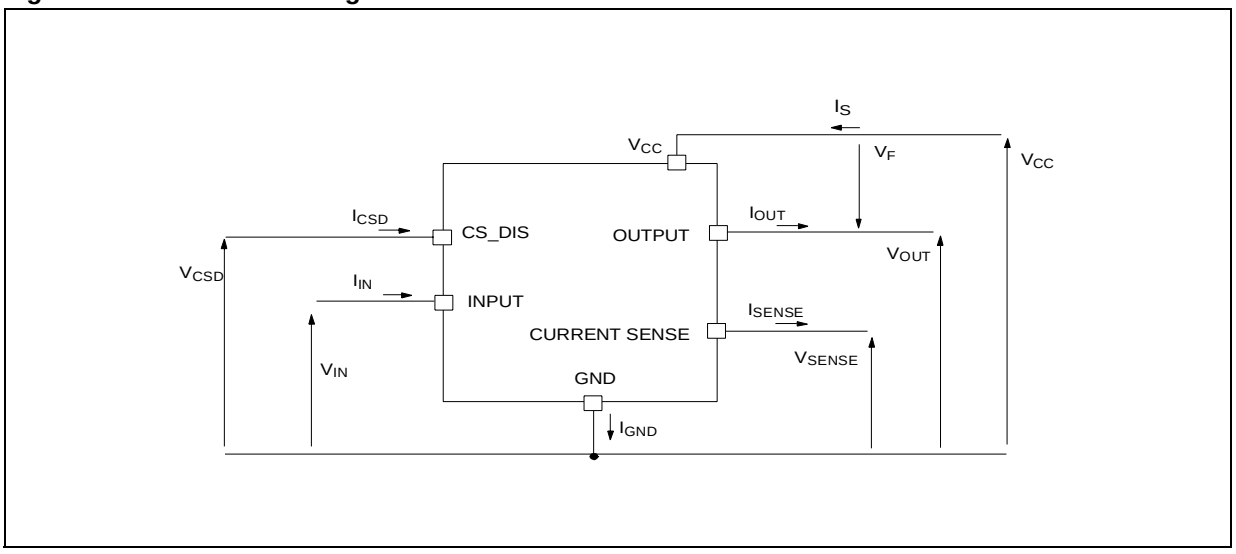
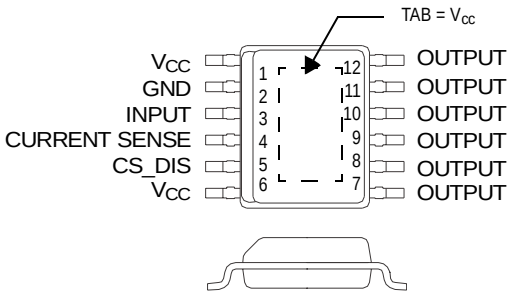


Figure 4. Configuration Diagram (Top View) & Suggested Connections For Unused and n.c. Pins



Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating		X	X	X	X
To Ground	Through 1KΩ resistor	X		Through 10KΩ resistor	Through 10KΩ resistor

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$- I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$- I_{OUT}$	Reverse DC output current	-30	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC}-41 $+V_{CC}$	V V
V_{ESD}	Electrostatic discharge (R=1.5kΩ; C=100pF)	2000	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

Table 5. Thermal Data

Symbol	Parameter	Max Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	75 (see note 1)	°C/W

Note: 1. When mounted on a standard single-sided FR4 board with 0.5cm^2 of Cu (at least 35 µm thick) connected to TAB.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C, unless otherwise specified)

Table 6. Power Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3	4.5	V
$V_{USDhyst}$	Undervoltage Shut-down hysteresis			0.5		V
R_{ON}	On state resistance	I_{OUT}=5A; T_j=25°C I_{OUT}=5A; T_j=150°C I_{OUT}=5A; V_{CC}=5V; T_j=25°C			16 32 20	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_S=20mA	41	46	52	V
I_S	Supply current	Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A		2(**) 1.5	5(**) 3	µA mA
$I_{L(off)}$	Off state output current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25°C V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125°C	0 0		3 5	µA

Note: (**) PowerMOS leakage included

Table 7. Switching (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L=2.6Ω		15		µs
$t_{d(off)}$	Turn-off delay time	R_L=2.6Ω		40		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω		0.3		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω		0.35		V/µs
W_{ON}	Switching losses energy at turn-on	R_L=2.6Ω		TBD		mJ
W_{OFF}	Switching losses energy at turn-off	R_L=2.6Ω		TBD		mJ

ELECTRICAL CHARACTERISTICS (continued)

Table 8. Logic Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN}=0.9V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN}=2.1V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	5.5	 -0.7	TBD	V V
V_{CSDL}	CS_DIS low level voltage				0.9	V
I_{CSDL}	Low level CS_DIS current	V_{CSD}=0.9V	1			µA
V_{CSDH}	CS_DIS high level voltage		2.1			V
I_{CSDH}	High level CS_DIS current	V_{CSD}=2.1V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD}=1mA I_{CSD}=-1mA	5.5	 -0.7	TBD	V V

Table 9. Protections and Diagnostics (see note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC Short circuit current	V_{CC}=13V 5V<V_{CC}<36V	40	60	80 80	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC}=13V T_R<T_j<T_{TSD}		24		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of STATUS		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD}-T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-46	V_{CC}-52	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.3A; T_j= -40°C...+150°C (see figure 9)		25		mV

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

ELECTRICAL CHARACTERISTICS (continued)

Table 10. Current Sense (8V<V_{CC}<16V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1.5A; V_{SENSE}=0.5V; V_{CSD}=0V; T_j= -40°C...150°C	TBD	5000	TBD	
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10A; V_{SENSE}=4V; V_{CSD}=0V; T_j=-40°C T_j=25°C...150°C	 TBD TBD	 5000 5000	 TBD TBD	
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=25A; V_{SENSE}=4V; V_{CSD}=0V; T_j=-40°C T_j=25°C...150°C	 TBD TBD	 5000 5000	 TBD TBD	
I_{SENSE0}	Analog sense current	I_{OUT}=0A; V_{SENSE}=0V; V_{CSD}=5V; V_{IN}=0V; T_j=-40°C...150°C V_{CSD}=0V; V_{IN}=5V; T_j=-40°C...150°C	 0 0		 5 10	 µA µA
V_{SENSE}	Max analog sense output voltage	I_{OUT}=15A; V_{CSD}=0V; R_{SENSE}=3.9KΩ	5			V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=3.9KΩ		9		V
I_{SENSEH}	Analog sense output current in overtemperature condition	V_{CC}=13V, V_{SENSE}=5V		8		mA
$t_{DSENSE1H}$	Delay Response time from falling edge of CS_DIS pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=90% of $I_{SENSE\ max}$ (see fig 5)		50	100	µs
$t_{DSENSE1L}$	Delay Response time from rising edge of CS_DIS pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=10% of $I_{SENSE\ max}$ (see fig 5)		5	20	µs
$t_{DSENSE2H}$	Delay Response time from rising edge of INPUT pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=90% of $I_{SENSE\ max}$ (see fig 5)		270	600	µs
$t_{DSENSE2L}$	Delay Response time from falling edge of INPUT pin	V_{SENSE}<4V, 1.5A<Iout<25A I_{SENSE}=10% of $I_{SENSE\ max}$ (see fig 5)		100	250	µs

Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE (V_{CSD}=0V) (see note 3)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Short circuit to GND	L H	L L	0 0
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Note: 3. If the V_{CSD} is high, the SENSE output is at a high impedance.

Figure 5.

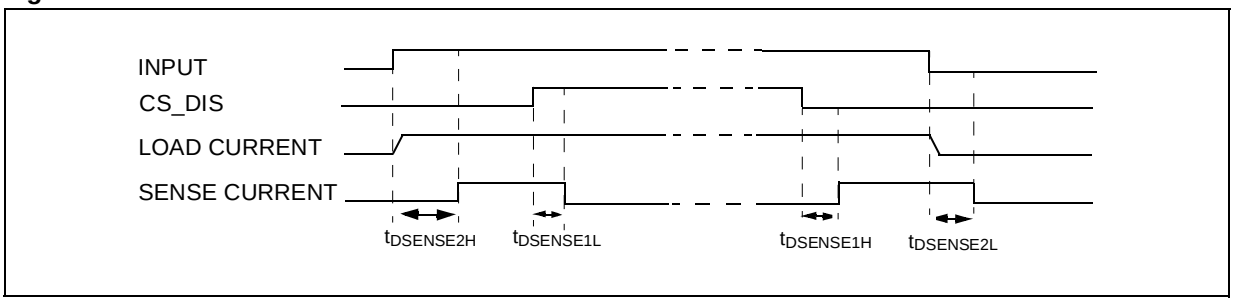


Figure 6. Switching Characteristics

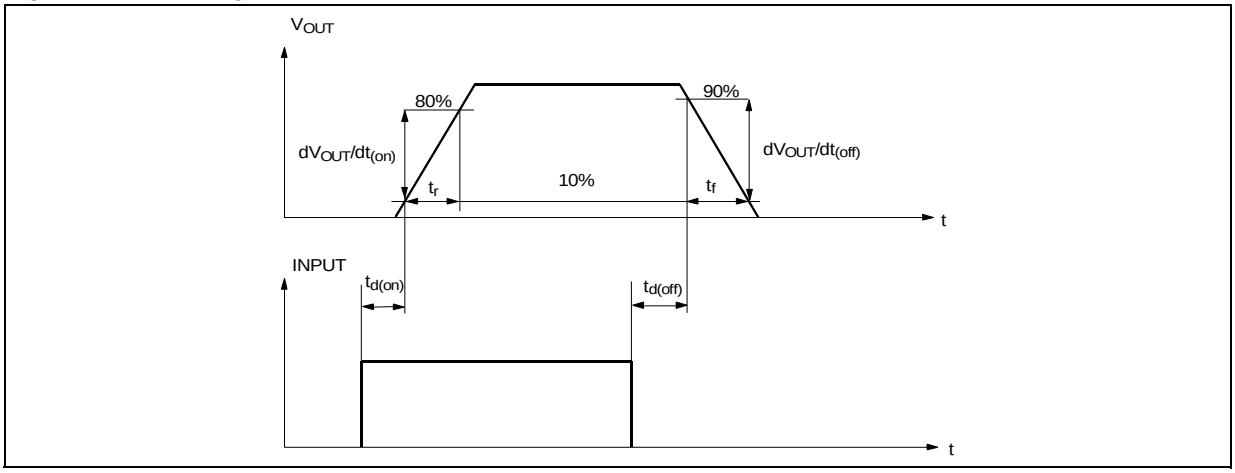


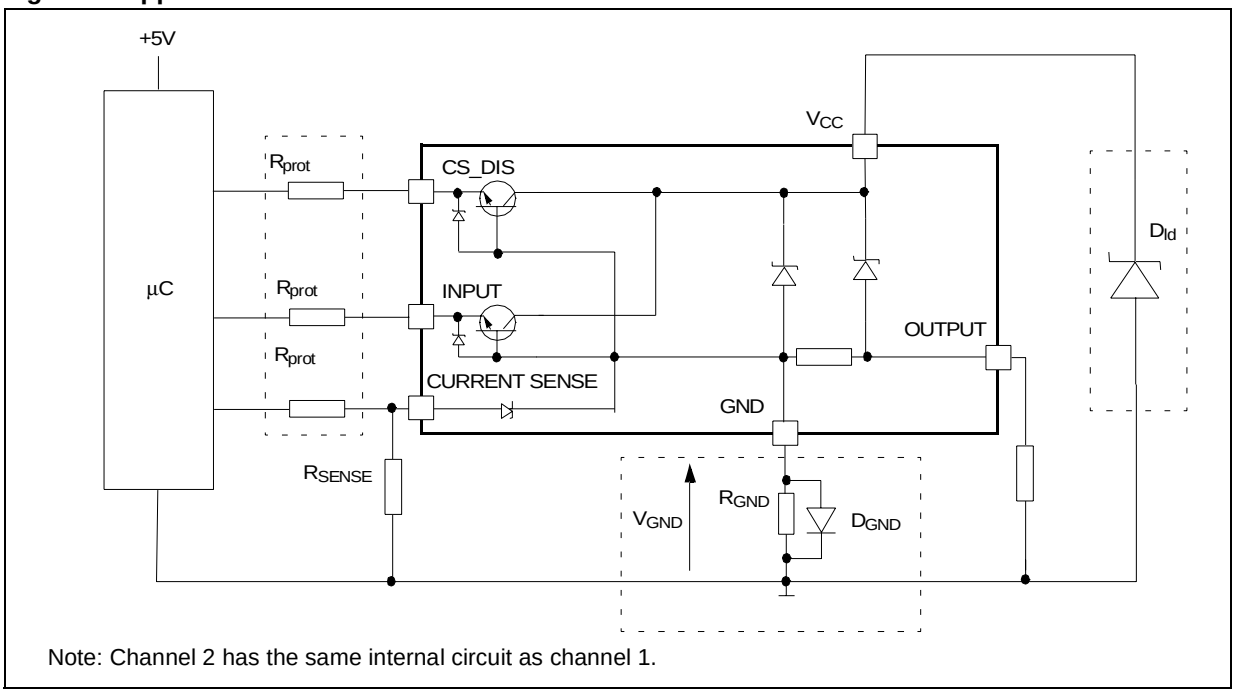
Table 12. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Application Schematic



Note: Channel 2 has the same internal circuit as channel 1.

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

Figure 8. Waveforms

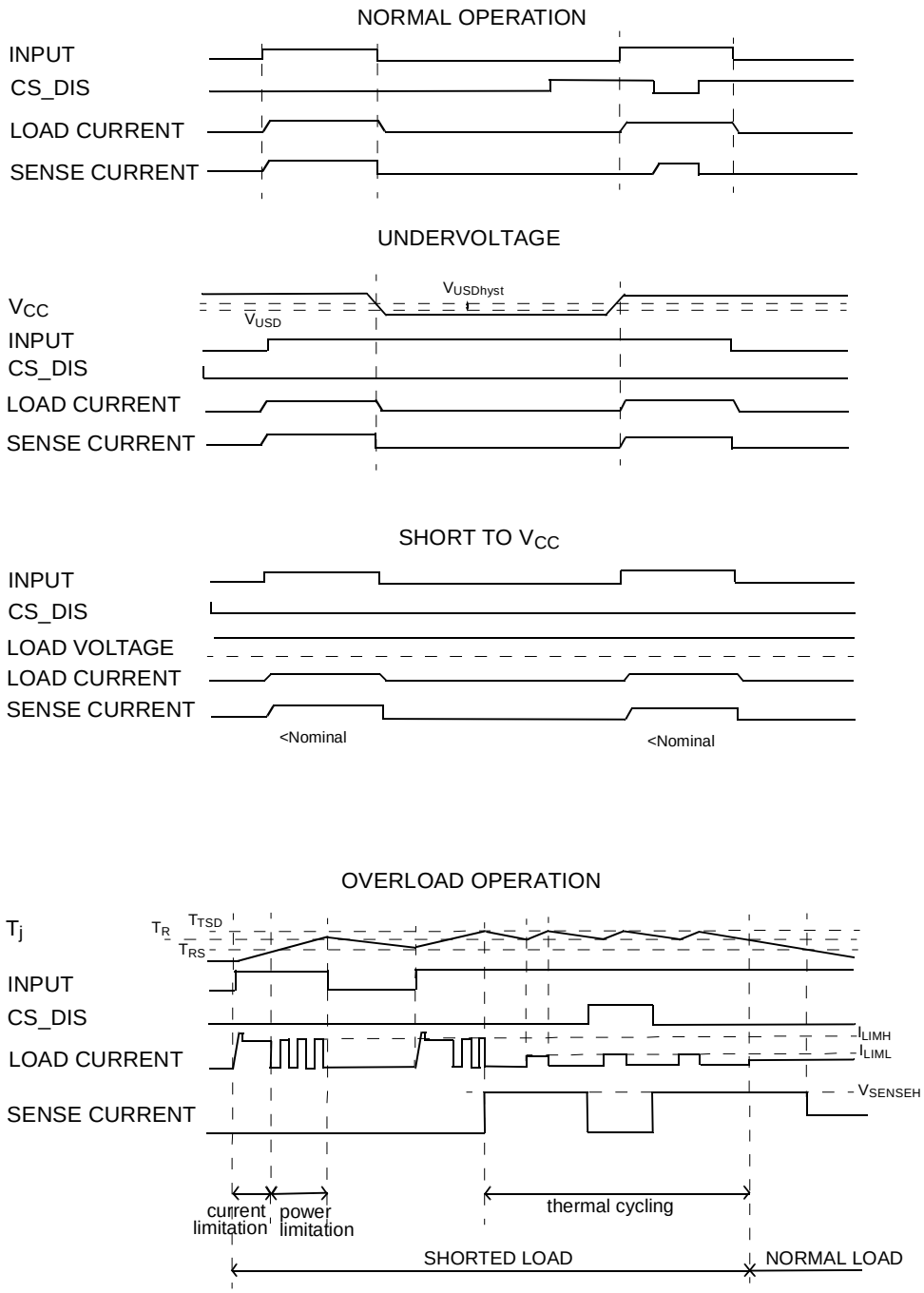
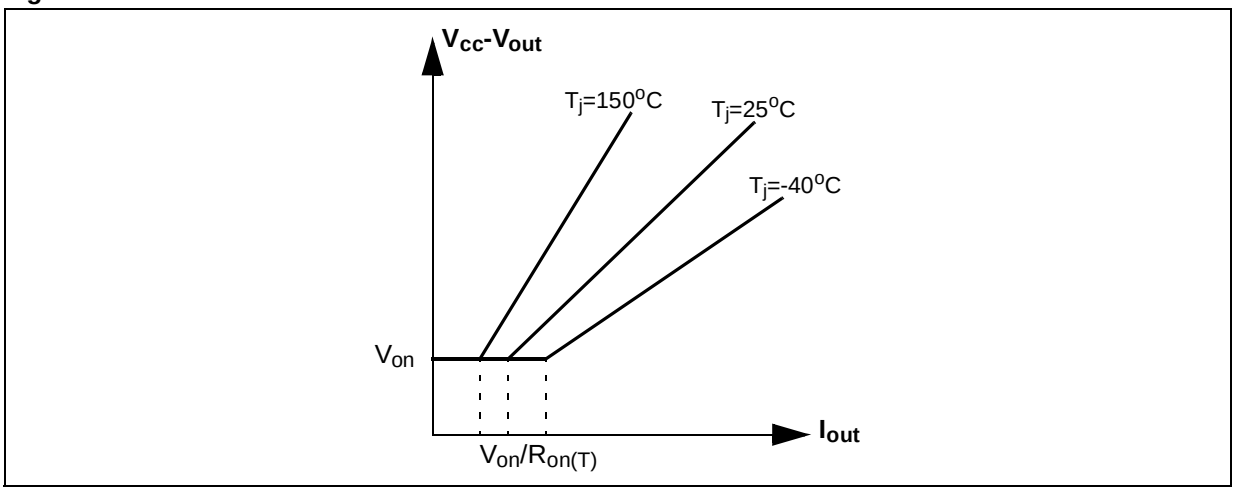


Figure 9.

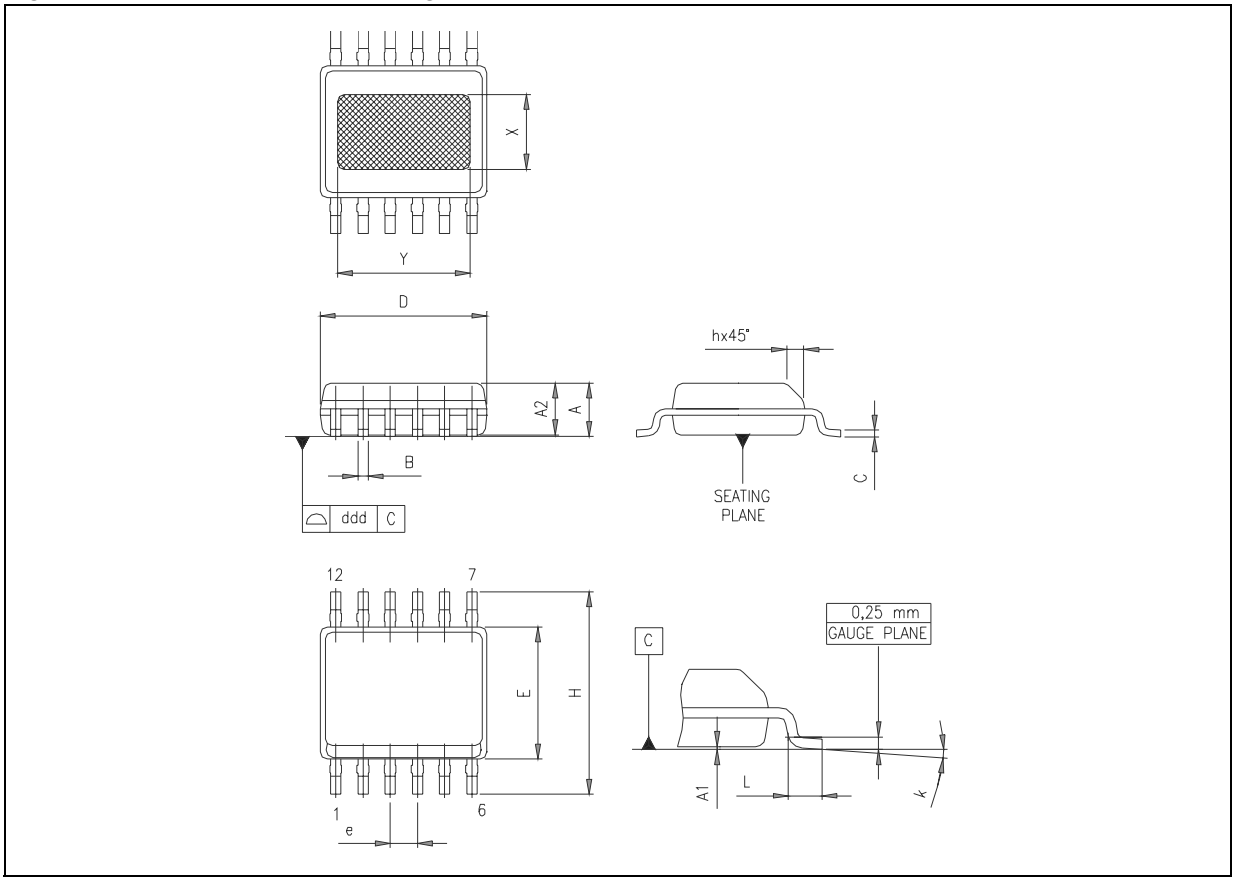


PACKAGE MECHANICAL

Table 13. PowerSSO-12™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0º		8º
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 10. PowerSSO-12™ Package Dimensions



REVISION HISTORY

Table 14. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	- First issue.
Jan. 2005	2	- Minor text changes.