500MHz Triple, Multiplexing Amplifiers

The ISL59446 (4:1) and ISL59448 (2:1) are fixed gain of 2 mux amps featuring high slew rates and excellent bandwidth for video switching. These devices feature a three-state output (HIZ) that enables the outputs of multiple devices to be wired together. A power-down mode ($\overline{\text{ENABLE}}$) is included to turn off un-needed circuitry in power sensitive applications. The $\overline{\text{ENABLE}}$ pin, when pulled high, sets the ISL59446 and ISL59448 into standby power mode - consuming just 18mW. An added feature in the ISL59448 is a latch enable function ($\overline{\text{LE}}$) that allows independent logic control using a common logic bus.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
ISL59448IAZ (See Note)	24 Ld QSOP (Pb-free)	-	MDP0040
ISL59448IAZ-T7 (See Note)	24 Ld QSOP (Pb-free)	7”	MDP0040
ISL59448IAZ-T13 (See Note)	24 Ld QSOP (Pb-free)	13”	MDP0040
ISL59448IRZ (See Note)	24 Ld Exposed Pad QFN (Pb-free)	-	MDP0046
ISL59448IRZ-T7 (See Note)	24 Ld Exposed Pad QFN (Pb-free)	7”	MDP0046
ISL59448IRZ-T13 (See Note)	24 Ld Exposed Pad QFN (Pb-free)	13”	MDP0046
ISL59446IRZ (See Note)	32 Ld Exposed Pad 3.6 x 4.6 QFN (Pb-free)	-	MDP0046
ISL59446IRZ-T7 (See Note)	32 Ld Exposed Pad 3.6 x 4.6 QFN (Pb-free)	7”	MDP0046
ISL59446IRZ-T13 (See Note)	32 Ld Exposed Pad 3.6 x 4.6 QFN (Pb-free)	13”	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Triple 2:1 (ISL59448) and 4:1 (ISL59446) multiplexers for RGB
- Internally set gain-of-2
- High speed three-state outputs (HIZ)
- Power-down mode ($\overline{\text{ENABLE}}$)
- Latch enable (ISL59448)
- ±5V operation
- ±1600 V/µs slew rate
- 500MHz bandwidth
- Supply current 16mA/ch (ISL59446) and 11mA/ch (ISL59448)
- Pb-free plus anneal available (RoHS compliant)

Applications

- HDTV/DTV analog inputs
- Video projectors
- Computer monitors
- Set-top boxes
- Security video
- Broadcast video equipment

TABLE 1. CHANNEL SELECT LOGIC TABLE ISL59448

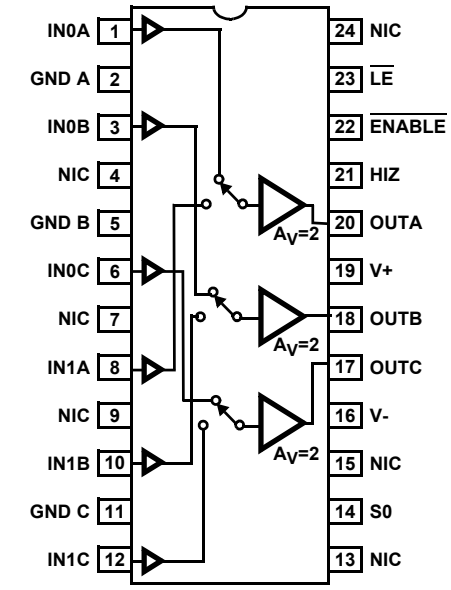
S0	$\overline{\text{ENABLE}}$	HIZ	$\overline{\text{LE}}$	OUTPUT
0	0	0	0	INO (A, B, C)
1	0	0	0	IN1 (A, B, C)
X	1	X	X	Power-down
X	0	1	X	High Z
X	0	0	1	Last S0 State Preserved

TABLE 2. CHANNEL SELECT LOGIC TABLE ISL59446

S1	S0	$\overline{\text{ENABLE}}$	HIZ	OUTPUT
0	0	0	0	IN0 (A, B, C)
0	1	0	0	IN1 (A, B, C)
1	0	0	0	IN2 (A, B, C)
1	1	0	0	IN3 (A, B, C)
X	X	1	X	Power-down
X	X	0	1	High Z

Pinouts

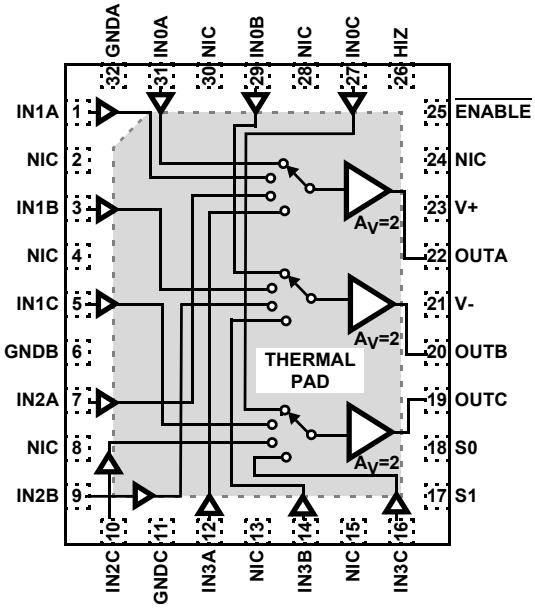
ISL59448
(24 LD QSOP)
TOP VIEW



LATCHED ON HIGH $\overline{LE}$

NIC = NO INTERNAL CONNECTION

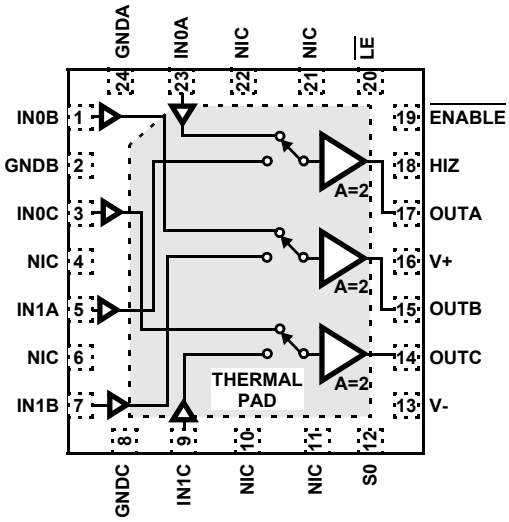
ISL59446
(32 LD QFN)
TOP VIEW



THERMAL PAD INTERNALLY CONNECTED TO V-. PAD MUST BE TIED TO V-

NIC = NO INTERNAL CONNECTION

ISL59448
(24 LD QFN)
TOP VIEW

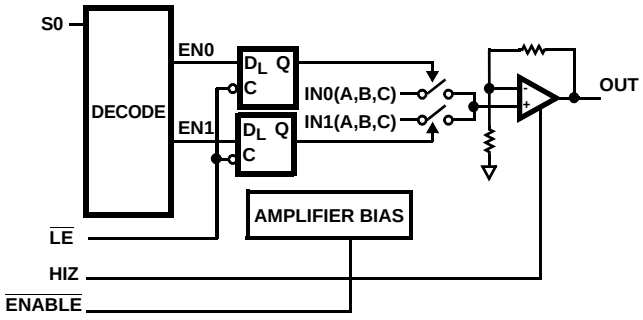


THERMAL PAD INTERNALLY CONNECTED TO V-. PAD MUST BE TIED TO V-

LATCHED ON HIGH $\overline{LE}$

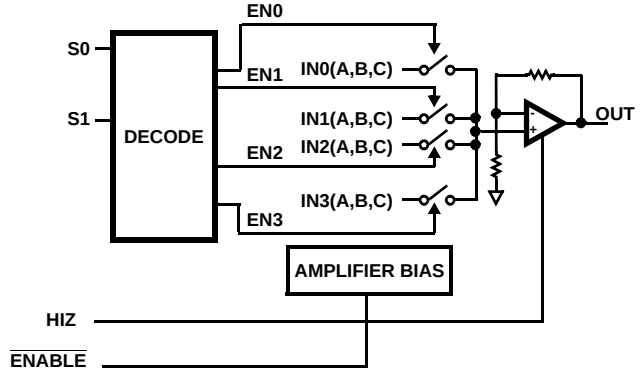
NIC = NO INTERNAL CONNECTION

Functional Diagram ISL59448



A logic high on $\overline{LE}$ will latch the last S0 state. This logic state is preserved when cycling HIZ or $\overline{ENABLE}$ functions.

Functional Diagram ISL59446



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V+ to V-). 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate 1V/µs
Digital & Analog Input Current (Note 1) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7). . . .2500V
Machine Model 300V

Storage Temperature Range . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . .-40°C to +125°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = 25°C, Vout = +/-2V_{P-P} & R_L = 500Ω to GND, C_L = 0pF unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
±I_S Enabled	Enabled Supply Current (ISL59448)	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low		30		mA
	Enabled Supply Current (ISL59446)			46		mA
+I_S Disabled	Disabled Supply Current (ISL59448)	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ High		2.8		mA
	Disabled Supply Current (ISL59446)	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ High		3.5		mA
-I_S Disabled	Disabled Supply Current	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ High		10		µA
V_{OUT}	Positive and Negative Output Swing	R_L = 500Ω		±3.4		V
I_{OUT}	Output Current	R_L = 10Ω to GND		±135		mA
V_{OS}	Output Offset Voltage (ISL59448)			±15		mV
V_{OS}	Output Offset Voltage (ISL59446)			±10		mV
Ib	Input Bias Current	V_{IN} = 0V		-2		µA
R_{OUT}	HIZ Output Resistance	HIZ = Logic High		920		Ω
R_{OUT}	Enabled Output Resistance	HIZ = Logic Low		0.2		Ω
R_{IN}	Input Resistance	V_{IN} = ±1.75V		10		MΩ
A_{CL} or A_V	Voltage Gain	R_L= 500Ω		2		V/V
I_{TRI}	Output Current in Three-state	V_{OUT} = 0V	8	15		µA
LOGIC						
V_{IH}	Input High Voltage (Logic Inputs)			2		V
V_{IL}	Input Low Voltage (Logic Inputs)			0.8		V
I_{IH}	Input High Current (Logic Inputs)	V_H = 5V		270		µA
I_{IL}	Input Low Current (Logic Inputs)	V_L = 0V		2		µA
AC GENERAL						
t_S	0.1% Settling Time	Vout step = 1V		TBD		ns
PSRR (ISL59448)	Power Supply Rejection Ratio	DC, PSRR V+ & V- combined Vout = 0dBm		TBD		dB
PSRR (ISL59446)	Power Supply Rejection Ratio	DC, PSRR V+ & V- combined Vout = 0dBm		TBD		dB

Electrical Specifications V+ = +5V, V- = -5V, GND = 0V, T_A = 25°C, Vout = +/-2V_{P-P} & R_L = 500Ω to GND, C_L = 0pF unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
ISO	Channel Isolation	f = 10MHz, Ch-Ch X-Talk and Off Isolation, Vout = 0dBm; C_L = 1.5pF		TBD		dB
dG	Differential Gain Error	NTC-7, RL = 150, C_L = 1.5pF		TBD		%
dP	Differential Phase Error	NTC-7, RL = 150, C_L = 1.5pF		TBD		°
BW	-3dB Bandwidth			500		MHz
FBW	0.1dB Bandwidth			TBD		MHz
	0.1dB Bandwidth			TBD		MHz
SR	Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L = 1.5pF		±1600		V/µs
SWITCHING CHARACTERISTICS						
V_{GLITCH}	Channel -to-Channel Switching Glitch	V_{IN} = 0V, C_L = 1.5pF		TBD		mV_{P-P}
ISL59448	$\overline{\text{Enable}}$ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		TBD		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		TBD		mV_{P-P}
V_{GLITCH}	Channel -to-Channel Switching Glitch	V_{IN} = 0V C_L = 1.5pF		TBD		mV_{P-P}
ISL59446	$\overline{\text{Enable}}$ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		TBD		mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V C_L = 1.5pF		TBD		mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low to High	1.2V logic threshold to 10% movement of analog output		18		ns
t_{SW-H-L}	Channel Switching Time High to Low	1.2V logic threshold to 10% movement of analog output		20		ns
tr, tf	Rise & Fall Time	10% to 90%		1.1		ns
tpd	Propagation Delay	10% to 10%		0.9		ns
t_{LH}	Latch Enable Hold time (ISL59448 only)	$\overline{\text{LE}}$ = 0		10		ns

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = 25°C, unless otherwise specified.

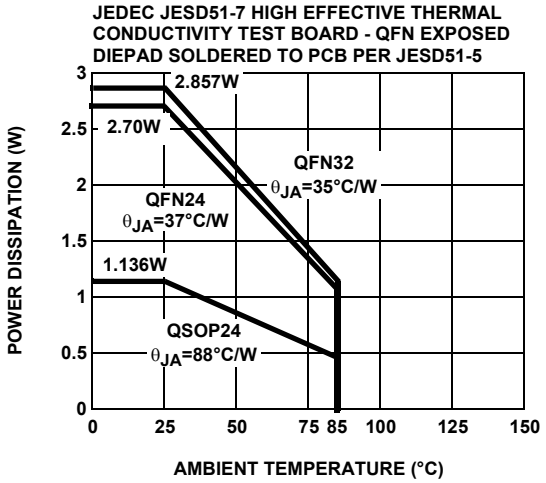


FIGURE 1. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

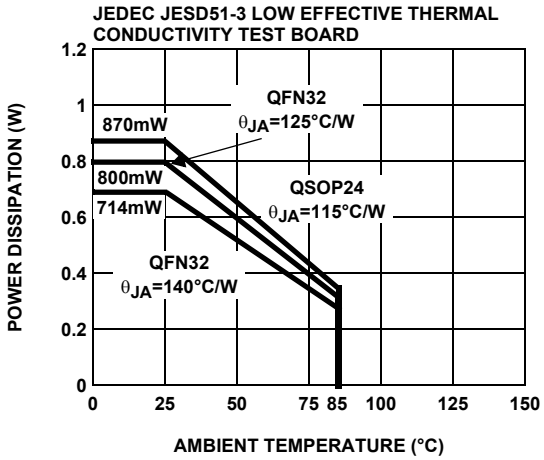
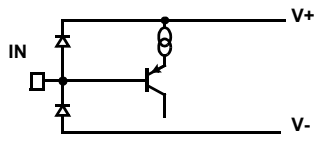
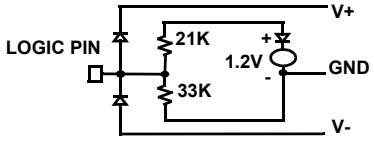


FIGURE 2. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

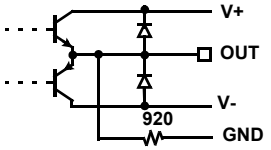
IISL59446 (32 LD QFN)	ISL59448 (24 LD QFN)	ISL59448 (24 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	5	8	IN1A	Circuit 1	Channel 1 input for output amplifier "A"
2, 4, 8, 13, 15, 24, 28, 30	4, 6, 10, 11, 21, 22	4, 7, 9, 13, 15, 24	NIC		**N**ot **I**nternally **C**onnected; it is recommended these pins be tied to ground to minimize crosstalk.
3	7	10	IN1B	Circuit 1	Channel 1 input for output amplifier "B"
5	9	12	IN1C	Circuit 1	Channel 1 input for output amplifier "C"
6	2	5	GNDB	Circuit 4	Ground pin for output amplifier “B”
7		NA	IN2A	Circuit 1	Channel 2 input for output amplifier "A"
9		NA	IN2B	Circuit 1	Channel 2 input for output amplifier "B"
10		NA	IN2C	Circuit 1	Channel 2 input for output amplifier "C"
11	8	11	GNDC	Circuit 4	Ground pin for output amplifier “C”
12		NA	IN3A	Circuit 1	Channel 3 input for output amplifier "A"
14		NA	IN3B	Circuit 1	Channel 3 input for output amplifier "B"
16		NA	IN3C	Circuit 1	Channel 3 input for output amplifier "C"
17		NA	S1	Circuit 2	Channel selection pin MSB (binary logic code)
18	12	14	S0	Circuit 2	Channel selection pin. LSB (binary logic code)
19	14	17	OUTC	Circuit 3	Output of amplifier “C”
20	15	18	OUTB	Circuit 3	Output of amplifier “B”
21	13	16	V-	Circuit 4	Negative power supply
22	17	20	OUTA	Circuit 3	Output of amplifier “A”
23	16	19	V+	Circuit 4	Positive power supply
25	19	22	$\overline{\text{ENABLE}}$	Circuit 2	Device enable (active low) w/Internal pull-down resistor. A logic High puts device into power-down mode with the only logic circuitry active. All logic states are preserved post power-down. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
	20	23	$\overline{\text{LE}}$	Circuit 2	Device latch enable on the ISL59424. A logic high on $\overline{\text{LE}}$ will latch the last (S0, S1) logic state. HIZ and $\overline{\text{ENABLE}}$ functions are not latched with the $\overline{\text{LE}}$ pin.
26	18	21	HIZ	Circuit 2	Output disable (active high) w/internal pull-down resistor. A logic high, puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line.
27	3	6	IN0C	Circuit 1	Channel 0 for output amplifier "C"
29	1	3	IN0B	Circuit 1	Channel 0 for output amplifier "B"
31	23	1	IN0A	Circuit 1	Channel 0 for output amplifier "A"
32	24	2	GNDA	Circuit 4	Ground pin for output amplifier “A”



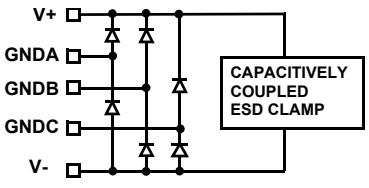
CIRCUIT 1



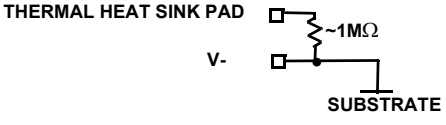
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



AC Test Circuits

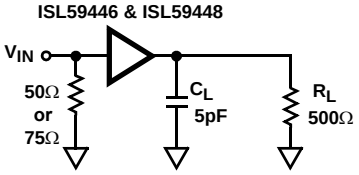


FIGURE 3A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

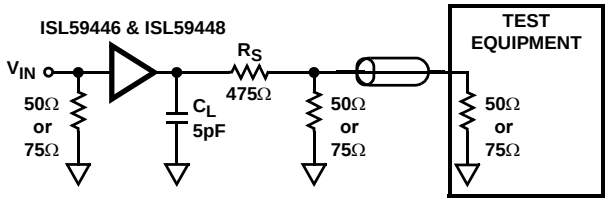


FIGURE 3B. TEST CIRCUIT FOR MEASURING WITH 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

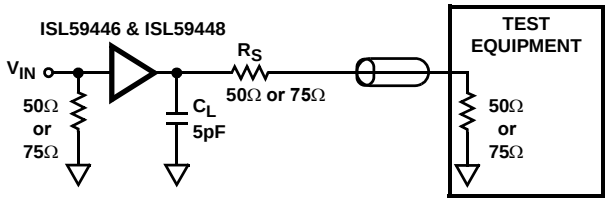


FIGURE 3C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

FIGURE 3. TEST CIRCUITS

Figure 3A illustrates the optimum output load for testing AC performance. Figure 3B illustrates the optimun output load when connecting to 50Ω input terminated equipment.

Application Information

General

The ISL59446 and ISL59448 triple 4:1 and 2:1 MUX amps are ideal as the matrix element of high performance switchers and routers. Key features include a fixed gain of 2, buffered high impedance analog inputs and excellent AC performance at output loads down to 150Ω for video cable-driving. The current feedback output amplifiers are stable operating into capacitive loads.

For the best isolation and crosstalk rejection, all GND pins and NIC pins must connect to the GND plane.

Control Signals

S0, S1, $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ - These are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select the inputs. All three amplifiers are switched simultaneously from their respective inputs. The $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ pins are used to disable the part to save power, latch in the last logic state and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

Power-up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT- triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the Pin Description table. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 4) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+

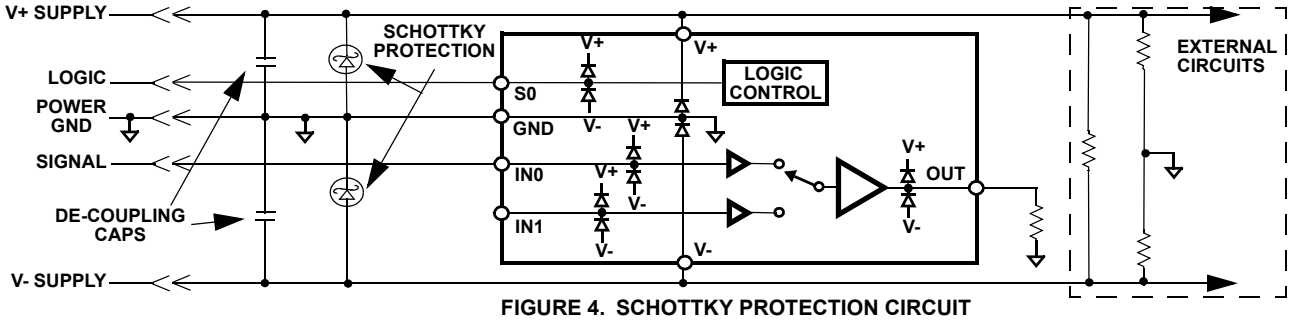


FIGURE 4. SCHOTTKY PROTECTION CIRCUIT

HIZ State

An internal pull-down resistor ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 15ns (Figure 16) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output impedance is 920Ω, enabling up to two additional devices to share a common output. The supply current during this state is same as the active state.

$\overline{\text{ENABLE}}$ and Power-down States

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{ENABLE}}$ pin. The Power-down state is established within approximately 80ns (Figure 14), if a logic high (>2V) is placed on the $\overline{\text{ENABLE}}$ pin. In the Power-down state, the output has no leakage but has a large variable capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA., therefore, the parallel connection of multiple outputs is not recommended unless the application can tolerate the limited powerdown output impedance.

$\overline{\text{LE}}$ State

The ISL59448 is equipped with a Latch Enable pin. A logic high (>2V) on the $\overline{\text{LE}}$ pin latches the last logic state. This logic state is preserved when cycling HIZ or $\overline{\text{ENABLE}}$ functions.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip line are used.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible - Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

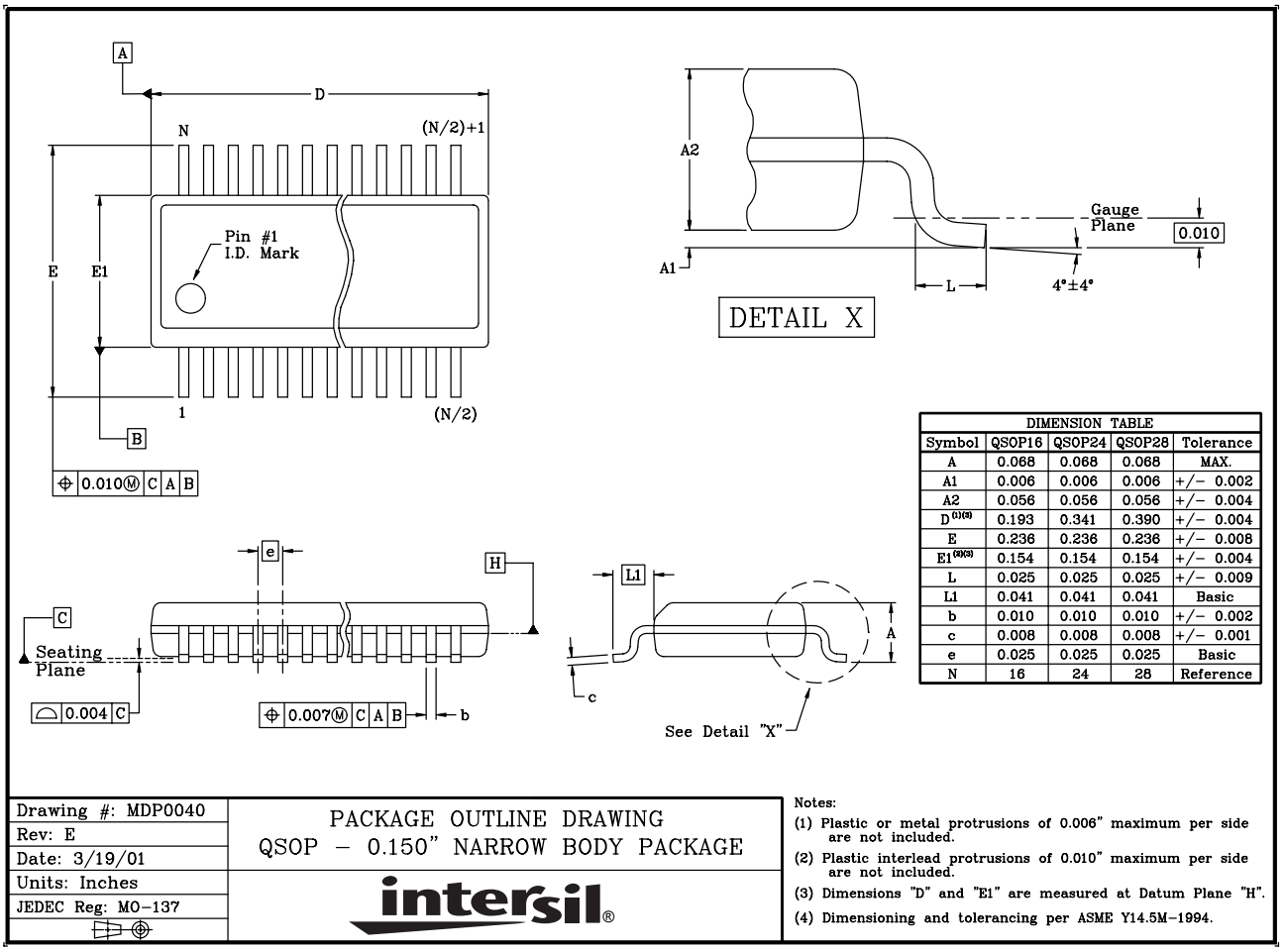
The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the V- supply through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Do **not** tie this pin to GND as this could result in large back biased currents flowing between GND and V-. The ISL59446 uses the package with pad dimensions of D2 = 2.48mm and E2 = 3.4mm.

Maximum AC performance is achieved if the thermal pad is attached to a dedicated de-coupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible a 1” x 1” pad area is sufficient for the ISL59446 that is dissipating 0.5W in +50°C ambient. Pad area requirements should be evaluated on a case by case basis.

QSOP Package Outline Drawing



DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/− 0.002
A2	0.056	0.056	0.056	+/− 0.004
D(1)(3)	0.193	0.341	0.390	+/− 0.004
E	0.236	0.236	0.236	+/− 0.008
E1(2)(3)	0.154	0.154	0.154	+/− 0.004
L	0.025	0.025	0.025	+/− 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/− 0.002
c	0.008	0.008	0.008	+/− 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040	PACKAGE OUTLINE DRAWING QSOP – 0.150" NARROW BODY PACKAGE
Rev: E	
Date: 3/19/01	
Units: Inches	
JEDEC Reg: MO-137	

Notes:

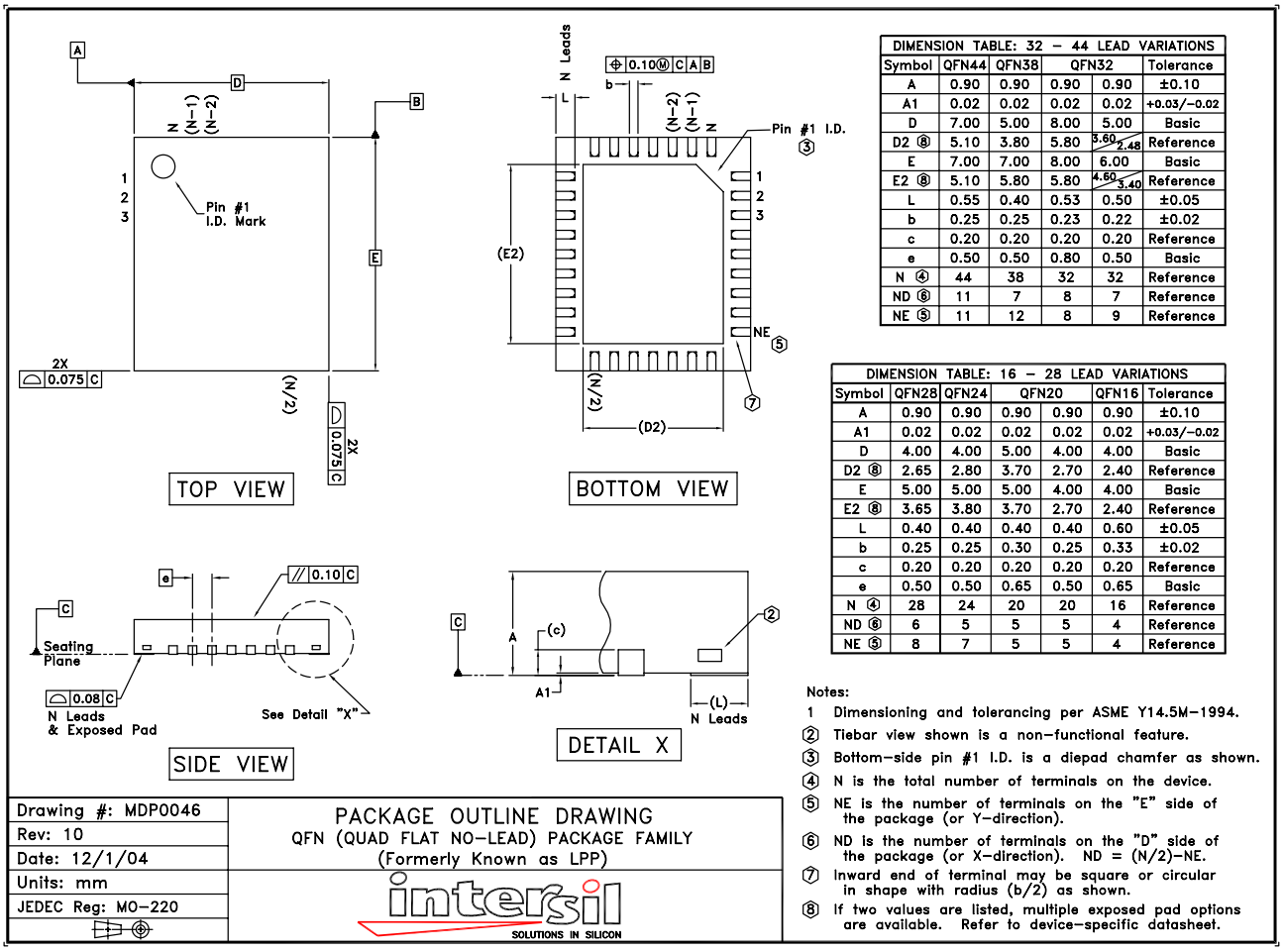
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M–1994.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/–0.02
D	7.00	5.00	8.00	5.00	Basic
D2 ⑧	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 ⑧	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N ④	44	38	32	32	Reference
ND ⑥	11	7	8	7	Reference
NE ⑤	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/–0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 ⑧	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 ⑧	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N ④	28	24	20	20	16	Reference
ND ⑧	6	5	5	5	4	Reference
NE ⑤	8	7	5	5	4	Reference

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

NOTE: The package drawings shown here may not be the latest versions. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp