ComLink™ Series
CY2DL814
1:4 Clock Fanout Buffer

Features

- Low-voltage operation
- V_{DD} = 3.3V
- 1:4 Fanout
- Single-input configurable for
  - — LVDS, LVPECL, or LVTTL
  - — Four differential pairs of LVDS outputs
- Drives 50- or 100-ohm load (selectable)
- Low input capacitance
- 85 ps typical output-to-output skew
- <4 ns typical propagation delay
- Does not exceed Bellcore 802.3 standards
- Operation at ⇒ 350 MHz – 700 Mbps
- Industrial versions available
- Packages available include TSSOP/SOIC

Description

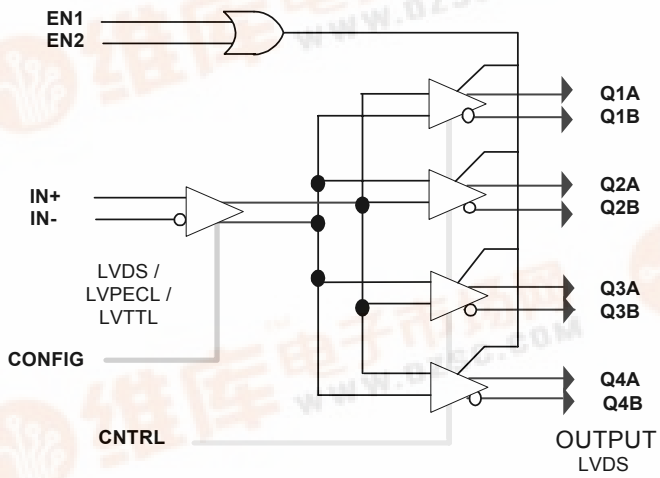
The Cypress CY2 series of network circuits is produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic.

The Cypress CY2DL814 fanout buffer features a single LVDS-, LVPECL-, or LVTTL-compatible input and four LVDS output pairs.

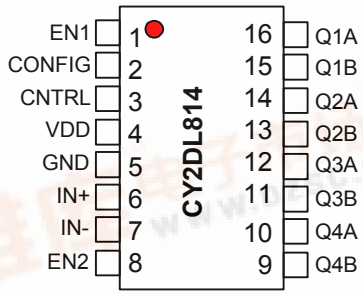
Designed for data-communication clock management applications, the fanout from a single input reduces loading on the input clock.

The CY2DL814 is ideal for both level translations from single ended to LVDS and/or for the distribution of LVDS-based clock signals. The Cypress CY2DL814 has configurable input and output functions. The input can be selectable for LVPECL/LVTTL or LVDS signals while the output driver's support standard and high drive LVDS. Drive either a 50-ohm or 100-ohm line with a single part number/device.

Block Diagram



Pin Configuration



16-pin TSSOP/SOIC

Pin Description

Pin Number	Pin Name	Pin Standard Interface	Description
6,7	IN+, IN–	Configurable	Differential input pair or single line. LVPECL default. See config below.
3	CNTRL	LVTTL/LVCMOS	Converts into a High drive driver from a standard LVDS. Standard drive (logic = 0) B/High drive/Bus (logic = 1)
2	CONFIG	LVTTL/LVCMOS	Converts inputs (IN^+/IN^-), (EN, EN#) from the default LVPECL/LVDS (logic = 0) To LVTTL/LVCMOS (logic = 1)
1,8	EN1, EN2	LVTTL/LVCMOS	Enable/disable logic. See *Table 1* below for details.
16,15,14,13 12,11,10,9	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B	LDVS	Differential outputs.
4	V_{DD}	POWER	Positive supply voltage
5	G_{ND}	POWER	Ground

Maximum Ratings[1, 2]

Storage Temperature: .....–65°C to + 150°C

Ambient Temperature:.....–40°C to +85°C

Supply Voltage to Ground Potential (Inputs and V_{CC} only)..... –0.3V to 4.6V

Supply Voltage to Ground Potential (Outputs only)..... –0.3V to V_{DD} + 0.3V

DC Input Voltage ..... –0.3V to V_{DD} + 0.3V

DC Output Voltage..... –0.3V to V_{DD} + 0.9V

Power Dissipation..... 0.75W

Table 1. EN1 EN2 Function Table–Differential Input Mode

Enable Logic		Input		Outputs	
EN1	**EN2**	**IN+**	**IN–**	**QnA**	**QnB**
H	X	H	L	H	L
H	X	L	H	L	H
X	L	H	L	H	L
X	L	L	H	L	H
L	H	X	X	Z	Z

Table 2. Output Drive Control for Standard and Bus/B/High Drive B

CNTRL Pin 3 Binary Value	Drive STD	Impedance	Output Voltage Value
0	Standard	100 ohm	V0 = Voutput
		50 ohm	V = 1/2 * V0
1	High Drive/Bus/B	100 ohm	V = 2 * V0
		50 ohm	V = V0

Notes:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Table 3. Input Receiver Configuration for Differential or LVTTL/LVCMOS

CONFIG Pin 2 Binary Value	Input Receiver Family	Input Receiver Type
1	LVTTL in LVCMOS	Single-ended, Non-inverting, Inverting, Void of Bias Resistors
0	LVDS	Low-voltage Differential Signaling
	LVPECL	Low-voltage Pseudo (Positive) Emitter Coupled Logic

Table 4. Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal

LVTTL/LVCMOS Input Logic			
Input Condition		Input Logic	Output Logic Q Pins, Q1A or Q1
Ground	IN– Pin 7		
	IN+ Pin 6	Input	True
V_{CC}	IN– Pin 7		
	IN+ Pin 6	Input	Invert
Ground	IN+ Pin 6		
	IN– Pin 7	Input	True
V_{CC}	IN+ Pin 6		
	IN– Pin 7	Input	Invert

Table 5. Power Supply Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CCD}	Dynamic Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open		1.5	2.0	mA/MHz
I_C	Total Power Supply Current	V_{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open fL=100 MHz		90	100	mA

Table 6. D.C Electrical Characteristics: 3.3V–LVDS Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{ID}	Magnitude of Differential Input Voltage			100		600	mV
V_{IC}	Common-mode of Differential Input Voltage $\|V_{ID}\|$ (min. and max.)			$\|V_{ID}\|/2$	2.4–($\|V_{ID}\|/2$)		V
V_{IH}	Input High Voltage	Guaranteed Logic High Level	Config/Cntrl Pins	2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD} = Max.	$V_{IN} = V_{DD}$		±10	±20	µA
I_{IL}	Input Low Current	V_{DD} = Max.	$V_{IN} = V_{SS}$		±10	±20	µA
I_I	Input High Current	V_{DD} = Max., $V_{IN} = V_{DD}$(max.)				±20	µA

Table 7. D.C Electrical Characteristics: 3.3V–LVPECL Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{ID}	Differential Input Voltage p-p	Guaranteed Logic High Level		400		2600	mV
V_{CM}	Common-mode Voltage			1.65		2.25	V
I_{IH}	Input High Current	V_{DD} = Max.	$V_{IN} = V_{DD}$		±10	±20	µA
I_{IL}	Input Low Current	V_{DD} = Max.	$V_{IN} = V_{SS}$		±10	±20	µA
I_I	Input High Current	V_{DD} = Max., $V_{IN} = V_{DD}$(Max.)				±20	µA

Table 8. D.C Electrical Characteristics: 3.3V–LVTTL/LVCMOS Input

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Guaranteed Logic High Level		2			V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I_{IH}	Input High Current	V_{DD}= Max.	V_{IN} = 2.7V			1	µA
I_{IL}	Input Low Current	V_{DD}= Max.	V_{IN} = 0.5V			–1	µA
I_I	Input High Current	V_{DD} = Max., V_{IN} = V_{DD}(Max.)				20	µA
V_{IK}	Clamp Diode Voltage	V_{DD} = Min., IIN = –18 mA			–0.7	–1.2	V
V_H	Input Hysteresis				80		mV

Table 9. D.C Electrical Characteristics: 3.3V–LVDS OUTPUT

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
I V_{OD} **I**	Differential output voltage p-p	V_{DD} = 3.3V, V_{IN} = V_{IH}, or V_{IL}	RL = 100 ohm	0.25	–	0.45	V
VOC(SS)	Steady-state common-mode output voltage			–	–	226	mV
Delta VOC(SS)	Change in VOC(SS) between logic states			–50	3	50	mV
VOC(PP)	Peak to peak common mode output voltage			–	–	150	mV
I_{OS}	Output short circuit	QA = 0V or QB = 0V		–	–	–20	mA
Voh	Output voltage high		RL = 100 ohm	–	–	1475	mV
Vol	Output voltage low			925	–	–	mV

Table 10.AC Parameters

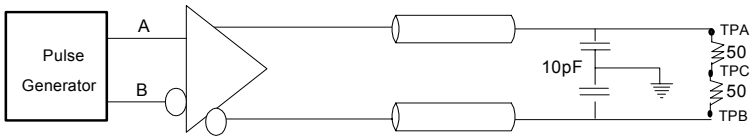
Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
Rise Time	Pin control (pin 3) logic is “FALSE” defaulting to 100 ohm output drivers. Differential 20% to 80%	CL–10 pF RL and CL to GND 3 CL = $C_{intrinsic}$ and $C_{external}$	RL = 100 ohm	–	–	1.4	ns
Fall Time				–	–	1.4	ns
Rise Time	Pin control (pin 3) logic is “True” defaulting to 50 ohm output drivers. Differential 20% to 80%	CL–10 pF RL and CL to GND 3 CL = $C_{intrinsic}$ and $C_{external}$	RL = 50 ohm Output boost	–	350	600	ps
Fall Time				–	350	600	ps

Table 11.AC Switching Characteristics @ 3.3 V (V_{DD} = 3.3V ±5%, Temperature = –40°C to +85°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
IN [+,-] to Q[A,B] Data and Clock Speed						
t_{PLH}	Propagation Delay – Low to High	V_{OD} = 100 mV	3	4	5	ns
t_{PHL}	Propagation Delay – High to Low		3	4	5	ns
T_{pd}	Propagation Delay		3	4	5	ns
IN [1,2] to Q[A,B] Control Speed						
T_{Pe}	Enable (EN) to functional operation		–	–	6	ns
T_{pd}	Functional operation to Disable		–	–	5	ns
Q[A,B] Output Skews						
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)		–	0.085	0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}–t_{PLH})		–	0.2	–	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	V_{ID} = 100 mV	–	–	1	ns

Table 12.High Frequency Parametrics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Maximum frequency V_{DD} = 3.3V	50% duty cycle tW(50–50) Standard Load Circuit.	–	–	400	MHz
Fmax(20)	Maximum frequency V_{DD} = 3.3V	20% duty cycle tW(50–50) LVPECL Input $V_{IN} = V_{IH}(Max.)/V_{IL}(Min.)$ $V_{OUT} = V_{OH}(Min.)/V_{OL}$ (Max.) (Limit)	–	–	200	MHz
TW	Minimum pulse V_{DD} = 3.3V	LVPECL Input $V_{IN} = V_{IH}(Max.)/V_{IL}(Min.)$ F= 100 MHz $V_{OUT} = V_{OH}(Min.)/V_{OL}(Max.)$(Limit)	1	–	–	ns



Standard Termination

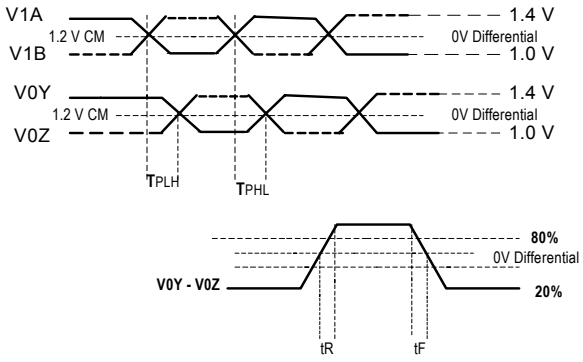
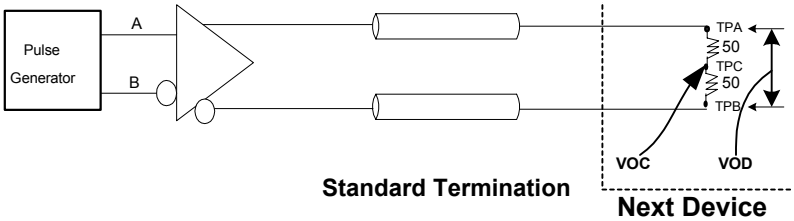


Figure 1. Differential Receiver to Driver Propagation Delay and Driver Transition Time[3, 4, 5, 6]



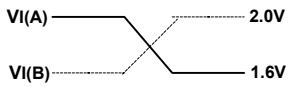
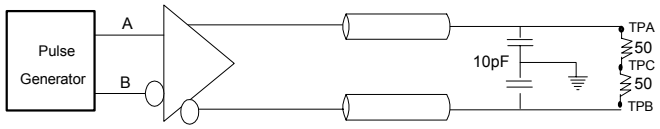


Figure 2. Test Circuit and Voltage Definitions for the Driver Common-mode Output Voltage[3, 4, 5, 6]

Notes:
3. All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse rerate = 50 Mpps; pulse width = 10 ± 0.2 ns.
4. RL= 50 ohm ± 1% Zline = 50 ohm 6".
5. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
6. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to V_{DD-2}.



Standard Termination

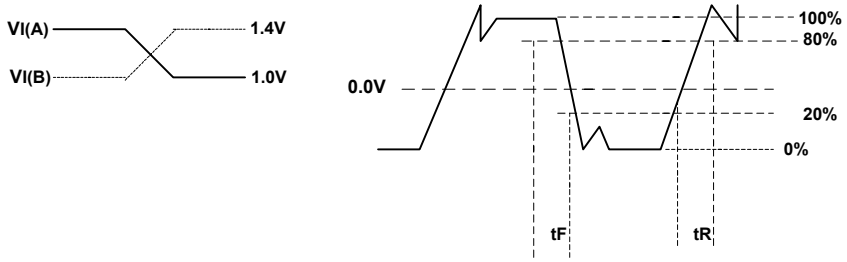


Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal[3, 4, 5, 6]

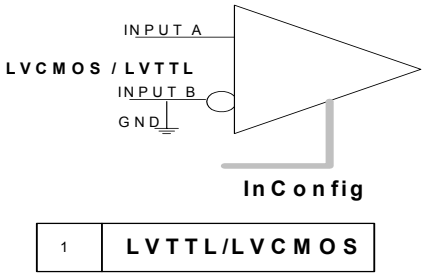


Figure 4. LVCMOS/LVTTL Single-ended Input Value[7]

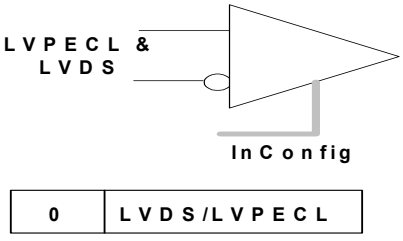


Figure 5. LVPECL or LVDS Differential Input Value[8]

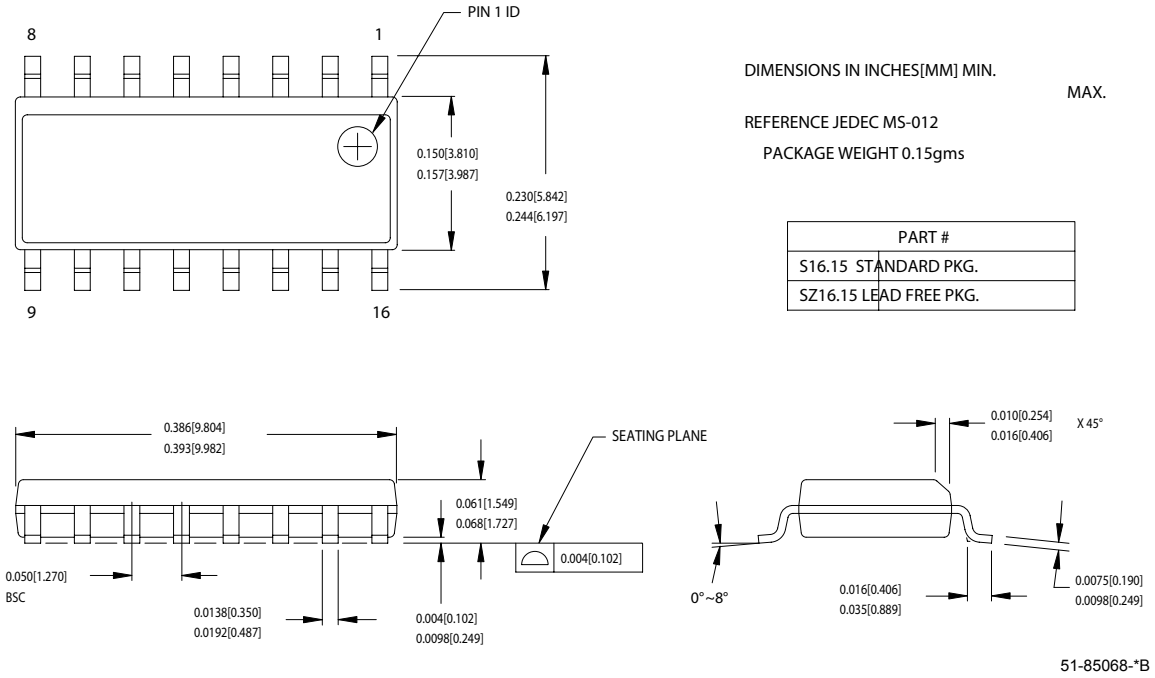
Ordering Information

Part Number	Package Type	Product Flow
CY2DL814ZI	16-pin TSSOP	Industrial, –40°C to 85°C
CY2DL814ZIT	16-pin TSSOP–Tape and Reel	Industrial, –40°C to 85°C
CY2DL814SI	16-pin SOIC	Industrial, –40°C to 85°C
CY2DL814SIT	16-pin SOIC–Tape and Reel	Industrial, –40°C to 85°C
CY2DL814ZC	16-pin TSSOP	Commercial, 0°C to 70 °C
CY2DL814ZCT	16-pin TSSOP–Tape and Reel	Commercial, 0°C to 70 °C
CY2DL814SC	16-pin SOIC	Commercial, 0°C to 70 °C
CY2DL814SCT	16-pin SOIC–Tape and Reel	Commercial, 0°C to 70 °C
Lead-free		
CY2DL814ZXI	16-pin TSSOP	Industrial, –40°C to 85°C
CY2DL814ZXIT	16-pin TSSOP–Tape and Reel	Industrial, –40°C to 85°C
CY2DL814SXI	16-pin SOIC	Industrial, –40°C to 85°C
CY2DL814SXIT	16-pin SOIC–Tape and Reel	Industrial, –40°C to 85°C
CY2DL814ZXC	16-pin TSSOP	Commercial, 0°C to 70 °C
CY2DL814ZXCT	16-pin TSSOP–Tape and Reel	Commercial, 0°C to 70 °C
CY2DL814SXC	16-pin SOIC	Commercial, 0°C to 70 °C
CY2DL814SXCT	16-pin SOIC–Tape and Reel	Commercial, 0°C to 70 °C

Notes:
7. LVCMOS/LVTTL single ended input value. Ground either input: when on the B side then non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See *Table 4*.
8. LVPECL or LVDS differential input value.

Package Drawing and Dimensions

16-Lead (150-Mil) SOIC S16.15



DIMENSIONS IN INCHES[MM] MIN.
MAX.

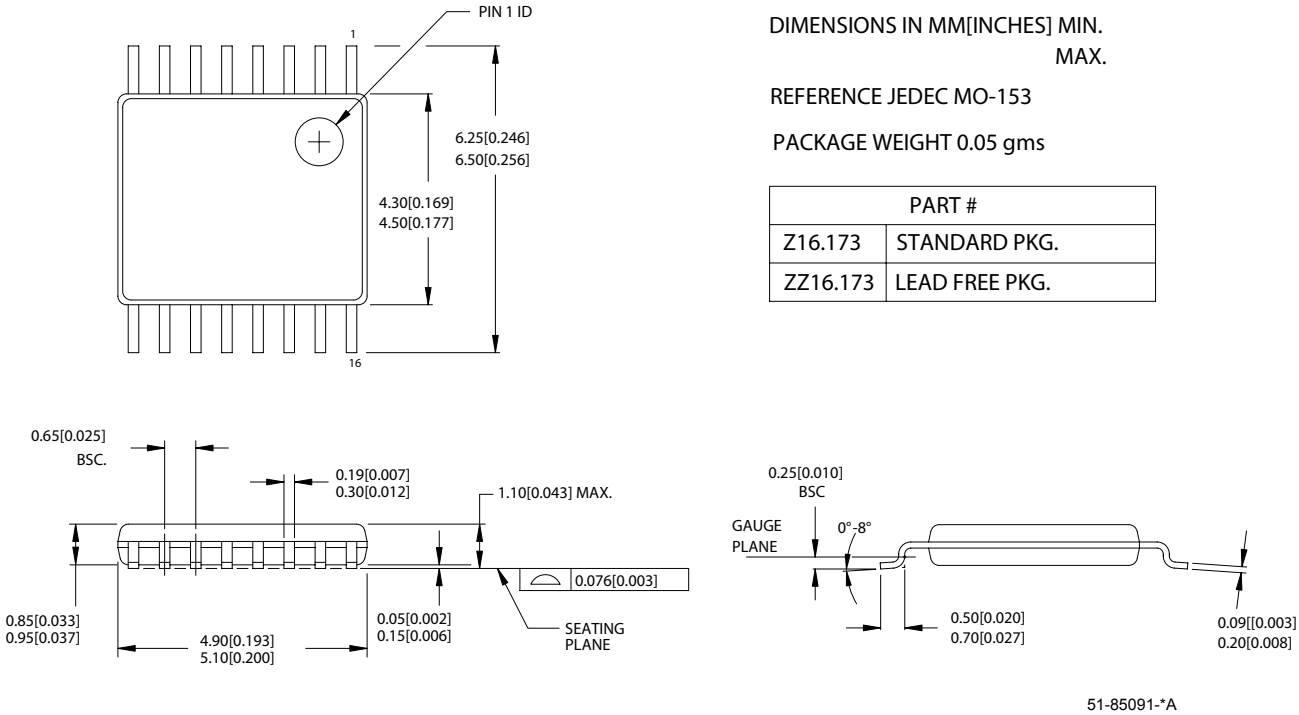
REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #
S16.15 STANDARD PKG.
SZ16.15 LEAD FREE PKG.

51-85068-*B

16-lead TSSOP 4.40 mm Body Z16.173



DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.

51-85091-*A

Document Title: ComLink™ Series CY2DL814 1:4 Clock Fanout Buffer Document Number: 38-07057				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115362	07/10/02	EHX	New Data Sheet
*A	122744	12/14/02	RBI	Added power up requirements to maximum ratings information.
*B	384077	See ECN	RGL	Added Lead-free devices Added typical values