



DCR3030V42

Phase Control Thyristor Preliminary Information

DS5810-1.1 June 2005 (LN24022)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR3030V42	4200	$T_{vj} = -40^{\circ}\text{C to } 125^{\circ}\text{C}$, $I_{DRM} = I_{RRM} = 200\text{mA}$, $V_{DRM}, V_{RRM} t_p = 10\text{ms}$, $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR3030V40	4000	
DCR3030V35	3500	
DCR3030V30	3000	

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR3030V42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	4200V
$I_{T(AV)}$	3030A
I_{TSM}	40600A
dV/dt^*	1500V/ μs
di/dt	400A/ μs

* Higher dV/dt selections available

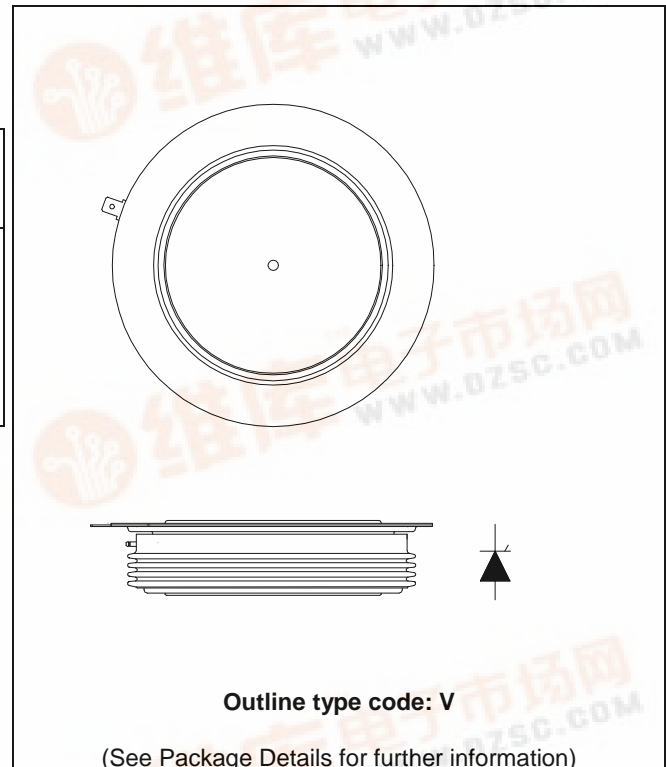


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ} C$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3030	A
$I_{T(RMS)}$	RMS value	-	4760	A
I_T	Continuous (direct) on-state current	-	4550	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ} C$	40.6	kA
I^2t	I^2t for fusing	$V_R = 0$	8.24	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	$^{\circ}C/W$
		Single side cooled	Anode DC	-	0.0130	$^{\circ}C/W$
			Cathode DC	-	0.0178	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	0.002	$^{\circ}C/W$
			Single side	-	0.004	$^{\circ}C/W$
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	$^{\circ}C$
		Reverse (blocking)		-	125	$^{\circ}C$
T_{stg}	Storage temperature range		-55	125	$^{\circ}C$	
F_m	Clamping force		48.0	59.0	kN	

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^{\circ}C$	-	200	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^{\circ}C$, gate open	-	1500	V/ μs	
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to $2x I_{T(AV)}$	Repetitive 50Hz	-	200	A/ μs
		Gate source 30V, 10 Ω , $t_r < 0.5\mu s$, $T_j = 125^{\circ}C$	Non-repetitive	-	400	A/ μs
$V_{T(TO)}$	Threshold voltage – Low level	200A to 1700A at $T_{case} = 125^{\circ}C$	-	0.82	V	
	Threshold voltage – High level	1700A to 7000A at $T_{case} = 125^{\circ}C$	-	0.98	V	
r_T	On-state slope resistance – Low level	200A to 1700A at $T_{case} = 125^{\circ}C$	-	0.292	m Ω	
	On-state slope resistance – High level	1700A to 7000A at $T_{case} = 125^{\circ}C$	-	0.198	m Ω	
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu s$, $T_j = 25^{\circ}C$	TBD	TBD	μs	
t_q	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, $dl/dt = 1A/\mu s$, $dV_{DR}/dt = 20V/\mu s$ linear	250	500	μs	
Q_s	Stored charge	$T_j = 125^{\circ}C$, $dl/dt = 1A/\mu s$, $V_{Rpk} = 3000V$, $V_{RM} = 1700V$	1600	3500	μC	
I_L	Latching current	$T_j = 25^{\circ}C$, $V_D = 5V$	TBD	TBD	mA	
I_H	Holding current	$T_j = 25^{\circ}C$, $R_{G-K} = \infty$, $I_{TM} = 500A$, $I_T = 5A$	TBD	TBD	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25° C	1.5	V
V _{GD}	Gate non-trigger voltage	At V _{DRM} , T _{case} = 125° C	TBD	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25° C	250	mA
I _{GD}	Gate non-trigger current	V _{DRM} = 5V, T _{case} = 25° C	TBD	mA

CURVES

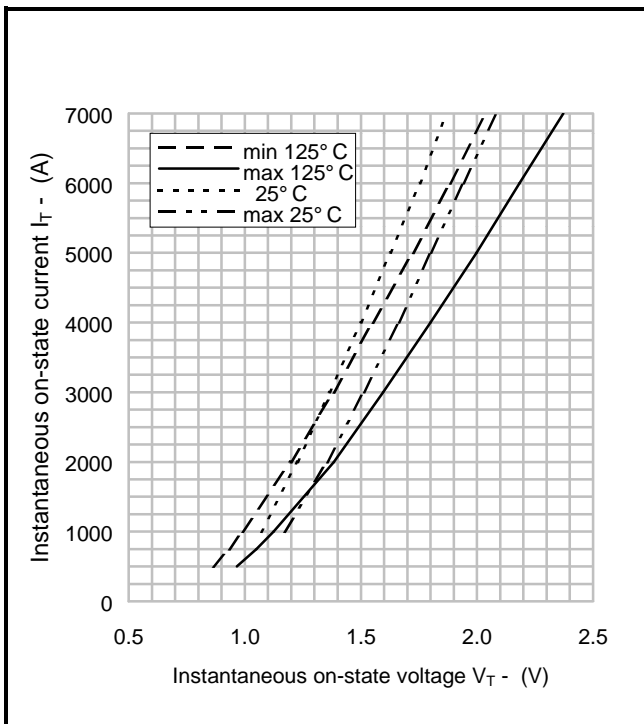


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where A = 0.866995
 B = -0.042053
 C = 0.000100
 D = 0.014062

these values are valid for T_j = 125° C for I_T 500A to 10000A

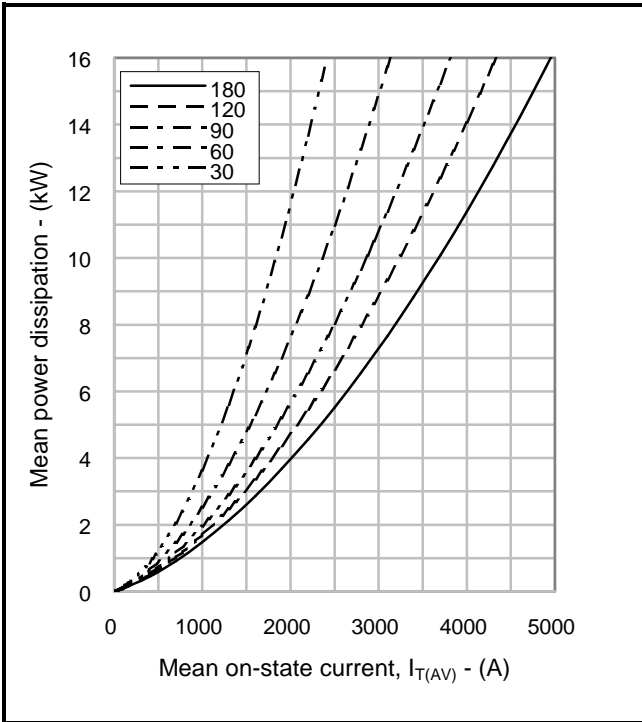


Fig.3 On-state power dissipation – sine wave

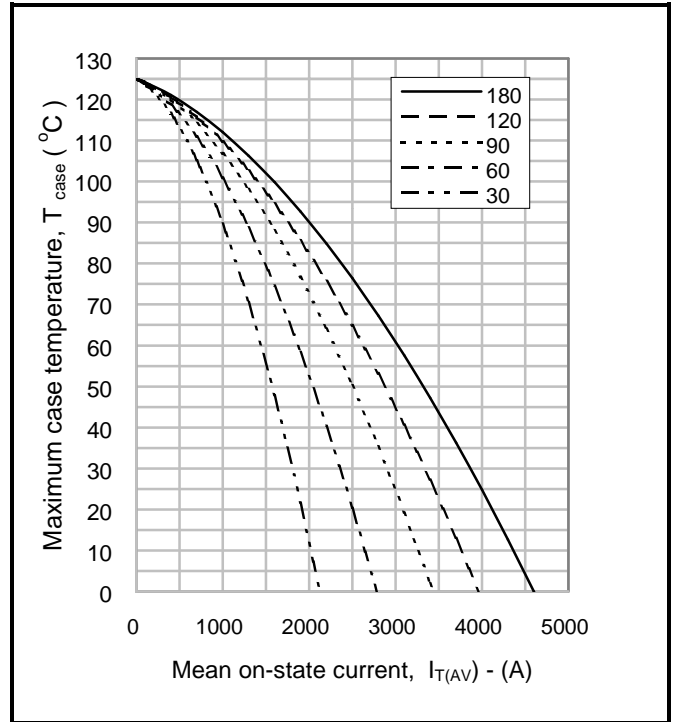


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

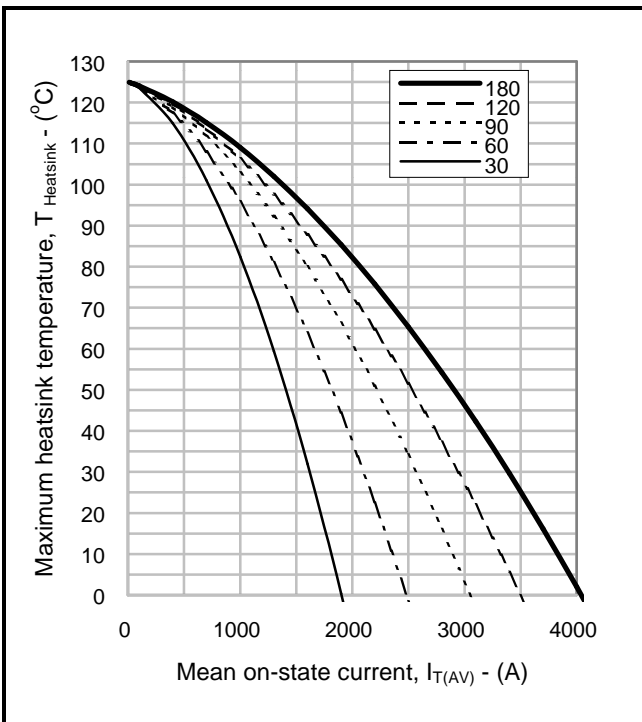


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

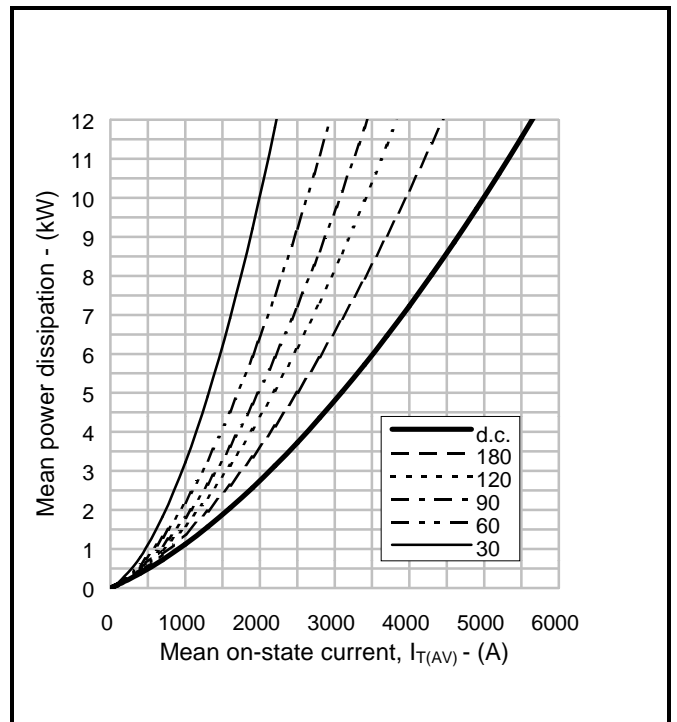


Fig.6 On-state power dissipation – rectangular wave

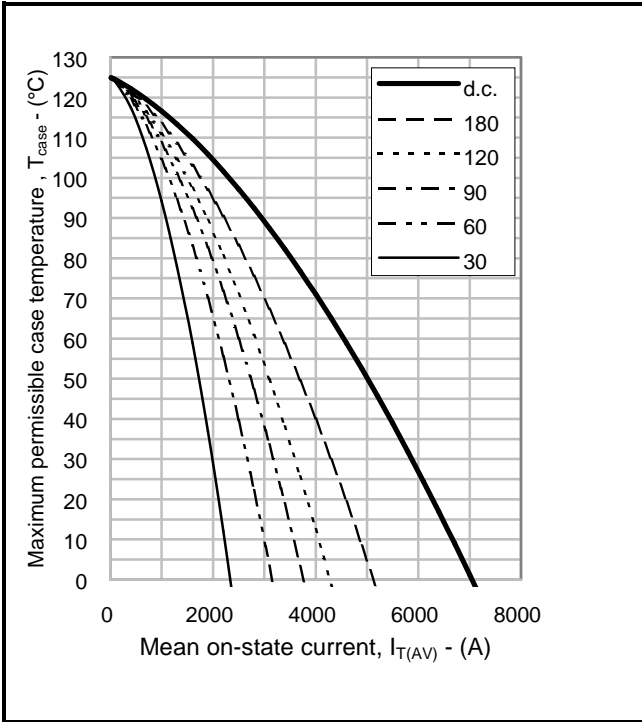


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

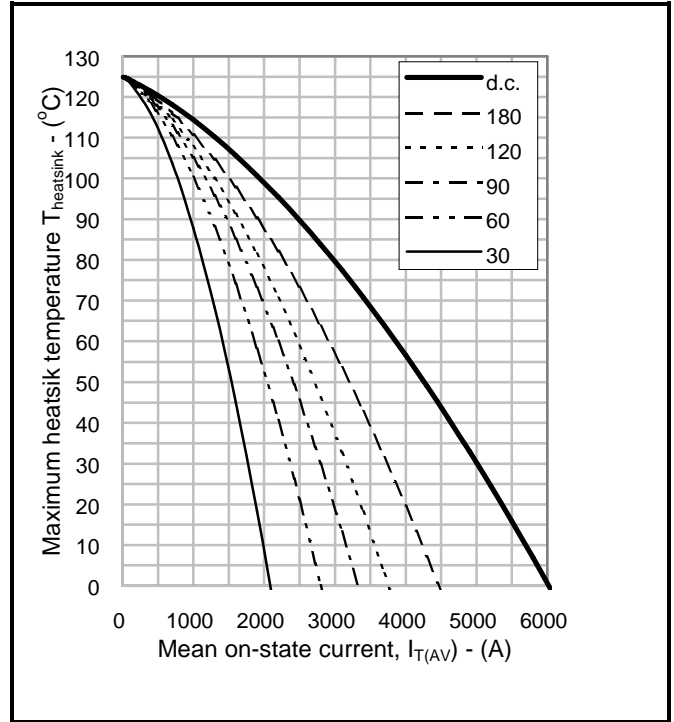


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

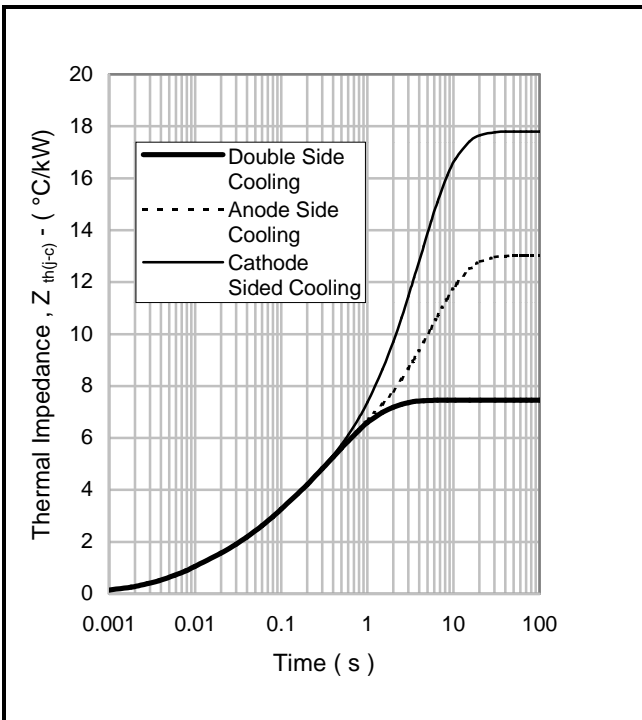


Fig.9 Maximum (limit) transient thermal impedance – junction to case (° C/kW)

		1	2	3	4
Double side cooled	R _i (° C/kW)	0.9206	1.8299	3.4022	1.3044
	T _i (s)	0.0076807	0.0579454	0.4078613	1.2085
Anode side cooled	R _i (° C/kW)	0.9032	1.6719	3.0101	7.4269
	T _i (s)	0.0075871	0.0536531	0.3144537	5.624
Cathode side cooled	R _i (° C/kW)	0.9478	2.0661	1.6884	13.0847
	T _i (s)	0.0078442	0.0645541	0.3894389	4.1447

$$Z_{th} = \sum [R_i \times (1 - \exp. (t/t_i))] \quad [1]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
θ°	$\Delta Z_{th} (z)$		θ°	$\Delta Z_{th} (z)$		θ°	$\Delta Z_{th} (z)$	
	sine.	rect.		sine.	rect.		sine.	rect.
180	1.34	0.88	180	1.34	0.88	180	1.33	0.88
120	1.57	1.30	120	1.57	1.30	120	1.57	1.29
90	1.83	1.54	90	1.84	1.54	90	1.83	1.53
60	2.08	1.81	60	2.08	1.81	60	2.07	1.80
30	2.27	2.11	30	2.28	2.11	30	2.26	2.10
15	2.36	2.28	15	2.37	2.28	15	2.35	2.26

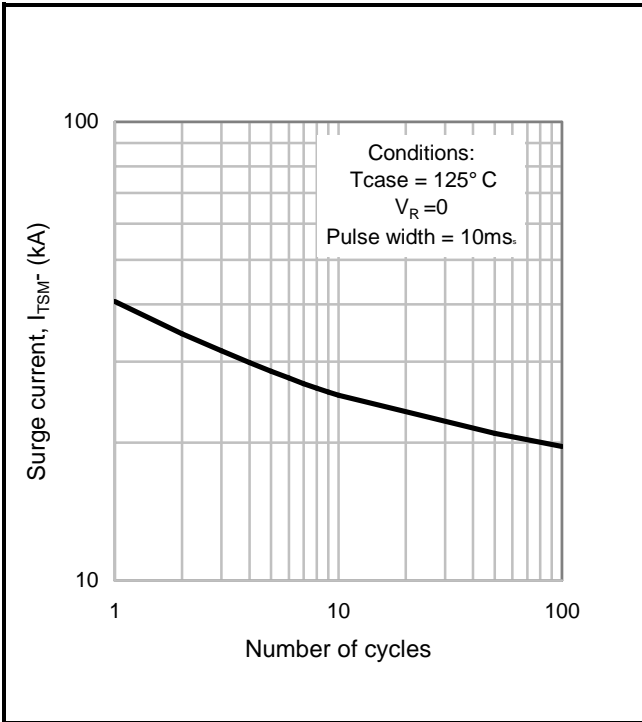


Fig.10 Multi-cycle surge current

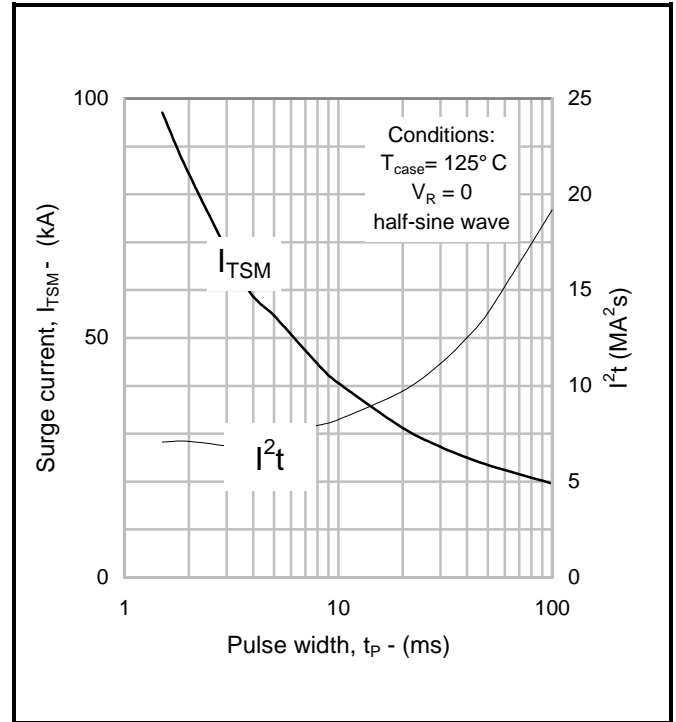


Fig.11 Single-cycle surge current

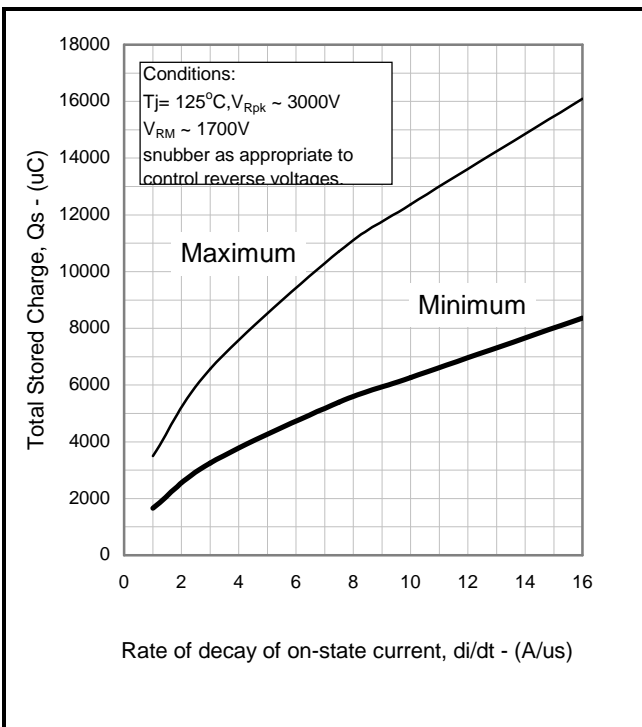


Fig. 12 Stored Charge

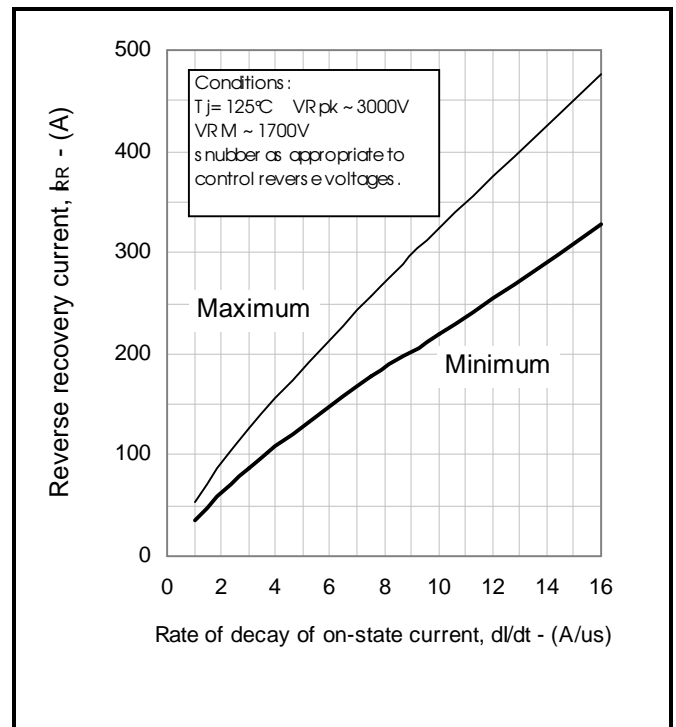


Fig. 13 Reverse Recovery Current

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. **DO NOT SCALE.**

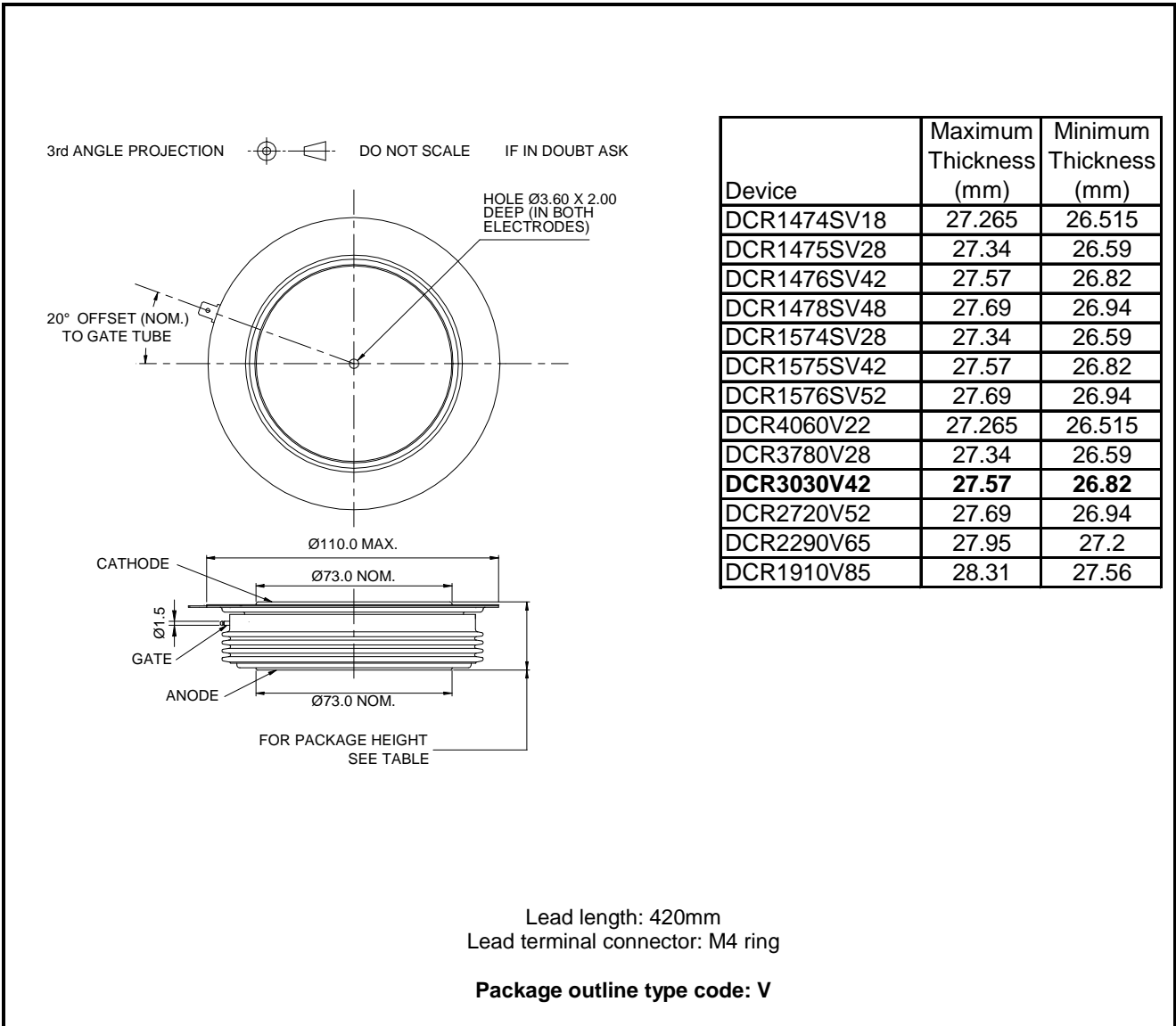


Fig.15 Package outline

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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