LINEAR TECHNOLOGY

LT1102

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

FEATURES

- Slew Rate: 30V/μs
- Gain-Bandwidth Product: 35MHz
- Settling Time (0.01%): 3μs
- Overdrive Recovery: 0.4μs
- Gain Error: 0.05% Max
- Gain Drift: 5ppm/°C
- Gain Nonlinearity: 16ppm Max
- Offset Voltage (Input + Output): 600μV Max
  – Drift with Temperature: 2μV/°C
- Input Bias Current: 40pA Max
- Input Offset Current: 40pA Max
  – Drift with Temperature (to 70°C): 0.5pA/°C

APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with < 1Hz Lowpass Filtering

DESCRIPTION

The LT®1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 180μV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 40pA.

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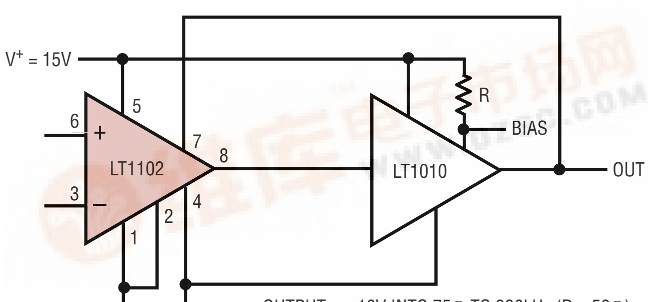
TYPICAL APPLICATION

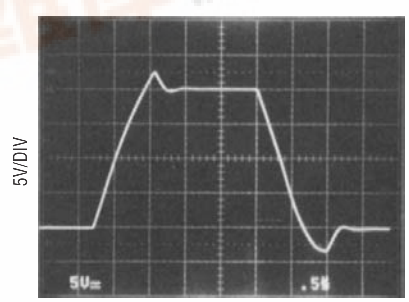
Wideband Instrumentation Amplifier with ±150mA Output Current



OUTPUT = ±10V INTO 75Ω TO 330kHz (R = 50Ω)
±10V INTO 200Ω TO 330kHz (R = 200Ω)
DRIVES 2.2nF CAP LOAD
GAIN = 10, DEGRADED 0.01% DUE TO LT1010

LT1102 • TA01

Slew Rate



G = 10 0.5μs/DIV

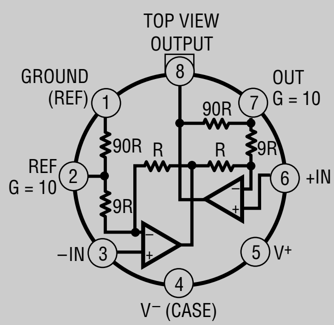
LT1102 • TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±20V
Differential Input Voltage .... ±40V
Input Voltage .... ±20V
Output Short-Circuit Duration .... Indefinite

Operating Temperature Range
  LT1102I .... −40°C to 85°C
  LT1102AC/LT1102C .... 0°C to 70°C
  LT1102AM/LT1102M **(OBSOLETE)**.....−55°C to 125°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

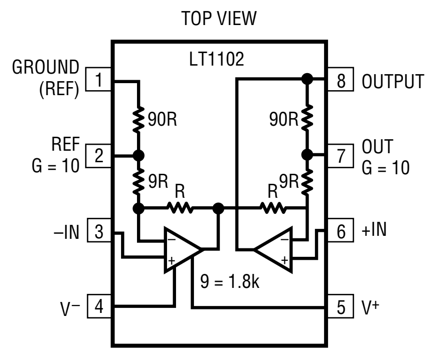
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER
LT1102AMH LT1102MH LT1102ACH LT1102CH



N8 PACKAGE
8-LEAD PDIP
$T_{JMAX} = 100°C, \theta_{JA} = 130°C/W$

ORDER PART NUMBER
LT1102IN8 LT1102ACN8 LT1102CN8

J8 PACKAGE
8-LEAD CERDIP

OBSOLETE PACKAGE
Consider the N8 Package for Alternate Source

ORDER PART NUMBER
LT1102MJ8 LT1102CJ8

LT1102 • POI01

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM/AC MIN	LT1102AM/AC TYP	LT1102AM/AC MAX	LT1102M/I/C MIN	LT1102M/I/C TYP	LT1102M/I/C MAX	UNITS
G_E	Gain Error	$V_O = \pm 10V$, R_L = 50k or 2k		0.010	0.050		0.012	0.070	%
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k		3	14		4	18	ppm
		G = 100, R_L = 2k		8	20		8	25	ppm
		G = 10, RL = 50k or 2k		7	16		7	30	ppm
V_{OS}	Input Offset Voltage			180	600		200	900	μV
I_{OS}	Input Offset Current			3	40		4	60	pA
I_B	Input Bias Current			±3	±40		±4	±60	pA
	Input Resistance Common Mode	V_{CM} = –11V to 8V		10^{12}			10^{12}		Ω
		V_{CM} = 8V to 11V		10^{11}			10^{11}		Ω
	Differential Mode			10^{12}			10^{12}		Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8		μV_{P-P}
	Input Noise Voltage Density	f_O = 10Hz		37			37		$nV/\sqrt{Hz}$
		f_O = 1000Hz (Note 2)		19	30		20		$nV/\sqrt{Hz}$
	Input Noise Voltage Density	f_O = 1000Hz, 10Hz (Note 3)		1.5	4		2	5	$fA/\sqrt{Hz}$
	Input Voltage Range		±10.5	±11.5		±10.5	±11.5		V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = \pm 10.5V$	84	98		82	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 9V$ to $\pm 18V$	88	102		86	101		dB
I_S	Supply Current			3.3	5.0		3.4	5.6	mA
V_O	Maximum Output Voltage Swing	R_L = 50k	±13.0	±13.5		±13.0	±13.5		V
		R_L = 2k	±12.0	±13.0		±12.0	±13.0		V
BW	Bandwidth	G = 100 (Note 4)	120	220		100	220		kHz
		G = 10 (Note 4)	2.0	3.5		1.7	3.5		MHz
SR	Slew Rate	G = 100, $V_{IN} = \pm 0.13V$, $V_O = \pm 5V$	12	17		10	17		V/μs
		G = 10, $V_{IN} = \pm 1V$, $V_O = \pm 5V$	21	30		18	30		V/μs
	Overdrive Recovery	50% Overdrive (Note 5)		400			400		ns
	Settling Time	V_O = 20V Step (Note 4)							
		G = 10 to 0.05%		1.8	4.0		1.8	4.0	μs
		G = 10 to 0.01%		3.0	6.5		3.0	6.5	μs
		G = 100 to 0.05%		7	13		7	13	μs
		G = 100 to 0.01%		9	18		9	18	μs

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, Gain = 10 or 100, –55°C ≤ T_A ≤ 125°C for AM/M grades, –40°C ≤ T_A ≤ 85°C for I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AM MIN	LT1102AM TYP	LT1102AM MAX	LT1102M/I MIN	LT1102M/I TYP	LT1102M/I MAX	UNITS
G_E	Gain Error	G = 100, V_O = ±10V, R_L = 50k or 2k G = 10, V_O = ±10V, R_L = 50k or 2k		0.10 0.05	0.25 0.12		0.10 0.06	0.30 0.15	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		9 5	20 10		10 6	25 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L = 50k G = 100, R_L = 2k G = 10, R_L = 50k or 2k		20 28 9	70 85 20		24 32 9	90 110 24	ppm ppm ppm
V_{OS}	Input Offset Voltage			300	1400		400	2000	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	μV/°C
I_{OS}	Input Offset Current			0.3	4		0.4	6	nA
I_B	Input Bias Current			±2	±10		±2.5	±15	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.3V	82	97		80	96		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±17V	88	100		84	99		dB
I_S	Supply Current	T_A = 125°C		2.5			2.5		mA
V_O	Maximal Output Voltage Swing	R_L = 50k R_L = 2k	±12.5 ±12.0	±13.2 ±12.6		±12.5 ±12.0	±13.2 ±12.6		V V

V_S = ±15V, V_{CM} = 0V, Gain = 10 or 100, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1102AC MIN	LT1102AC TYP	LT1102AC MAX	LT1102C MIN	LT1102C TYP	LT1102C MAX	UNITS
G_E	Gain Error	G = 100, V_O = ±10V, R_L = 50k or 2k G = 10, V_O = ±10V, R_L = 50k or 2k		0.04 0.03	0.11 0.09		0.05 0.04	0.14 0.12	% %
TCG_E	Gain Error Drift (Note 6)	G = 100, R_L = 50k or 2k G = 10, R_L = 50k or 2k		8 5	18 10		9 6	22 14	ppm/°C ppm/°C
G_{NL}	Gain Nonlinearity	G = 100, R_L= 50k G = 100, R_L= 2k G = 10, R_L= 50k or 2k		8 11 8	30 36 18		9 12 8	40 48 22	ppm ppm ppm
V_{OS}	Input Offset Voltage			230	1000		280	1400	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 6)		2	8		3	12	μV/°C
I_{OS}	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 6)		0.5	3		0.5	4	pA/°C
I_B	Input Bias Current			±40	±300		±50	±400	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 6)		1	4		1	6	pA/°C
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.3V	83	98		81	97		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±17V	87	101		85	100		dB
I_S	Supply Current	T_A = 70°C		2.8			2.9		mA
V_O	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±12.8 ±12.0	±13.4 ±12.8		±12.8 ±12.0	±13.4 ±12.8		V V

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$i_n = (2qI_B)^{1/2}$

where $q = 1.6 \bullet 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 4: This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

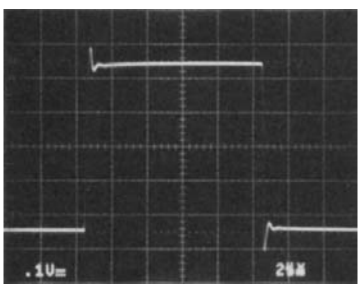
Note 5: Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation.

50% overdrive equals V_{IN} = ±2V (G = 10) or V_{IN} = ±200mV (G = 100).

Note 6: This parameter is not tested. It is guaranteed by design and by inference from other tests.

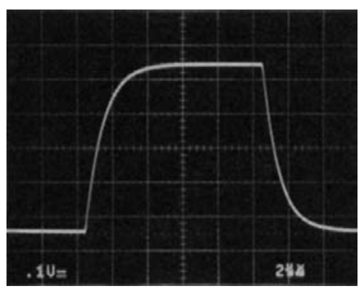
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Response, G = 10 (Input = 50mV Pulse)



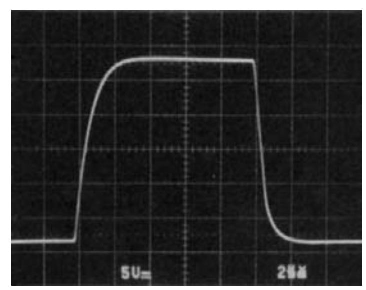
LT1102 • TPC01

Small Signal Response, G = 100 (Input = 5mV Pulse)



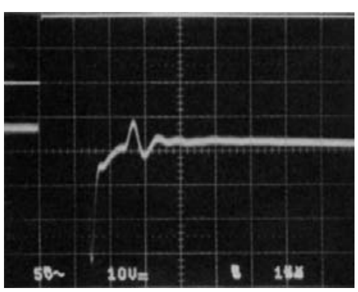
LT1102 • TPC02

Slew Rate, G = 100 (Input = ±130mV Pulse)



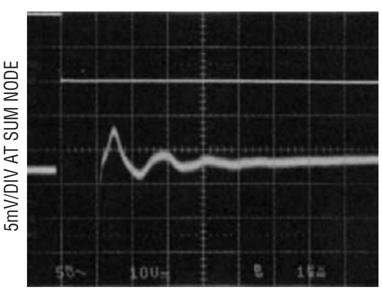
LT1102 • TPC03

Settling Time, G = 10 (Input From –10V to 10V)



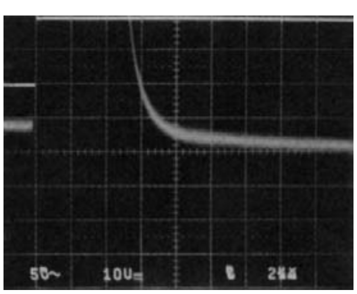
LT1102 • TPC04

Settling Time, G = 10 (Input From 10V to –10V)



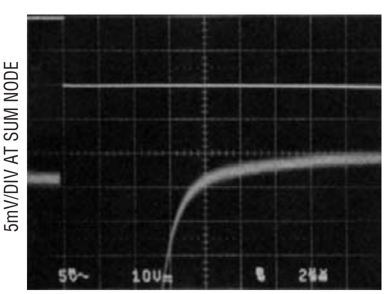
LT1102 • TPC05

Settling Time, G = 100 (Input From –10V to 10V)



LT1102 • TPC06

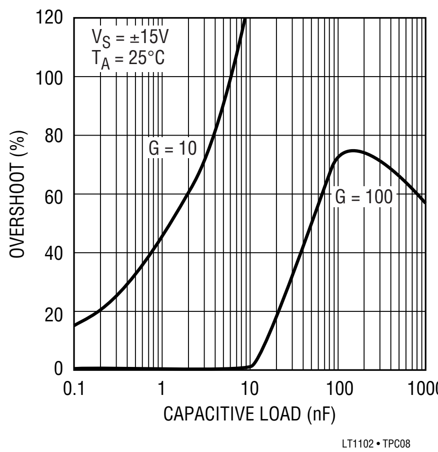
Settling Time, G = 100 (Input From 10V to –10V)



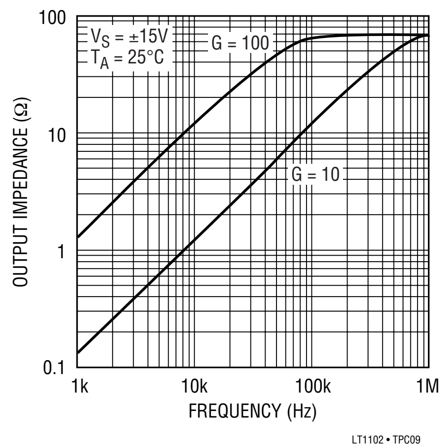
LT1102 • TPC07

TYPICAL PERFORMANCE CHARACTERISTICS

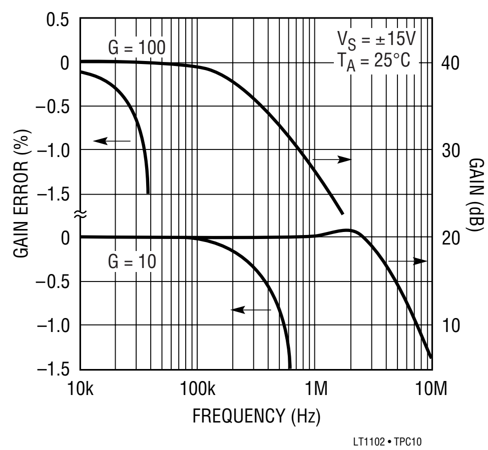
Capacitive Load Handling



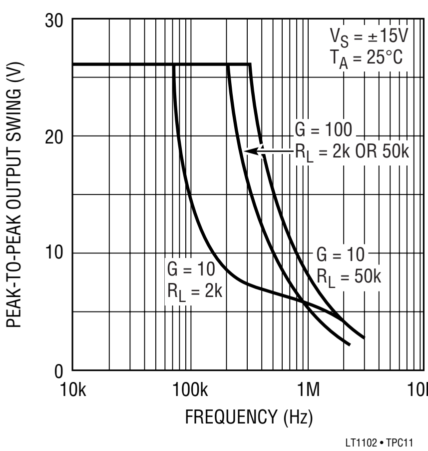
Output Impedance vs Frequency



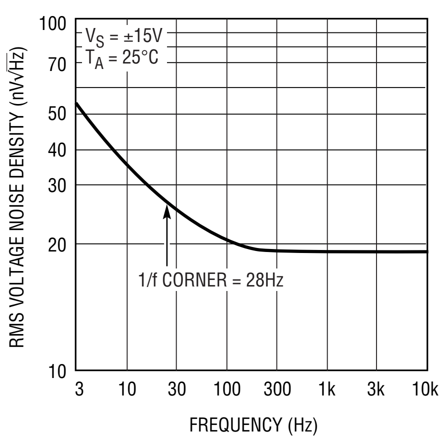
Gain vs Frequency



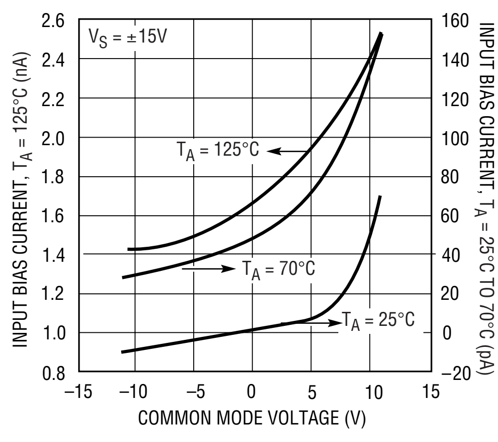
Undistorted Output vs Frequency



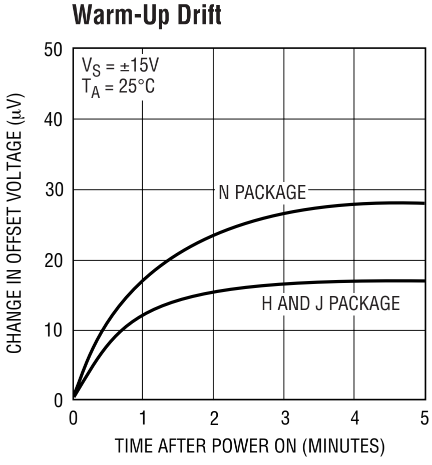
Voltage Noise vs Frequency



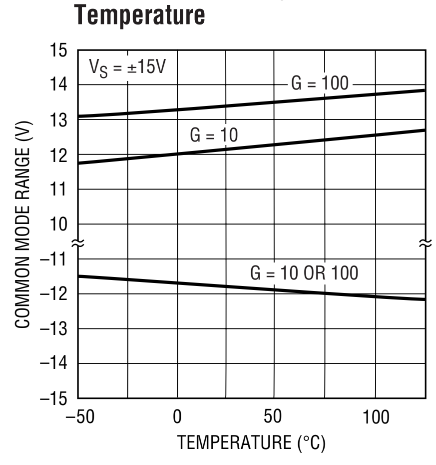
Input Bias Current Over the Common Mode Range



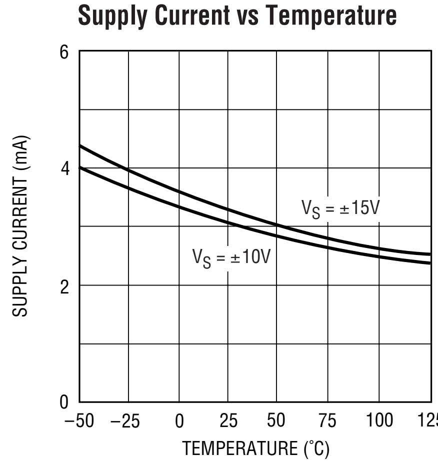
Warm-Up Drift



Common Mode Range vs Temperature

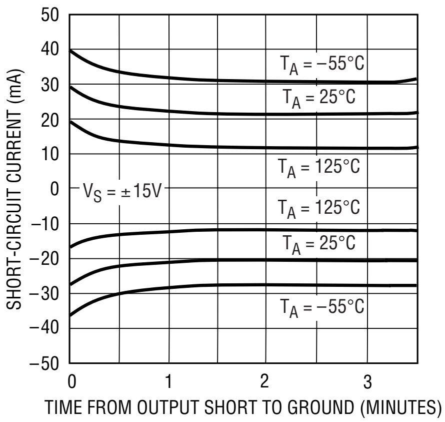


Supply Current vs Temperature



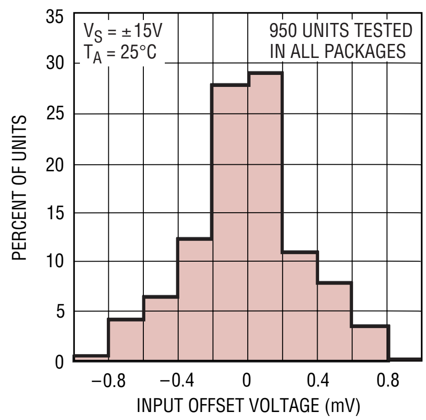
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Current vs Time



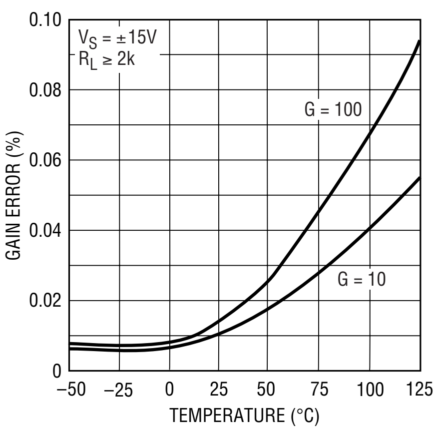
LT1102 • TPC17

Distribution of Offset Voltage



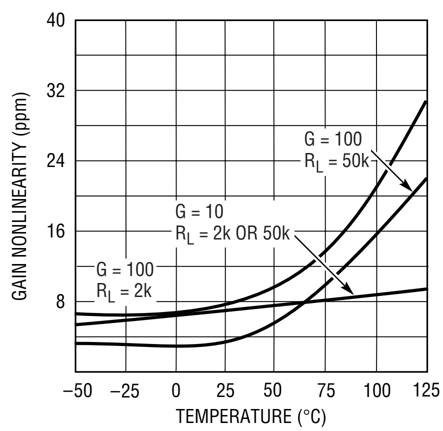
LT1102 • TPC18

Gain Error vs Temperature



LT1102 • TPC19

Gain Nonlinearity Over Temperature

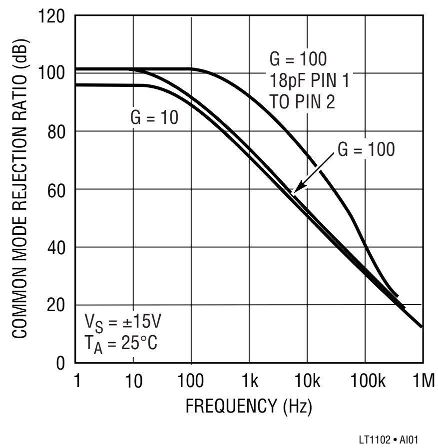


LT1102 • TPC20

APPLICATIONS INFORMATION

In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102, the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the G = 10 mode, because the bandwidths of the two op amps are similar. When G = 100, this statement is no longer true; however, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz, CMRR versus frequency is improved by an order of magnitude.

Common Mode Rejection Ratio vs Frequency



Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies). Some competitive instrumentation amplifiers have NPN inputs which are protected by back-to-back diodes. When the differential input Voltage exceeds ±13V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (= R_X) between pins 1 and 2 and pins 7 and 8.

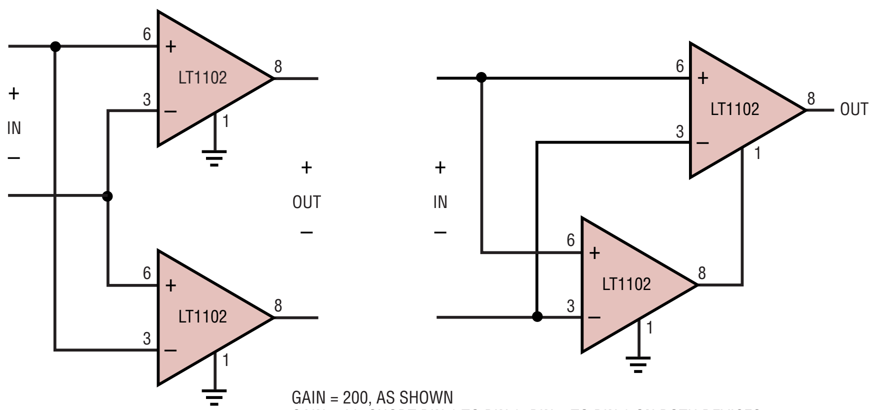
$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 1.84kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit, 90R can be measured between Pins 1 and 2.

APPLICATIONS INFORMATION

Gain = 20, 110, or 200 Instrumentation Amplifiers

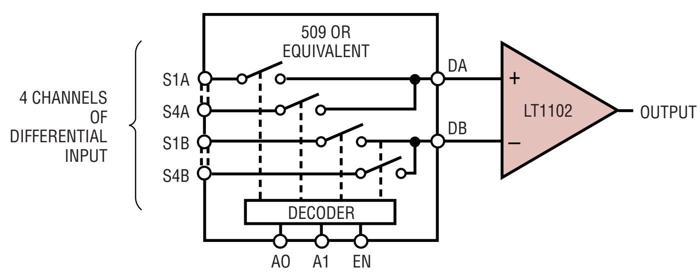
Differential Output / Single Ended Output



GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY √2 (G = 200 OR 20)

LT1102 • AI02

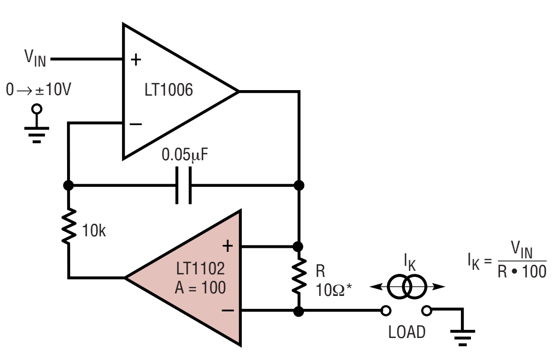
Multiplexed Input Data Acquisition



800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

LT1102 • AI03

Voltage Programmable Current Source is Simple and Precise

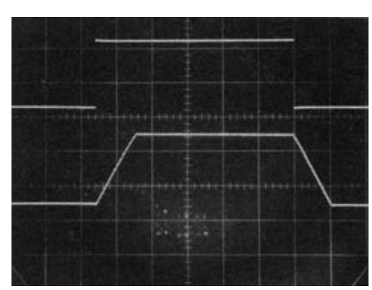


LT1102 • AI04

Dynamic Response of the Current Source

A = 5V/DIV

B = 5mA/DIV

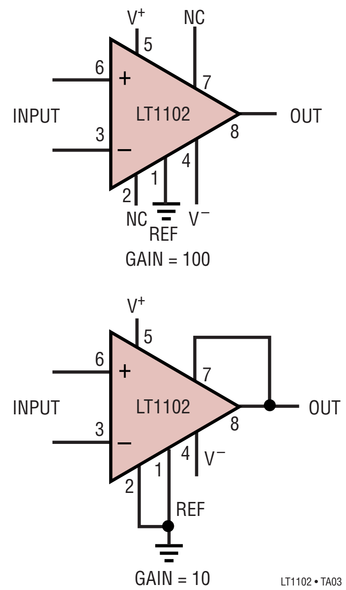


HORIZ. = 20μs/DIV

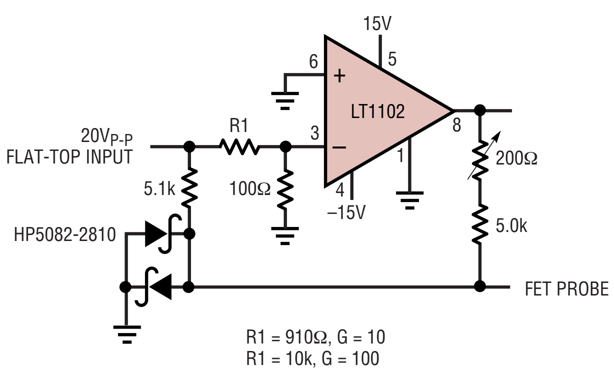
LT1102 • AI05

TYPICAL APPLICATIONS

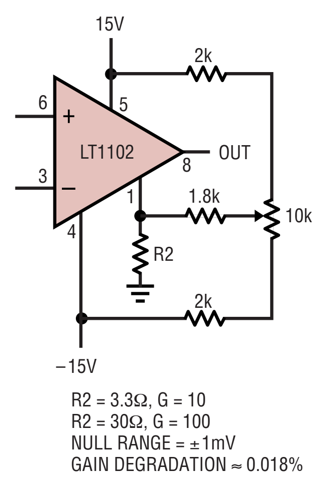
Basic Connections



Settling Time Test Circuit

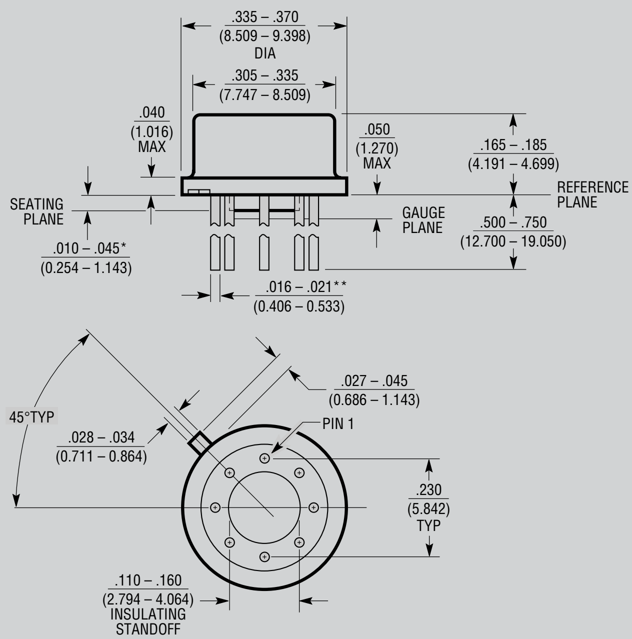


Offset Nulling



PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.230 Inch PCD)
(Reference LTC DWG # 05-08-1321)

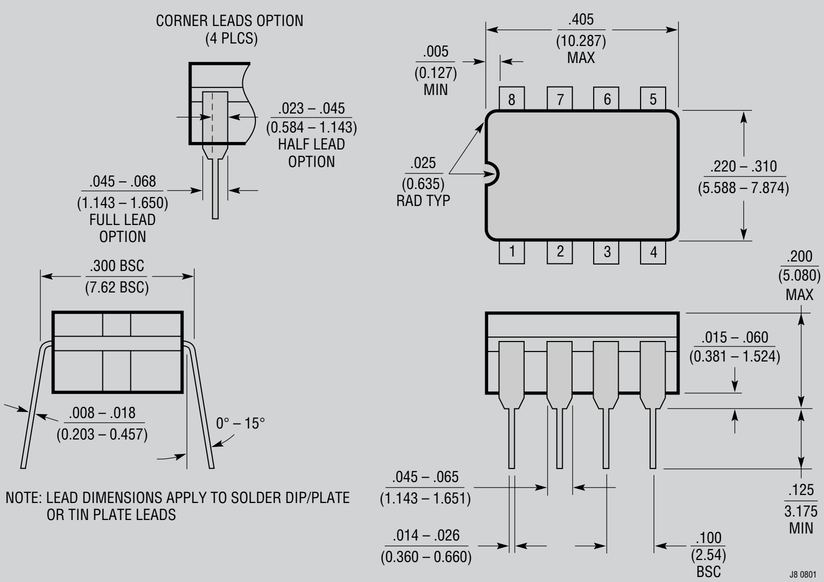


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016 – .024 (0.406 – 0.610)

H8 (TO-5) 0.230 PCD 0801

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



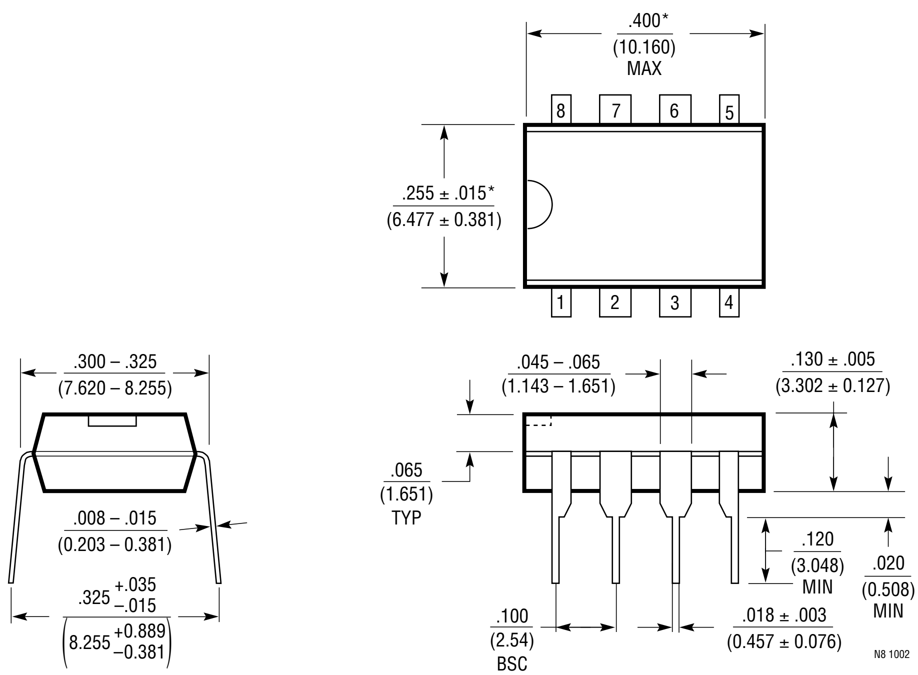
NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

J8 0801

OBSOLETE PACKAGES

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

Linear Technology Corporation
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