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19-3659; Rev 0; 4/05

MAXIM

MAX12555 Evaluation Kit

Evaluates: MAX12553/MAX12554/MAX12555

General Description

The MAX12555 evaluation kit (EV kit) is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX12555 14-bit, 95Msps analog-to-digital converter (ADC). The MAX12555 accepts differential or single-ended analog inputs, however, the EV kit allows for evaluation with either type of signal from one single-ended analog signal source. The ADC digital output can be captured easily with a user-provided high-speed logic analyzer or data-acquisition system. The EV kit operates from a 1.8V and a 3.3V power supply and includes circuitry that generates a low-jitter clock signal from an AC signal provided by the user. The EV kit comes with the MAX12555 installed. To evaluate the MAX12554 (80Msps) or MAX12553 (65Msps) on the EV kit, order free samples of these pin-compatible parts.

Features

- ♦ **95Msps Sampling Rate with the MAX12555**
- ♦ **Low-Voltage and Low-Power Operation**
- ♦ **Fully Differential or Single-Ended Signal Input Configuration**
- ♦ **Differential or Single-Ended Clock Configuration**
- ♦ **On-Board Clock-Shaping Circuit with Adjustable Duty Cycle**
- ♦ **Also Evaluates MAX12554 (80Msps) or MAX12553 (65Msps)**
- ♦ **Fully Assembled and Tested**

Selector Guide

PART	SPEED (Msps)	APPLICATION
MAX12555ETL	95	IF/Baseband sampling
MAX12554ETL	80	IF/Baseband sampling
MAX12553ETL	65	IF/Baseband sampling

Note: *To evaluate the MAX12554 or MAX12553, request a free sample with the MAX12555 EV kit*

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX12555EVKIT	0°C to +70°C	40 Thin QFN-EP*

**EP = Exposed paddle.*

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C7, C33	4	22µF ±20%, 10V tantalum capacitors (B-case) AVX TAJB226M010
C3, C4, C6, C8–C12, C17, C21, C27, C34, C43, C45	14	1.0µF ±10%, 6.3V X5R ceramic capacitors (0402) TDK C1005X5R0J105K
C5, C14, C16, C18, C19, C20, C38, C44, C49, C50	0	Not installed, capacitors (0402)
C13, C15, C22–C26, C42	8	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M
C28	1	10µF ±20%, 6.3V X5R ceramic capacitor (0805) TDK C2012X5R0J106M
C29, C40, C41, C48, C51, C52	0	Not installed, ceramic capacitors (0603)
C30, C31, C32, C35, C36, C37	6	2.2µF ±20%, 6.3V X5R ceramic capacitors (0603) TDK C1608X5R0J225M
C39	1	4.7µF ±10%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J475K
C46, C47	2	15pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRP1555C1H150J
CLOCK4	0	Not installed, SMA vertical connector (SMA)
CLOCK, AINP, AINN	3	SMA vertical PC-mount connectors
D1	1	Dual Schottky diode (SOT23) Central Semiconductor CMPD6263S
D2	0	Not installed, diode (SOT23)
J1	1	Dual row, 2 x 20, 40-pin header
JU1, JU9, JU10	0	Not installed, 2-pin headers

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at

MAX12555 Evaluation Kit

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
JU2–JU8	7	3-pin headers
L1–L4	4	EMI filters Murata NFM41PC204F1H3B
R1, R8, R11, R15–R28, R31	0	Not installed, resistors (0603)
R2, R12, R13, R14	0	Not installed, resistors (0402)
R3, R4	2	75Ω ±0.5% resistors (0603)
R5, R6	2	1.0kΩ ±5% resistors (0402)
R7, R9	2	100Ω ±1% resistors (0603)
R10	1	10kΩ potentiometer, 12-turn, 1/4in
R29, R30	2	110Ω ±0.5% resistors (0603)
RA1–RA4	4	220Ω ±5% resistor arrays Panasonic EXB-2HV-221J
T1, T2	2	1:1 RF transformers Mini-Circuits ADT1-1WT
T3	1	4:1 RF transformer Mini-Circuits ADT4-6WT
T4	0	Not installed, transformer
TP1–TP4	4	Test points (red)
TP5, TP6	2	Test points (black)
U1	**1**	**MAX12555ETL (40 Thin QFN-EP, 6mm x 6mm)**
U2	1	Low-voltage, 16-bit register (48-pin TSSOP) Texas Instruments SN74AVC16374DGG
U3	0	Not installed (SC70-5)
U4	1	TinyLogic UHS buffer (SC70-5) Fairchild NC7SZ125P5
U5	0	Not installed (SO-8)
U6	1	TinyLogic dual UHS inverter (SC70-6) Fairchild NC7WZ04P6
None	7	Shunts (JU2–JU8)
None	1	MAX12555 PC Board

Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
AVX	843-946-0238	843-626-3123	www.avxcorp.com
Central Semiconductor	631-435-1110	631-435-1824	www.centralsemi.com
Fairchild	888-522-5372	—	www.fairchildsemi.com
Mini-Circuits	718-934-4500	718-332-4661	www.minicircuits.com
Murata	770-436-1300	770-436-3030	www.murata.com
Panasonic	714-373-7366	714-737-7323	www.panasonic.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Texas Instruments	972-644-5580	214-480-7800	www.ti.com

Note: *Indicate that you are using the MAX12555 when contacting these component suppliers.*

Quick Start

Recommended Equipment

- DC power supplies:
  - Digital (VLDUT) 1.8V, 100mA
  - Logic (VL) 1.8V, 100mA
  - Analog (VDUT) 3.3V, 250mA
- Signal generator with low phase noise and low jitter for clock input (e.g., HP 8644B)
- Signal generator for analog signal input (e.g., HP 8644B)
- Logic analyzer or data-acquisition system (e.g., HP 16500C)
- Analog bandpass filters (e.g., K&L Microwave) for input and clock signal
- Digital voltmeter

Procedure

The MAX12555 EV kit is a fully assembled and tested surface-mount board. Follow the steps below for board operation. **Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed across pins 2 and 3 of jumpers JU2 (MAX12555 enabled) and JU3 (two's-complement digital output format).
2) Verify that shunts are installed across pins 1 and 2 of jumper JU4 (internal duty-cycle equalizer enabled) and JU5 (differential clock configuration).
3) Verify that shunts are installed across pins 2 and 3 of jumper JU6 and across pins 1 and 2 of jumpers JU7 and JU8.
4) Connect the clock generator output to the clock bandpass filter input.
5) Connect the output of the clock bandpass filter to the CLOCK SMA connector.
6) Connect the output of the analog signal generator to the input of the signal bandpass filter. Keep the cable connection between the signal generators, filters, and EV kit board as short as possible for optimum dynamic performance.
7) Connect the output of the signal bandpass filter to the AINP SMA connector. **Note:** It is recommended that a 3dB or 6dB attenuation pad be used to reduce reflections and distortion from the bandpass filter.
8) Connect the logic analyzer to the square pin header (J1). See the *Output Signal* section for bit locations and J1 header designations. The system clock is available on pin J1-3.
9) Connect a 3.3V, 250mA power supply to VDUT. Connect the ground terminal of this supply to the corresponding GND pad.
10) Connect a 1.8V, 100mA power supply to VL. Connect the ground terminal of this supply to the GND pad.
11) Connect a 1.8V, 100mA power supply to VLDUT. Connect the ground terminal of this supply to the GND pad.
12) Turn on the 3.3V power supply.
13) Turn on the 1.8V power supplies.
14) Enable the signal generators.
15) Set the clock signal generator for an output amplitude of $2V_{P-P}$ or higher (recommended +16dBm to +19dBm for optimum AC performance for input frequencies greater than 100MHz) and the frequency (f_{CLK}) to ≤ 95MHz.
16) Set the analog input signal generators for an output amplitude of less than or equal to $2V_{P-P}$ and to the desired test frequency.
17) Verify that the two signal generators are synchronized to each other. Adjust the output power level of the signal generators to overcome cable, bandpass filter, and attenuation pad losses at the input.
18) Enable the logic analyzer.
19) Collect data using the logic analyzer.

Detailed Description

The MAX12555 EV kit is a fully assembled and tested circuit board that contains all the components necessary to evaluate the performance of the MAX12555. Data generated by the MAX12555 is captured on a single 14-bit parallel bus. The EV kit comes with the MAX12555 installed and can be operated with a maximum clock frequency (f_{CLK}) of 95MHz. The MAX12555 accepts differential or single-ended analog inputs and differential or single-ended clock signals. With the proper board configuration, the ADC can be evaluated with both types of signals by supplying only one single-ended analog signal to the EV kit.

The EV kit is designed as a four-layer PC board to optimize the converter's performance. For simple operation, the EV kit requires 3.3V and 1.8V power supplies applied to analog and digital power planes, respectively. However, the digital plane can be operated down to 1.7V without compromising the ADC's performance. The logic analyzer's threshold must be adjusted accordingly.

Access to the digital outputs is provided through connector J1. The 40-pin connector easily interfaces with a user-provided logic analyzer or data-acquisition system. The DAV buffered output clock signal is available at pin J1-3 (CLKO), which can be used to synchronize the output data to the logic analyzer.

Power Supplies

The MAX12555 EV kit requires separate analog and digital power supplies for best performance. Separate 3.3V power supplies are used to power the analog circuit blocks of the MAX12555 (VDUT) and the clock-shaping circuit (VCLK). To evaluate single-ended clock signal operation, 3.3V must be supplied to VCLK. Separate 1.8V power supplies are used to power the digital circuit block of the MAX12555 (VLDUT) and the buffer/driver U2 (VL). The digital circuit blocks of the EV kit can operate with voltage supplies as low as 1.7V and as high as 3.6V.

Clock Input

The MAX12555 accepts a differential or single-ended clock input. However, the MAX12555 EV kit can only accept a single-ended clock signal. The MAX12555 EV kit includes circuitry that converts a single-ended signal to a differential clock signal through a transformer or a user-installed differential clock driver IC (U5). The EV kit also includes clock-shaping circuitry for a single-ended clock signal configuration. Jumper JU5 must be configured for differential or single-ended clock signal operation. See Table 1 for jumper settings.

Transformer-Coupled Differential Clock

A single-ended signal connected to the CLOCK SMA connector is converted to a differential signal by transformer T3. In this mode, diode D1 limits the clock signal amplitude. Using this diode in the signal path allows the clock signal to be increased significantly without violating the absolute maximum ratings of the converter inputs, as the diode clips the signal. Overdriving the clock input to the board (CLOCK SMA) results in an increased slew rate, which, in turn, compensates for the negative effects that clock jitter imposes on such parameters as signal-to-noise ratio (SNR) and signal-to-noise plus distortion (SINAD). See Table 2 for clock-drive jumper settings.

Install a shunt across pins 1 and 2 of jumper JU5 for differential clock operation. **Note:** While in transformer-coupled differential clock mode, power to VCLK should not be applied unless R10 is turned to one extreme to avoid unnecessary triggering of U6. Unnecessary triggering could potentially disturb the ground plane with unwanted spur energy.

Clock-Shaping Circuit with Variable Duty Cycle

An on-board variable duty-cycle clock-shaping circuit generates a single-ended clock signal from an AC-coupled sine-wave applied to the CLOCK SMA connector. Measure the clock signal at pin 2 of jumper JU7 and adjust potentiometer R10 to obtain the desired duty cycle. See Table 2 for shunt positions. A 3.3V voltage source must be connected across VCLK and GND to power the clock-circuit comparators.

Input Signal

The MAX12555 accepts differential or single-ended analog input signals. However, the EV kit requires only a single-ended analog input signal. Because the amplitude of the received signal at the ADC depends on the actual cable and bandpass filter loss, account for these losses when configuring the signal input generator. In differential mode, on-board transformers T1 and T2 take the single-ended analog input connected to the AINP SMA connector and generate a differential analog signal at the ADC's input pins. For direct single-ended or differential input signal operation, the EV kit board circuit modifications are listed in the *Direct AC-Coupled Differential Input* and *Direct AC-Coupled Single-Ended Input* sections.

Table 1. MAX12555 Clock Input Settings (JU5)

SHUNT POSITION	CLKTYP PIN	CLOCK INPUT CONFIGURATION
1-2	Connected to VLDUT	Differential
2-3	Connected to GND	Single-Ended

Table 2. CLOCK Drive Settings

JUMPER	SHUNT POSITION	CLOCK MODE
JU6	1-2	Single-Ended Clock Mode—See the *Clock-Shaping Circuit with Variable Duty Cycle* section.
JU7	2-3	
JU8	2-3	
JU6	2-3	Differential Clock Mode—A single-ended signal is converted to a differential signal, which drives the MAX12555 clock inputs.
JU7	1-2	
JU8	1-2	

Direct AC-Coupled Differential Input

To evaluate the MAX12555 with differential input signals directly connected to the ADC input pins, modify the EV kit as follows:

1) Remove transformers T1 and T2.
2) Remove the short across resistor PC board footprint R15.
3) Remove resistors R3 and R4.
4) Install 0Ω or low-value resistors across R20 and R24 PC board footprints.
5) Install 4.7µF ceramic capacitors across C51 and C52 PC board footprints.
6) Modify resistors R30 and R29 to match the source impedance, e.g., 25Ω resistors for a 50Ω differential source impedance.
7) Connect the positive input signal source to the AINP SMA connector.
8) Connect the negative input signal source to the AINN SMA connector.

Direct AC-Coupled Single-Ended Input

To evaluate the MAX12555 with a single-ended input signal directly connected to the ADC input terminal, modify the EV kit as follows:

1) Remove transformers T1 and T2.
2) Remove resistor R3.
3) Install 0Ω or low-value resistors across R20, R29, and R13 PC board footprints.
4) Install a 4.7µF ceramic capacitor across C51 PC board footprint.
5) Install a 1µF capacitor across C47 PC board footprints.
6) Modify resistor R30 to match the source impedance, e.g., a 50Ω resistor for a 50Ω source impedance.
7) Connect the input signal source to the AINP SMA connector.

MAX12555 Power-Down

Jumper JU2 controls the power-down function of the MAX12555. Other ICs on the MAX12555 EV kit will continue to draw quiescent current from the power supplies. See Table 3 for power-down jumper settings.

Table 3. Power-Down Settings (JU2)

SHUNT POSITION	PD PIN	EV KIT OPERATION
1-2	Connected to VLDUT	Powered Down
2-3	Connected to GND	Normal Operation

Reference Voltage

The MAX12555 requires an input reference voltage at its REFIN pin to set the full-scale analog signal voltage input. The ADC offers a stable on-chip reference voltage of 2.048V that can be accessed at the REFIN PC board pad. The EV kit is designed to use the on-chip reference voltage by shorting REFIN to REFOUT through resistor R12.

The user can externally adjust the reference level, and hence the full-scale range, by cutting open the PC trace shorting resistor R12 and installing the appropriate resistors at locations R2 and R12 (located on the board's component side). Calculate the resistor values using the following equation:

$$R12 = R2\left(\frac{V_{REFOUT}}{V_{REFIN}} - 1\right)$$

where:

R2 = 10kΩ ±1%

V_{REFOUT} = 2.048V

V_{REFIN} = desired REFIN voltage in the 0.7V to 2.2V range

Alternatively, resistors R12 and R2 can be left unpopulated, and the ADC's full-scale range can be set by applying a stable, low-noise, external voltage reference directly at the REFIN pad.

The internal reference voltage can be disabled by shorting the REFIN pad to ground through resistor R2. In this mode, test points TP1 (REFP), TP2 (REFN), and TP3 (COM) must be driven with stable reference voltages. Refer to the *Analog Inputs and Reference Configurations* section in the MAX12555 IC data sheet for further details. **Note:** To drive test point TP3 with an external reference voltage add a 0Ω resistor to R27.

Output Coding

The MAX12555 digital output coding can be set to either two's-complement or Gray-code format by configuring jumper JU6. See Table 4 for shunt positions.

Table 4. Output Code Settings (JU6)

SHUNT POSITION	G/$\overline{T}$ PIN	DIGITAL OUTPUT FORMAT
1-2	Connected to VLDUT	Gray Code
2-3	Connected to GND	Two's Complement

Digital Output

The MAX12555 features a 14-bit, parallel, CMOS-compatible, output bus. The outputs of the ADC are applied to an output buffer (U2) capable of driving large capacitive loads that may be present at the logic analyzer connection. The digital outputs are valid on the rising edge of the CLKO output signal. The outputs of the buffer are connected to a 40-pin header (J1) located on the right side of the EV kit, where the user can connect a logic analyzer or data-acquisition system. See Table 5 for bit locations at header J1. The signals are available on the J1 pins closest to the edge of the EV kit board.

Evaluating the MAX12553, MAX12554

The MAX12555 EV kit can also be used to evaluate the pin-compatible MAX12553 (65Msps) or MAX12554 (80Msps). Remove the MAX12555 (U1) from the EV kit and install a free sample of the desired ADC. Refer to the respective data sheet for electrical and performance details.

Table 5. Output Bit Locations (J1)

CLOCK	DOR	BIT D13	BIT D12	BIT D11	BIT D10	BIT D9	BIT D8	BIT D7	BIT D6	BIT D5	BIT D4	BIT D3	BIT D2	BIT D1	BIT D0
J1-3 CLKO ↑	J1-7	J1-11	J1-13	J1-15	J1-17	J1-19	J1-21	J1-23	J1-25	J1-27	J1-29	J1-31	J1-33	J1-35	J1-37

Component Placement and Board Layout Recommendations

A detailed discussion about component placement and PC board layout recommendations for the MAX12555 can be viewed in the *Schematic and Layout Guidelines for High-Speed Data Converters* application note located in the Maxim website www.maxim-ic.com/appnotes.cfm/appnote_number/3491.

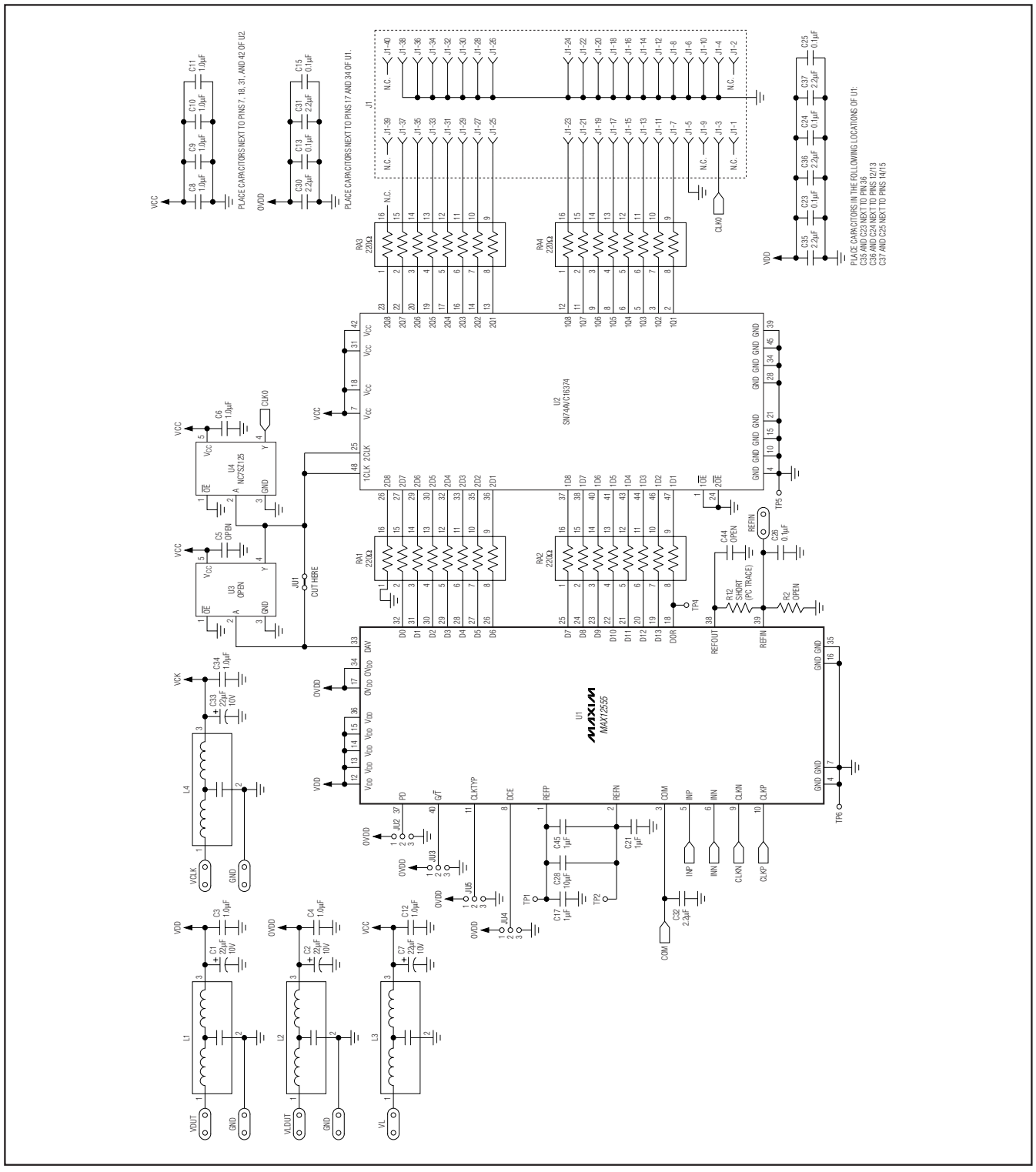


Figure 1. MAX12555 EV Kit Schematic (Sheet 1 of 2)

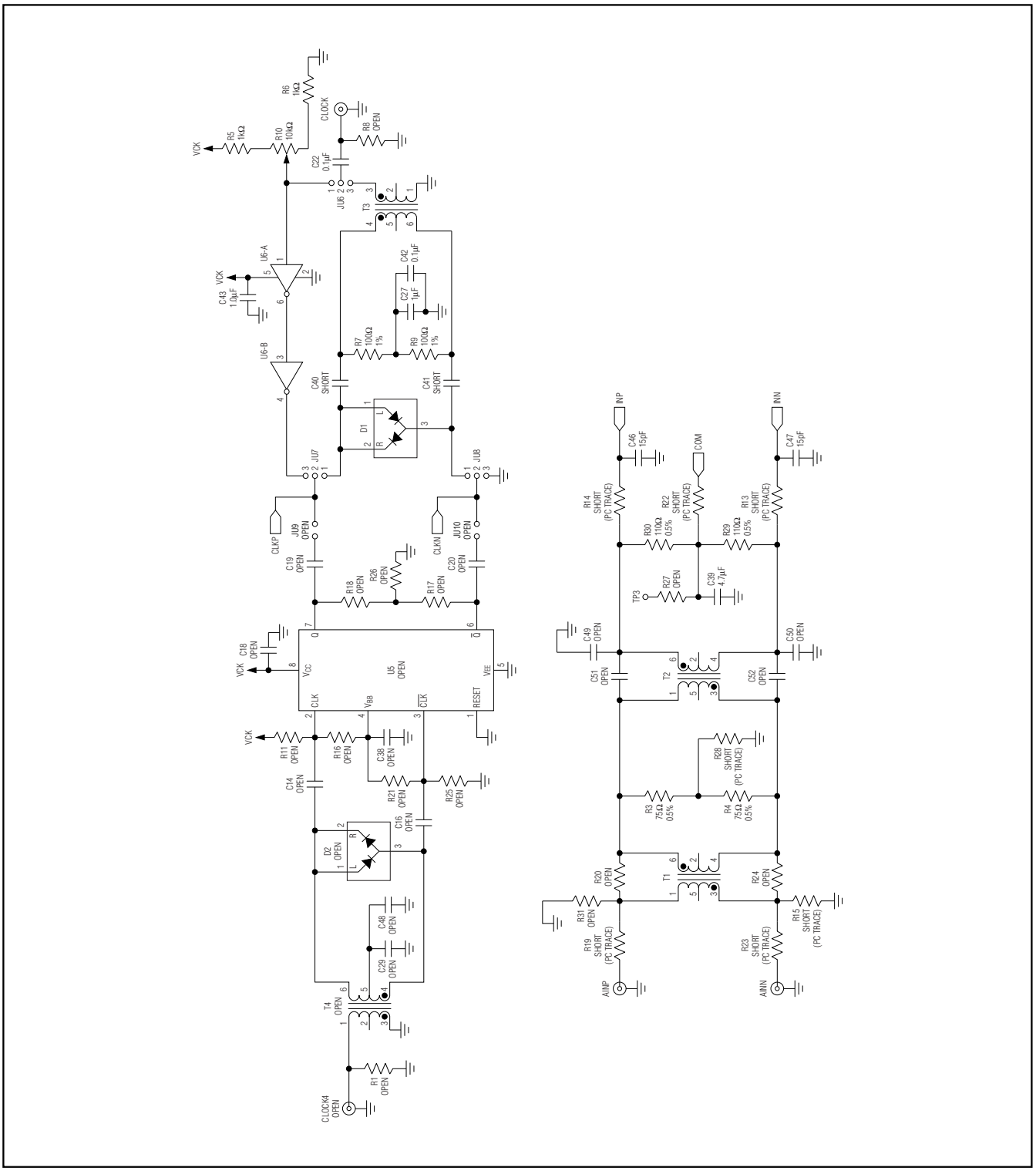


Figure 1. MAX12555 EV Kit Schematic (Sheet 2 of 2)

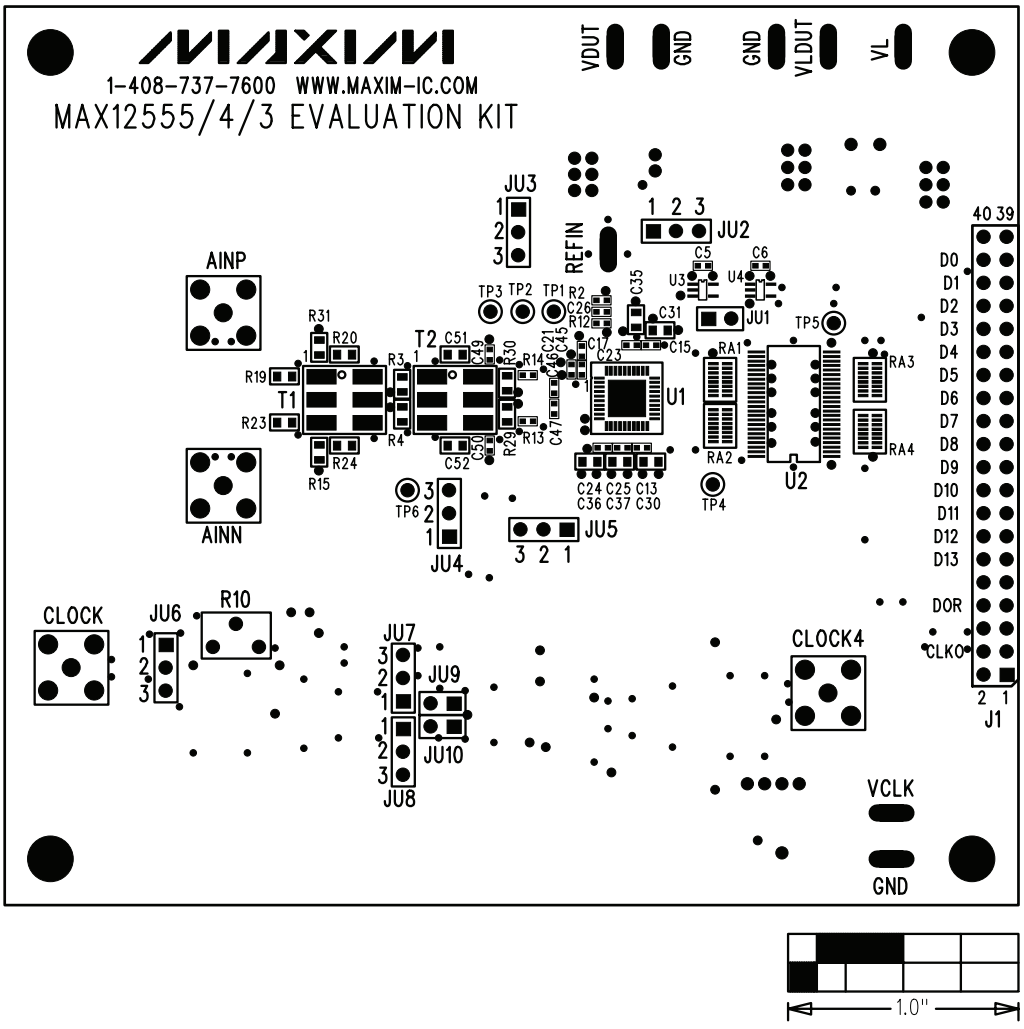


Figure 2. MAX12555 EV Kit Component Placement Guide—Component Side

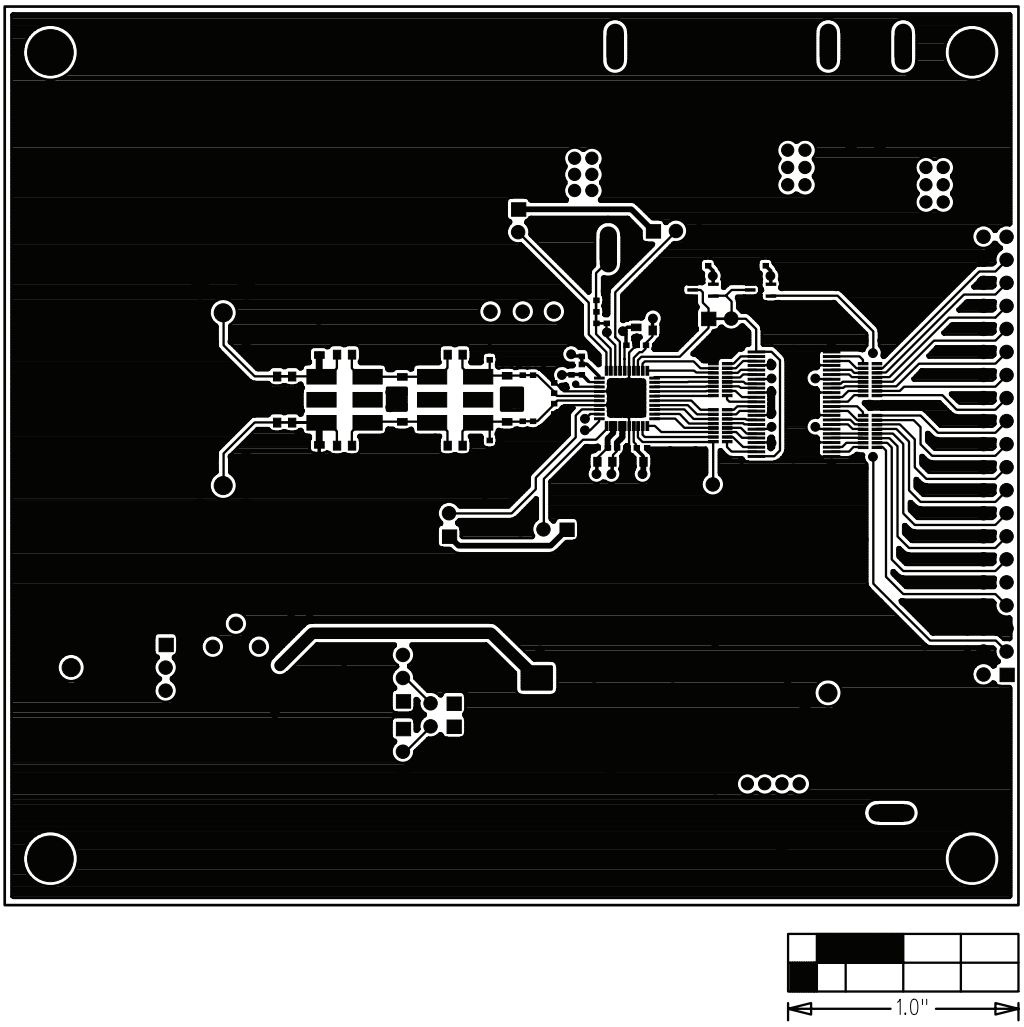


Figure 3. MAX12555 EV Kit PC Board Layout—Component Side

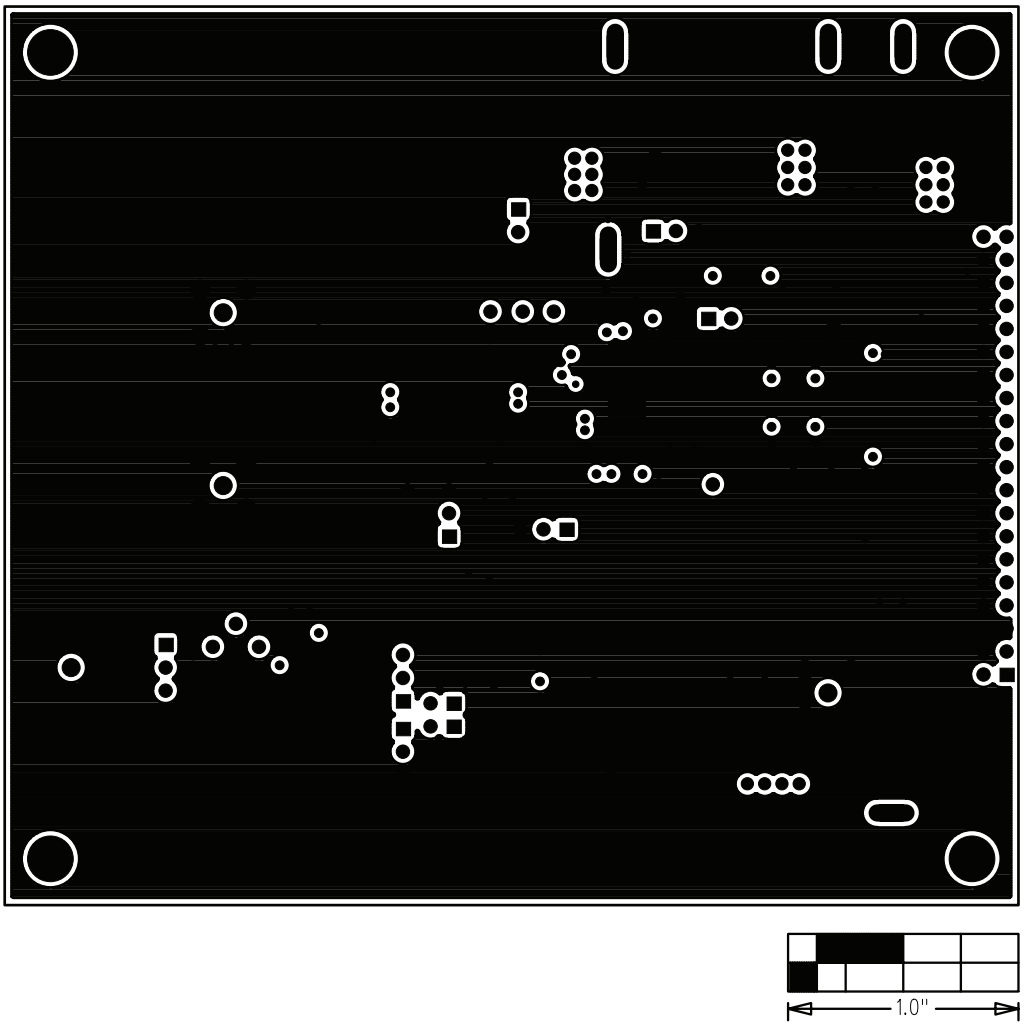


Figure 4. MAX12555 EV Kit PC Board Layout—Ground Planes

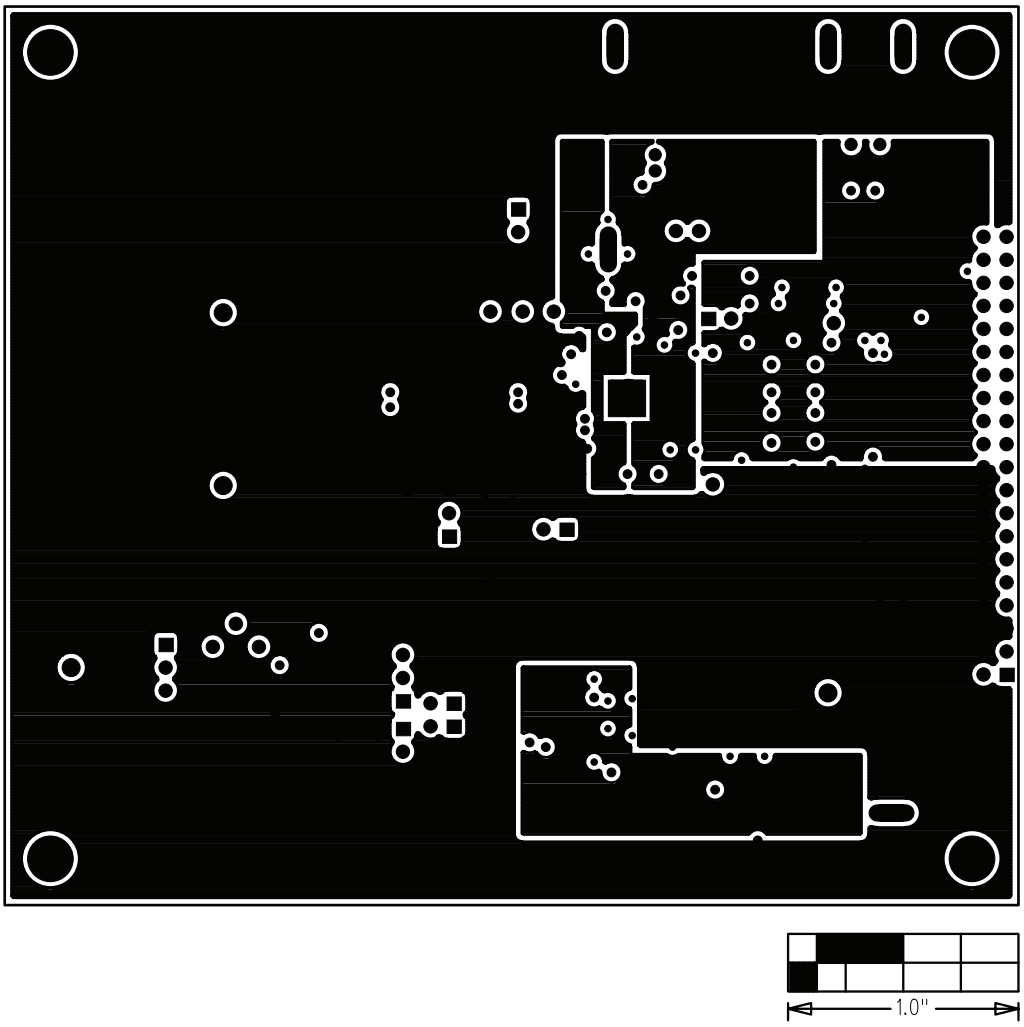


Figure 5. MAX12555 EV Kit PC Board Layout—Power Planes

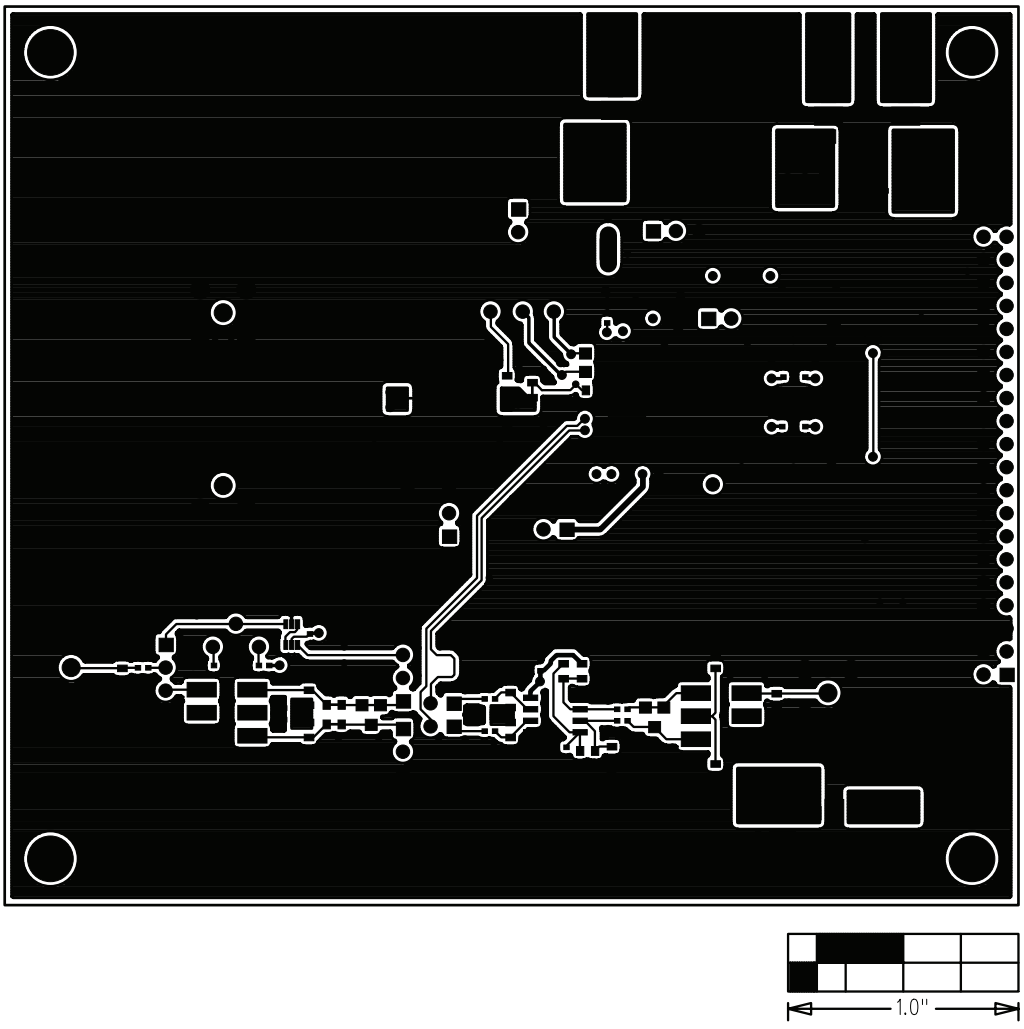
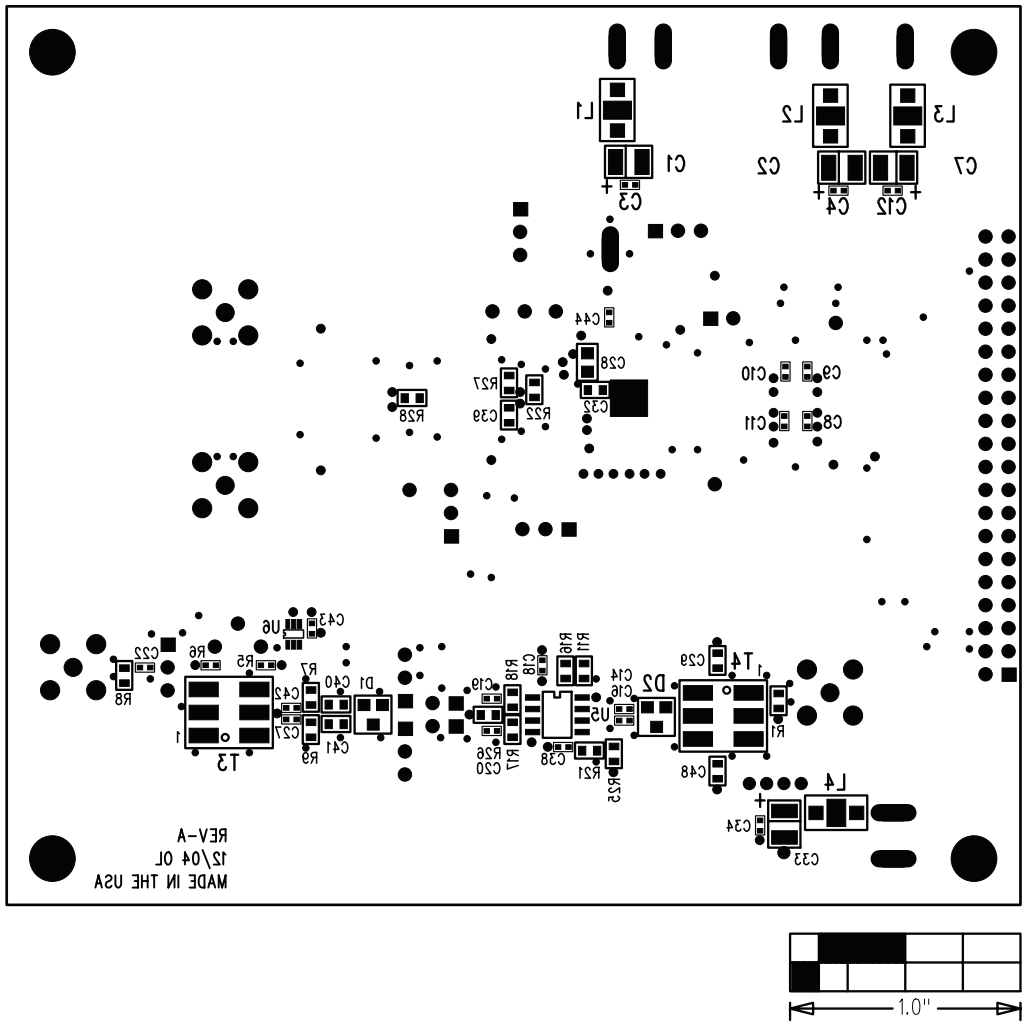


Figure 6. MAX12555 EV Kit PC Board Layout—Solder Side



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