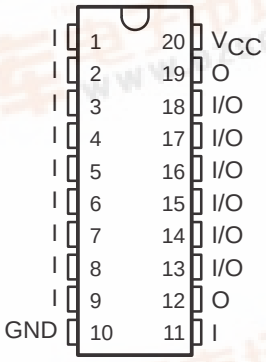
- **Choice of Operating Speeds**
  - **High-Speed, A Devices . . . 25 MHz Min**
  - **Half-Power, A-2 Devices . . . 16 MHz Min**
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

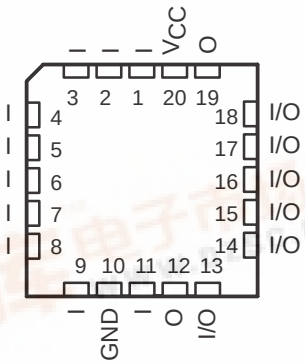
PAL16L8'
J OR W PACKAGE

(TOP VIEW)



PAL16L8'
FK PACKAGE

(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

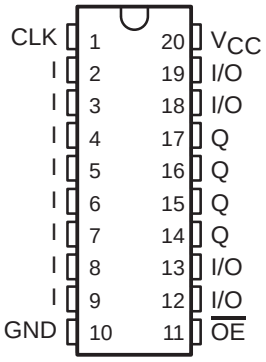
The PAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

PAL is a registered trademark of Advanced Micro Devices Inc.

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

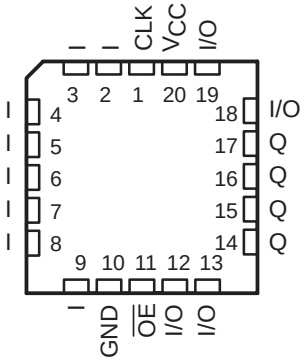
PAL16R4'
J OR W PACKAGE

(TOP VIEW)



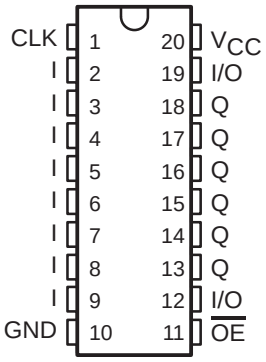
PAL16R4'
FK PACKAGE

(TOP VIEW)



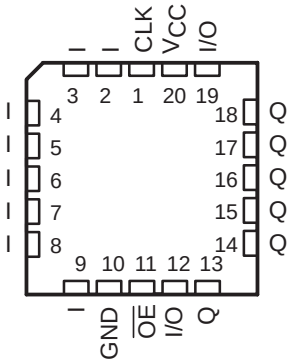
PAL16R6'
J OR W PACKAGE

(TOP VIEW)



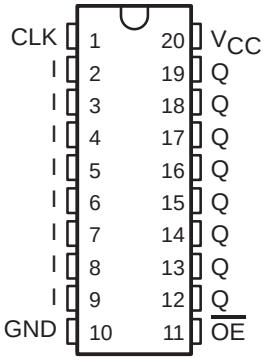
PAL16R6'
FK PACKAGE

(TOP VIEW)



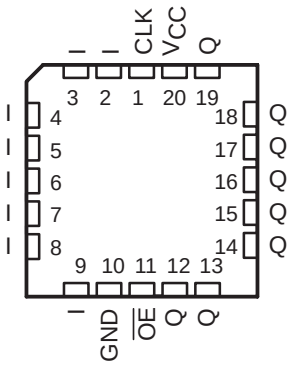
PAL16R8'
J OR W PACKAGE

(TOP VIEW)



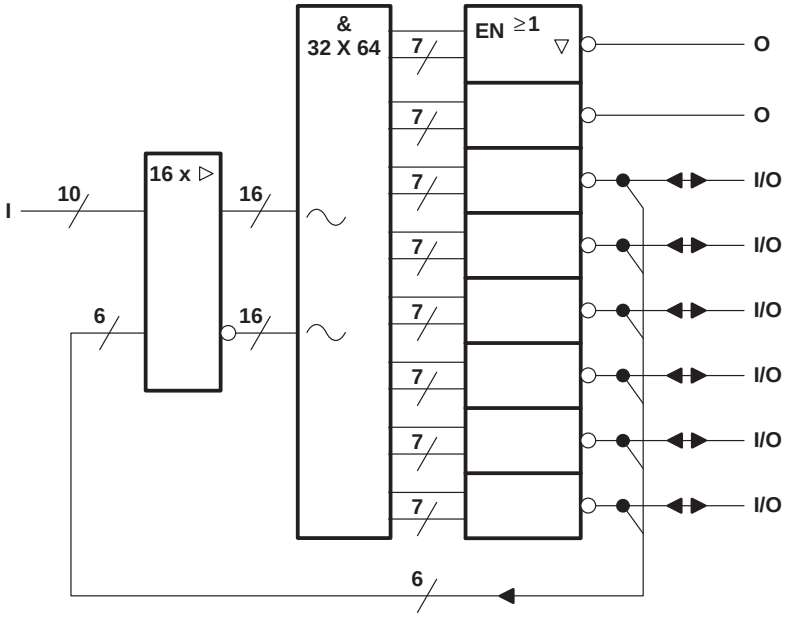
PAL16R8'
FK PACKAGE

(TOP VIEW)

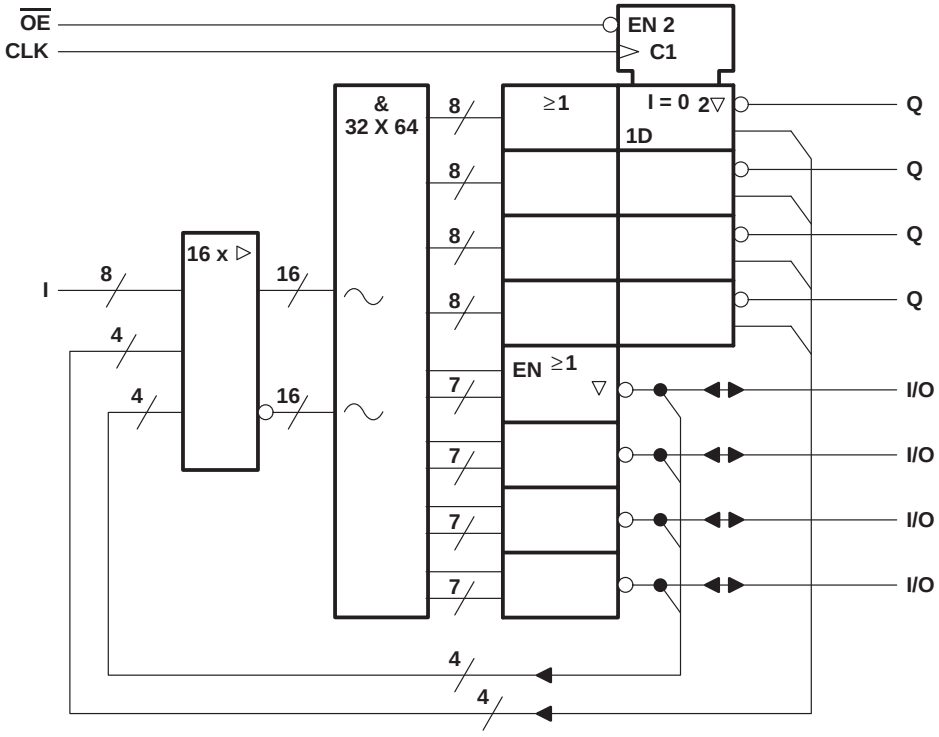


functional block diagrams (positive logic)

PAL16L8AM
PAL16L8A-2M



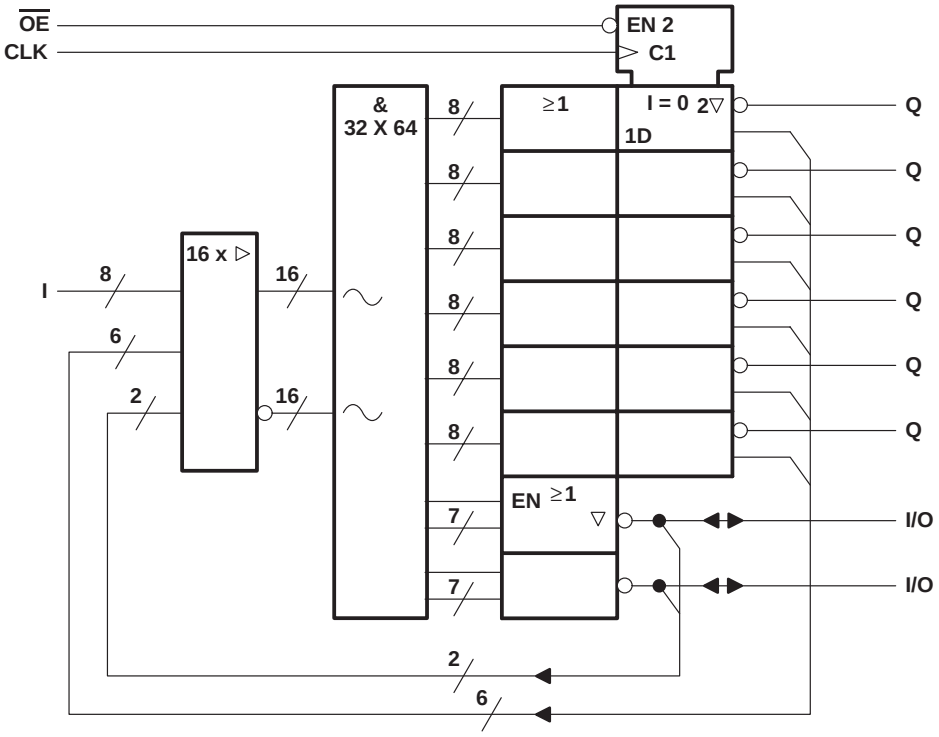
PAL16R4AM
PAL16R4A-2M



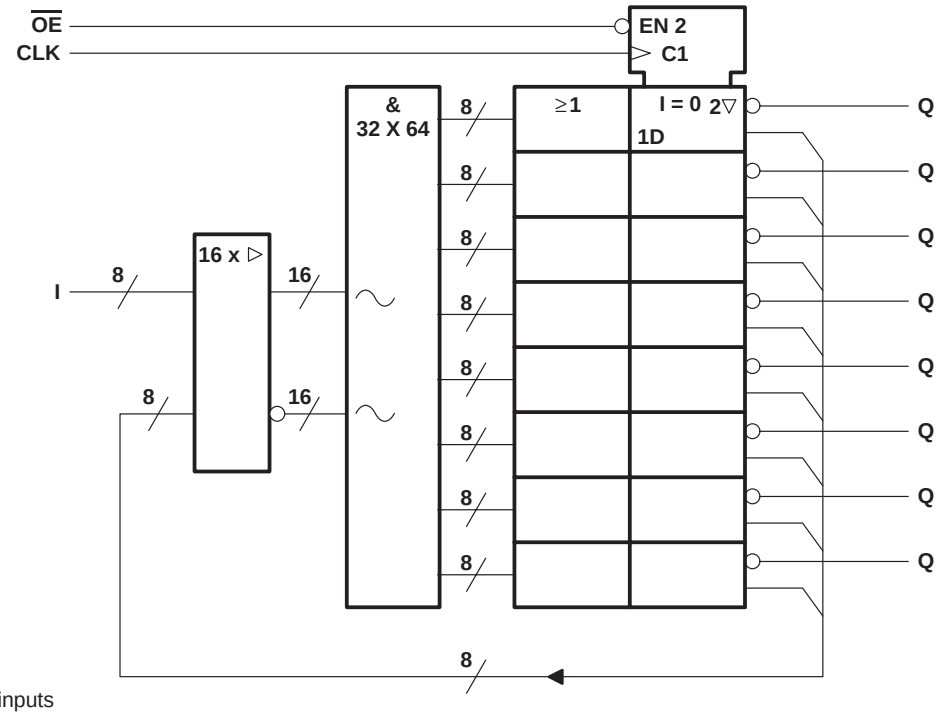
denotes fused inputs

functional block diagrams (positive logic)

PAL16R6AM
PAL16R6A-2M

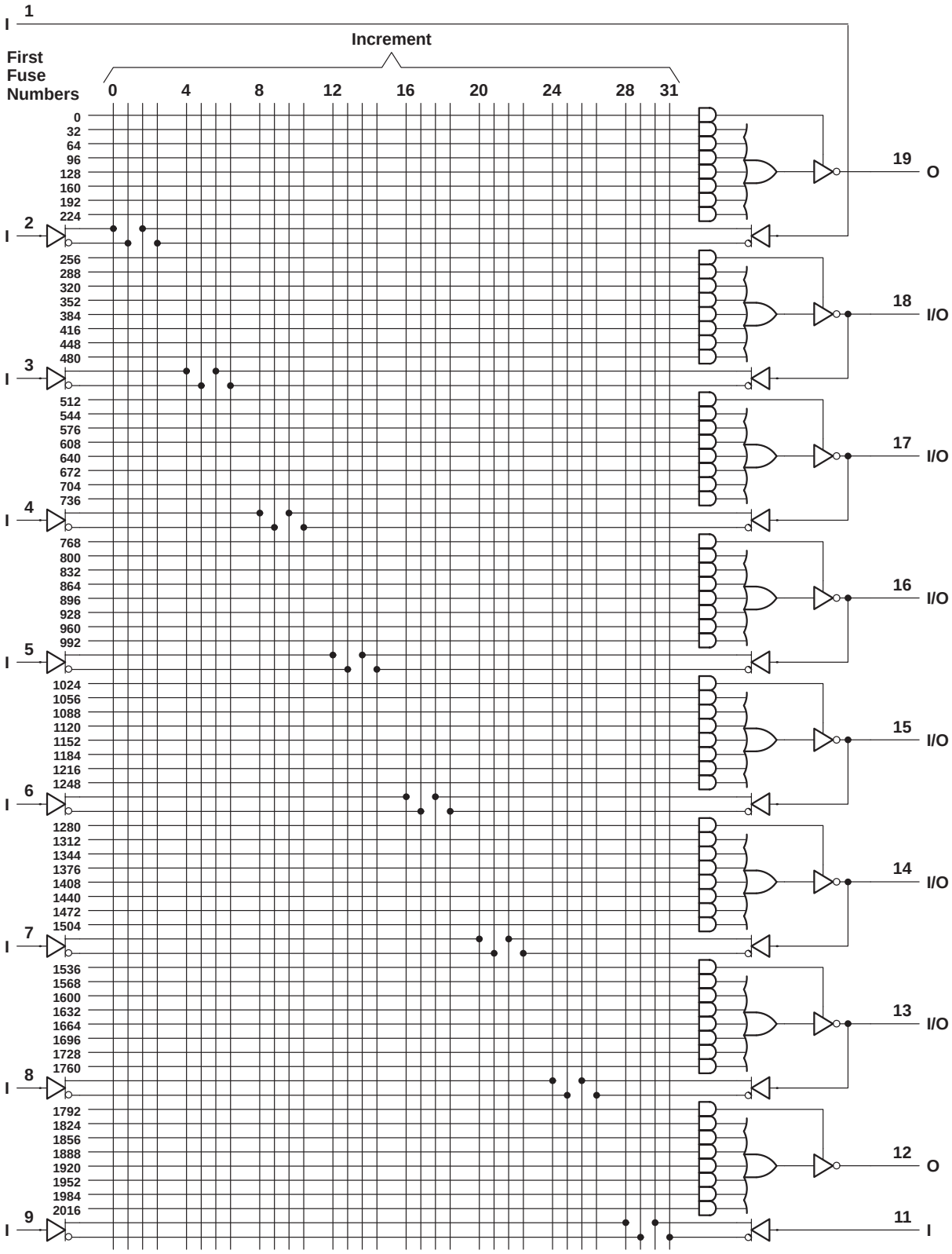


PAL16R8AM
PAL16R8A-2M



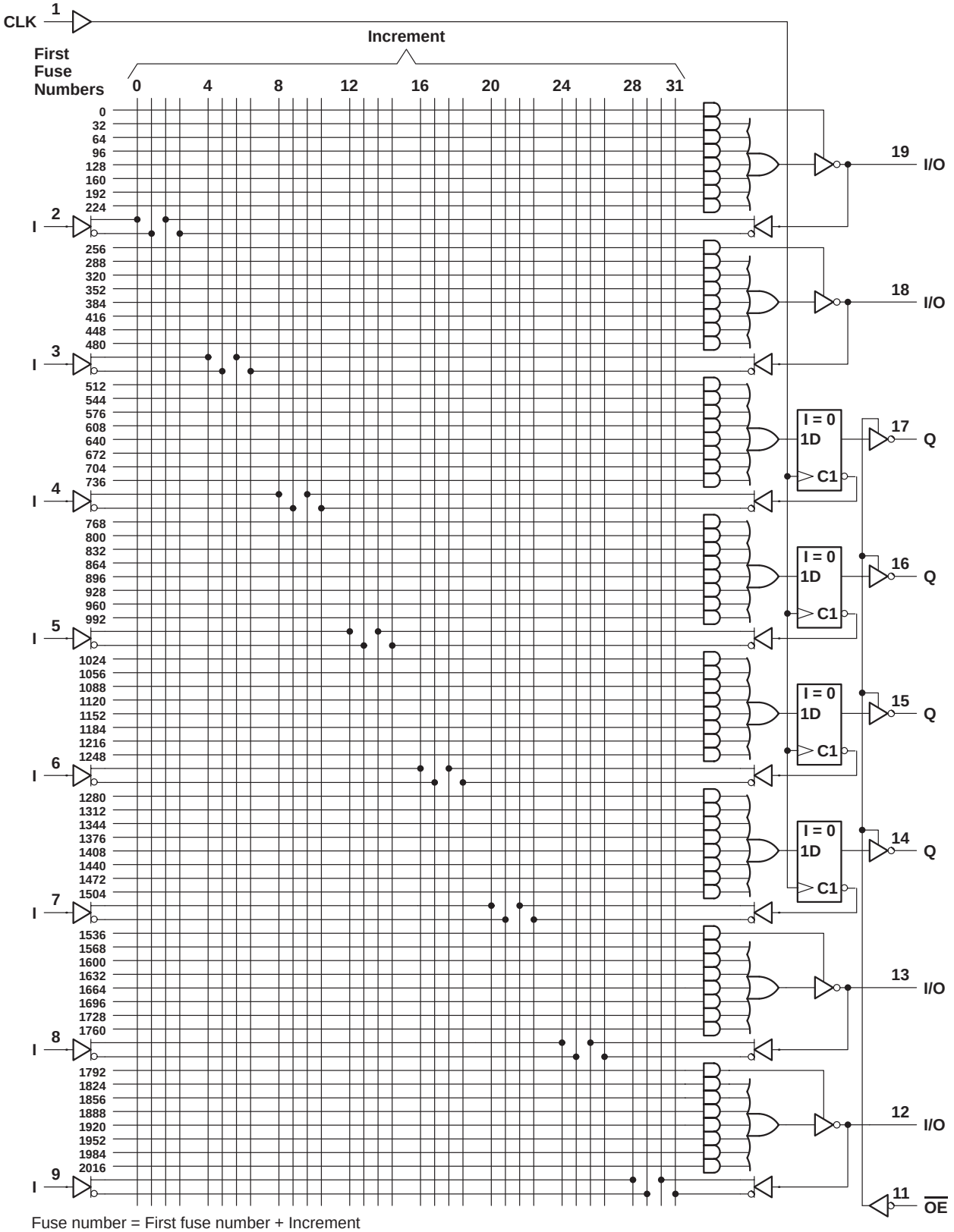
denotes fused inputs

logic diagram (positive logic)



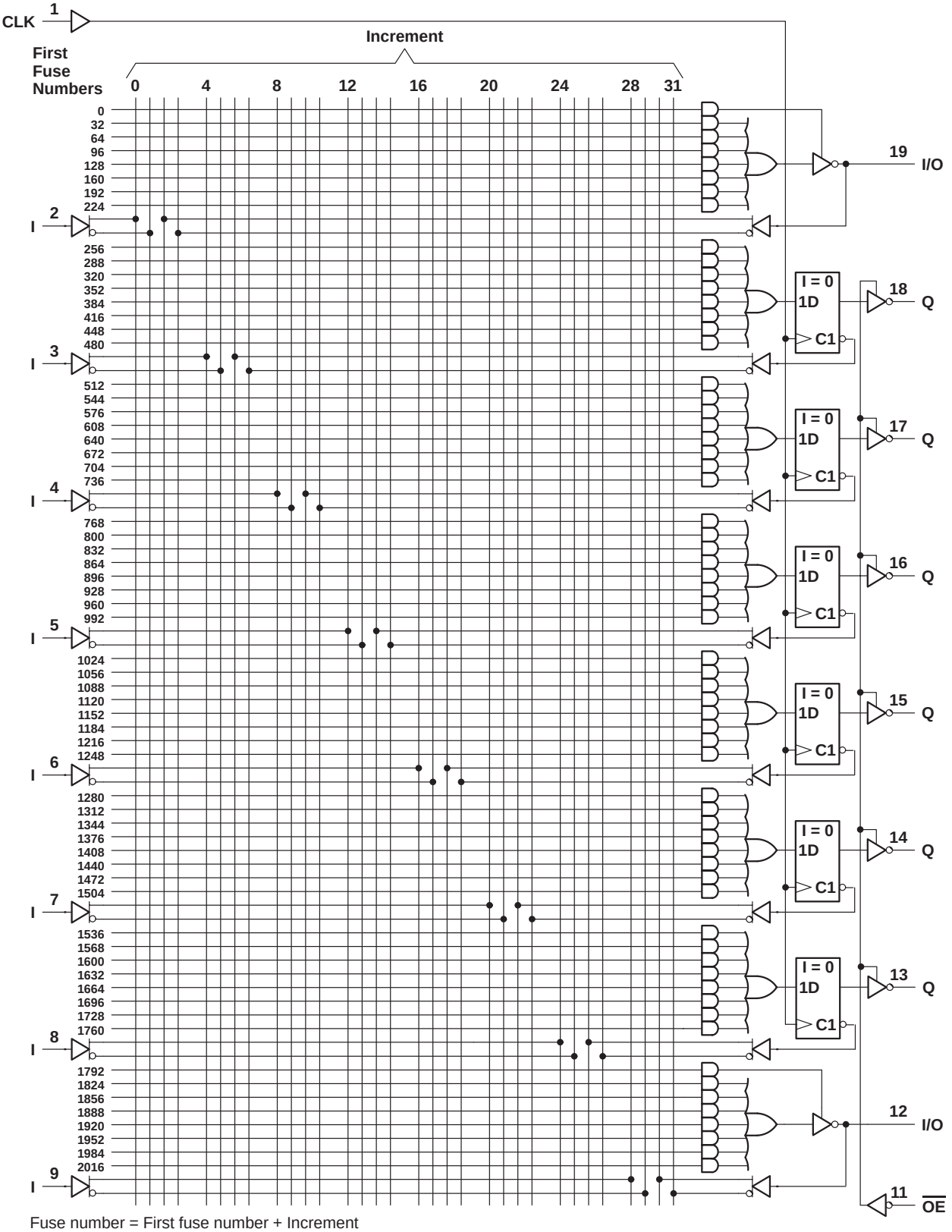
Fuse number = First fuse number + Increment

logic diagram (positive logic)



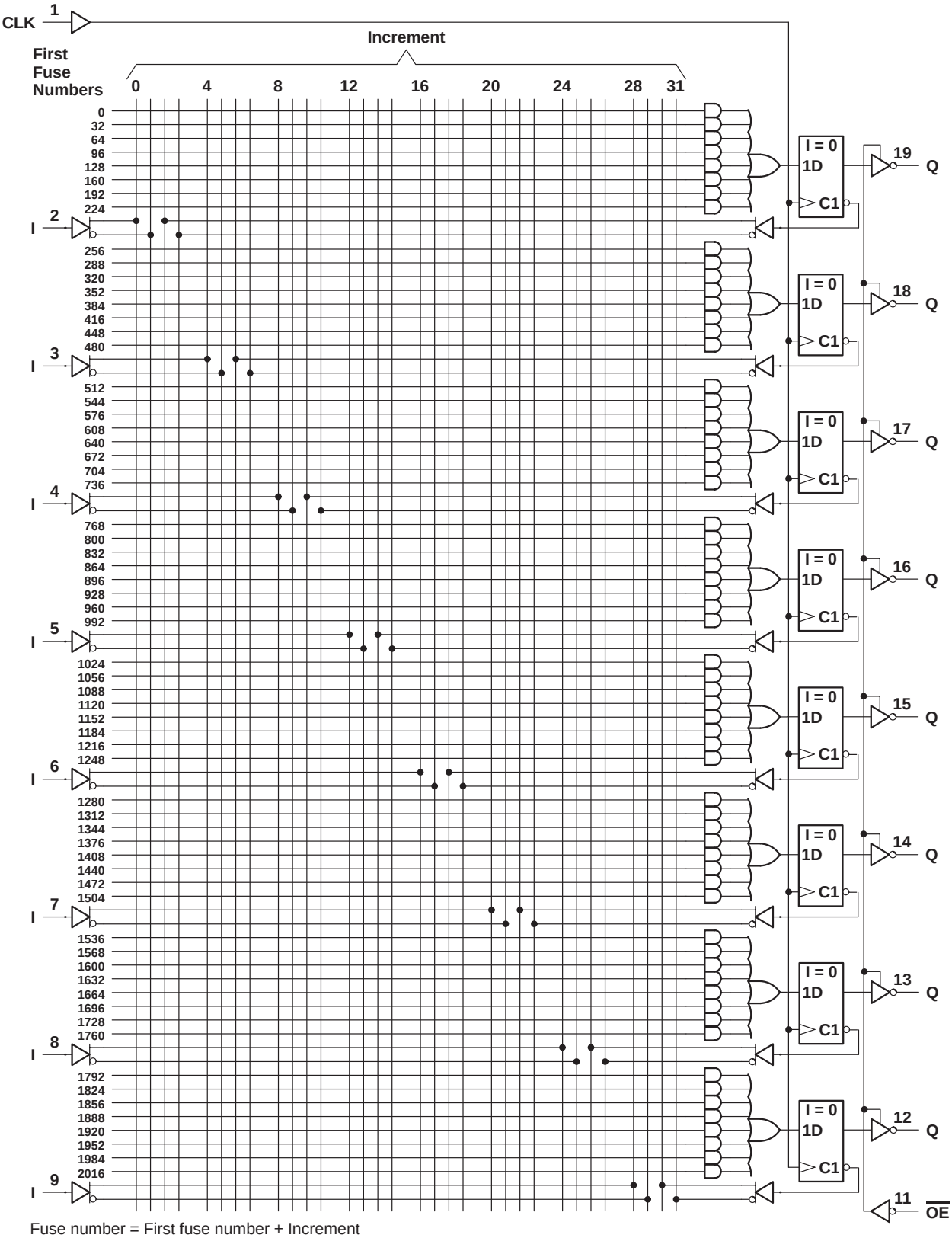
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–55	25	125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	µA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	µA
	I/O ports						–100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	µA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.2	mA
	All others						–0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	180	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	25	MHz
t_w	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t_{su}	Setup time, input or feedback before CLK↑		25		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}				25	45		MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		10	20	ns
t_{en}	$\overline{OE}$↓	Q	R2 = 750 Ω,		15	25	ns
t_{dis}	$\overline{OE}$↑	Q	See Figure 1		10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	µA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	µA
	I/O ports						–100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	µA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.2	mA
	All others						–0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	90	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	16	MHz
t_w	Pulse duration (see Note 2)	Clock high	25		ns
		Clock low	25		
t_{su}	Setup time, input or feedback before CLK↑		35		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

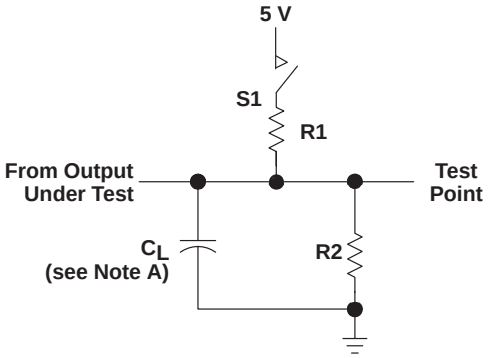
NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

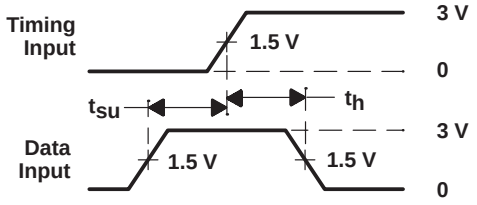
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}				16	25		MHz
t_{pd}	I, I/O	O, I/O			25	40	ns
t_{pd}	CLK↑	Q	R1 = 390 Ω,		11	25	ns
t_{en}	$\overline{OE}$↓	Q	R2 = 750 Ω,		20	25	ns
t_{dis}	$\overline{OE}$↑	Q	See Figure 1		11	25	ns
t_{en}	I, I/O	O, I/O			25	40	ns
t_{dis}	I, I/O	O, I/O			25	35	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

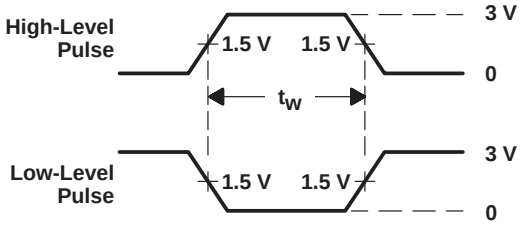
PARAMETER MEASUREMENT INFORMATION



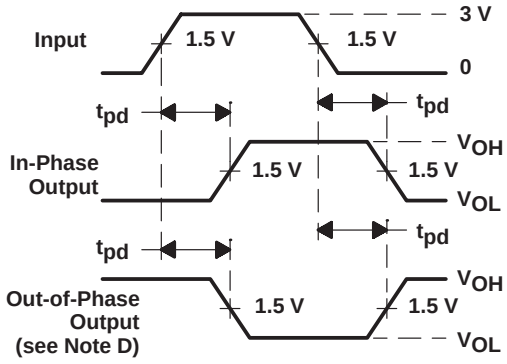
LOAD CIRCUIT FOR 3-STATE OUTPUTS



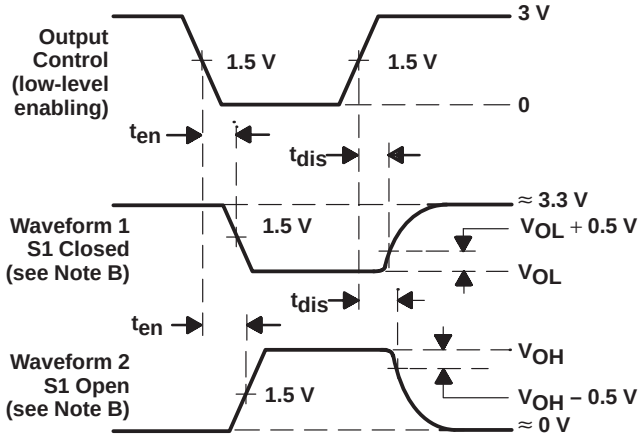
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
81036072A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103607RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103607SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036082A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103608RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103608SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036092A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103609RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103609SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036102A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103610RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103610SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036112A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103611RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103611SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036122A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103612RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103612SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036132A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103613RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103613SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
81036142A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8103614RA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
8103614SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8A-2MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8A-2MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8A-2MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8A-2MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8AMFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8AMJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8AMJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16L8AMWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4A-2MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4A-2MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4A-2MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4A-2MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4AMFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4AMJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4AMJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R4AMWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6A-2MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6A-2MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PAL16R6A-2MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6A-2MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6AMFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6AMJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6AMJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R6AMWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8A-2MFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8A-2MJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8A-2MJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8A-2MWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8AMFKB	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8AMJ	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8AMJB	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
PAL16R8AMWB	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265