



## 2.5V / 3.3V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

**IDT5V2528/A**

### FEATURES:

- Operates at 3.3V  $V_{DD}/AV_{DD}$  and 2.5V/3.3V  $V_{DDQ}$
- 1:10 fanout
- 3-level inputs for output control
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal
- No external RC network required for PLL loop stability
- Configurable 2.5V or 3.3V LVTTTL outputs
- $t_{PD}$  Phase Error at 100MHz to 166MHz:  $\pm 150ps$
- Jitter (peak-to-peak) at 133MHz and 166MHz:  $\pm 75ps$
- Spread spectrum compatible
- Operating Frequency:
  - Std: 25MHz to 140MHz
  - A: 25MHz to 167MHz
- Available in TSSOP package

### DESCRIPTION:

The IDT5V2528 is a high performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal.

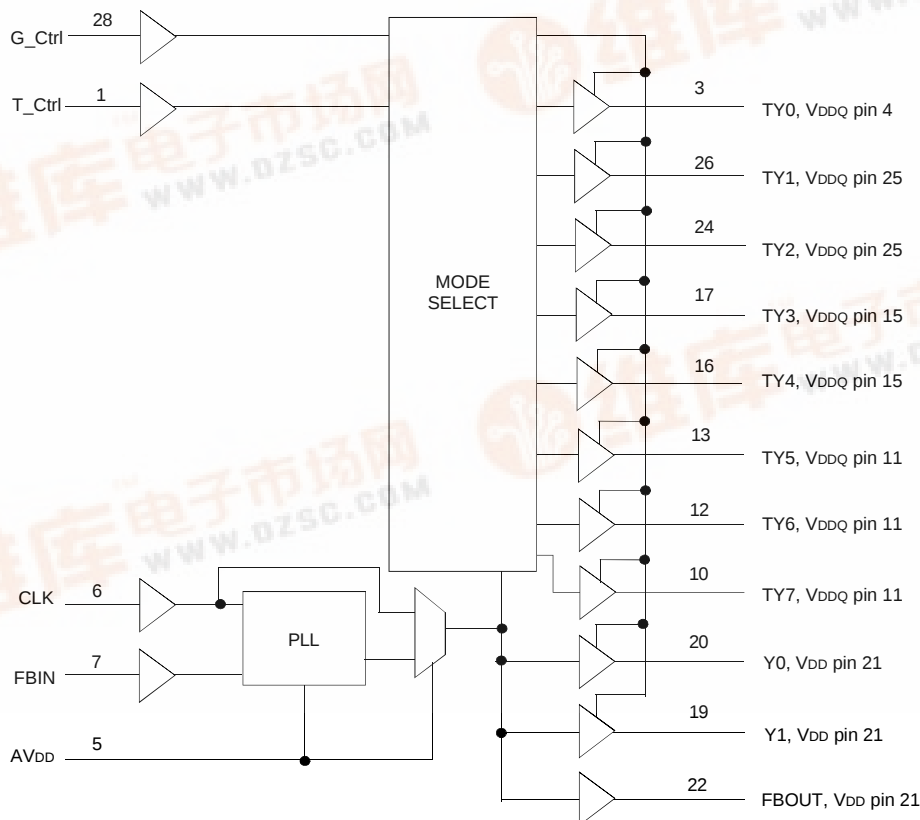
The IDT5V2528 inputs, PLL core,  $Y_0$ ,  $Y_1$ , and FBOUT buffers operate from the 3.3V  $V_{DD}$  and  $AV_{DD}$  power supply pins.

One bank of ten outputs provide low-skew, low-jitter copies of CLK. Of the ten outputs, up to seven may be configured for 2.5V or 3.3V LVTTTL outputs. The number of 2.5V outputs is controlled by 3-level input signals  $G\_Ctrl$  and  $T\_Ctrl$ , and by connecting the appropriate  $V_{DDQ}$  pins to 2.5V or 3.3V. The 3-level input signals may be hard-wired to high-mid-low levels. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. The outputs can be enabled or disabled via the  $G\_Ctrl$  input. When the  $G\_Ctrl$  input is mid or high, the outputs switch in phase and frequency with CLK; when the  $G\_Ctrl$  is low, all outputs (except FBOUT) are disabled to the logic-low state.

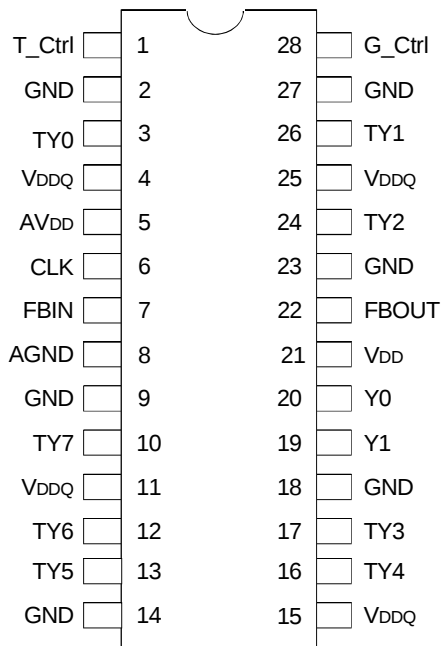
Unlike many products containing PLLs, the IDT5V2528 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the IDT5V2528 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping  $AV_{DD}$  to ground.

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



**TSSOP**  
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol                                                                    | Rating                                                       | Max.                         | Unit |
|---------------------------------------------------------------------------|--------------------------------------------------------------|------------------------------|------|
| V <sub>DD</sub> , V <sub>DDQ</sub> , AV <sub>DD</sub>                     | Supply Voltage Range                                         | −0.5 to +4.6                 | V    |
| V <sub>I</sub> <sup>(2)</sup>                                             | Input Voltage Range                                          | −0.5 to +5.5                 | V    |
| V <sub>O</sub> <sup>(2)</sup>                                             | Voltage Range applied to any output in the HIGH or LOW state | −0.5 to V <sub>DD</sub> +0.5 | V    |
| I <sub>IK</sub> (V <sub>I</sub> < 0)                                      | Input Clamp Current                                          | −50                          | mA   |
| I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub> ) | Output Clamp Current                                         | ±50                          | mA   |
| I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DD</sub> )                   | Continuous Output Current                                    | ±50                          | mA   |
| V <sub>DD</sub> or GND                                                    | Continuous Current                                           | ±200                         | mA   |
| T <sub>STG</sub>                                                          | Storage Temperature Range                                    | −65 to +150                  | °C   |
| T <sub>J</sub>                                                            | Junction Temperature                                         | +150                         | °C   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## CAPACITANCE<sup>(1)</sup>

| Symbol          | Description                                                   | Min          | Typ. | Max. | Unit |
|-----------------|---------------------------------------------------------------|--------------|------|------|------|
| C <sub>IN</sub> | Input Capacitance<br>V <sub>I</sub> = V <sub>DD</sub> or GND  | —            | 5    | —    | pF   |
| C <sub>O</sub>  | Output Capacitance<br>V <sub>I</sub> = V <sub>DD</sub> or GND | —            | 6    | —    | pF   |
| C <sub>L</sub>  | Load Capacitance                                              | 2.5V outputs | —    | 20   | pF   |
|                 |                                                               | 3.3V outputs | —    | 30   |      |

### NOTE:

- Unused inputs must be held HIGH or LOW to prevent them from floating.

## RECOMMENDED OPERATING RANGE

| Symbol                                            | Description                   | Min.         | Typ. | Max. | Unit |
|---------------------------------------------------|-------------------------------|--------------|------|------|------|
| V <sub>DD</sub> , AV <sub>DD</sub> <sup>(1)</sup> | Power Supply Voltage          | 3            | 3.3  | 3.6  | V    |
| V <sub>DDQ</sub> <sup>(1)</sup>                   | Power Supply Voltage          | 2.5V Outputs | 2.3  | 2.5  | V    |
|                                                   |                               | 3.3V Outputs | 3    | 3.3  |      |
| T <sub>A</sub>                                    | Ambient Operating Temperature | −40          | +25  | +85  | °C   |

### NOTE:

- All power supplies should operate in tandem. If V<sub>DD</sub> or V<sub>DDQ</sub> is at a maximum, then V<sub>DDQ</sub> or V<sub>DD</sub> (respectively) should be at maximum, and vice-versa.

## PIN DESCRIPTION

| Terminal              |                               | Type    | Description                                                                                                                                                                                                                                                             |
|-----------------------|-------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Name                  | No.                           |         |                                                                                                                                                                                                                                                                         |
| CLK <sup>(1)</sup>    | 6                             | I       | Clock input                                                                                                                                                                                                                                                             |
| FBIN                  | 7                             | I       | Feedback input                                                                                                                                                                                                                                                          |
| G_Ctrl <sup>(2)</sup> | 28                            | 3-level | 3-level input for 2.5V/3.3V Output Select/Output bank enable. When G_Ctrl is LOW, all outputs except FBOUT are disabled to a logic-LOW state. When G_Ctrl is MID or HIGH, all outputs are enabled and switch at the same frequency as CLK (see OUTPUT SELECTION table). |
| T_Ctrl <sup>(2)</sup> | 1                             | 3-level | 3-level input for 2.5V/3.3V Output Select (see OUTPUT SELECTION table)                                                                                                                                                                                                  |
| FBOUT                 | 22                            | O       | Feedback output                                                                                                                                                                                                                                                         |
| TY <sup>(7:0)</sup>   | 3, 10, 12, 13, 16, 17, 24, 26 | O       | 2.5V or 3.3V Clock outputs. 1, 2, 3, 5, or 7 of these outputs may be selected as 2.5V outputs (see OUTPUT SELECTION table).                                                                                                                                             |
| Y <sup>(1:0)</sup>    | 19, 20                        | O       | 3.3V Clock Outputs                                                                                                                                                                                                                                                      |
| AVDD <sup>(3)</sup>   | 5                             | Power   | 3.3V Analog power supply. AVDD provides the power reference for the analog circuitry.                                                                                                                                                                                   |
| AGND                  | 8                             | Ground  | Analog ground. AGND provides the ground reference for the analog circuitry.                                                                                                                                                                                             |
| VDD                   | 21                            | Power   | 3.3V Power supply                                                                                                                                                                                                                                                       |
| VDDQ                  | 4, 11, 15, 25                 | Power   | 2.5V or 3.3V Power supply for TY outputs                                                                                                                                                                                                                                |
| GND                   | 2, 9, 14, 18, 23, 27          | Ground  | Ground                                                                                                                                                                                                                                                                  |

### NOTES:

- CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time of 1ms is required for the PLL to phase lock the feedback signal to the reference signal.
- 3-level inputs will float to MID logic level if left unconnected.
- AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the outputs.

## STATIC FUNCTION TABLE (AVDD = 0V)<sup>(1)</sup>

| Inputs                           |        |         | Outputs             |                    |         |
|----------------------------------|--------|---------|---------------------|--------------------|---------|
| G_Ctrl                           | T_Ctrl | CLK     | TY <sup>(7:0)</sup> | Y <sup>(1:0)</sup> | FBOUT   |
| L                                | X      | L       | L                   | L                  | L       |
| L                                | X      | H       | L                   | L                  | H       |
| see<br>OUTPUT SELECTION<br>table |        | H       | H                   | H                  | H       |
|                                  |        | L       | L                   | L                  | L       |
|                                  |        | running | running             | running            | running |

### NOTE:

- AVDD should be powered up along with VDD, before setting AVDD to ground, to put the control pins in a valid state.

## OUTPUT SELECTION

| G_Ctrl | T_Ctrl | TY <sup>(7:0)</sup>                                                                                    | VDDQ<br>Configuration                   |
|--------|--------|--------------------------------------------------------------------------------------------------------|-----------------------------------------|
| M      | L      | TY <sub>0</sub> (2.5V)<br>TY <sub>1</sub> - TY <sub>7</sub> (3.3V)                                     | Pin 4 (2.5V)<br>Pins 11, 15, 25 (3.3V)  |
| M      | M      | TY <sub>1</sub> , TY <sub>2</sub> (2.5V)<br>TY <sub>0</sub> , TY <sub>3</sub> - TY <sub>7</sub> (3.3V) | Pin 25 (2.5V)<br>Pins 4, 11, 15 (3.3V)  |
| M      | H      | TY <sub>0</sub> - TY <sub>2</sub> (2.5V)<br>TY <sub>3</sub> - TY <sub>7</sub> (3.3V)                   | Pins 4, 25 (2.5V)<br>Pins 11, 15 (3.3V) |
| H      | L      | TY <sub>0</sub> - TY <sub>4</sub> (2.5V)<br>TY <sub>5</sub> - TY <sub>7</sub> (3.3V)                   | Pins 4, 15, 25 (2.5V)<br>Pin 11 (3.3V)  |
| H      | M      | TY <sub>1</sub> - TY <sub>7</sub> (2.5V)<br>TY <sub>0</sub> (3.3V)                                     | Pins 11, 15, 25 (2.5V)<br>Pin 4 (3.3V)  |
| H      | H      | TY <sub>0</sub> - TY <sub>7</sub> (3.3V)                                                               | Pins 4, 11, 15, 25 (3.3V)               |

## DYNAMIC FUNCTION TABLE (AVDD = 3.3V)

| Inputs                        |        |     | Outputs             |                    |       |
|-------------------------------|--------|-----|---------------------|--------------------|-------|
| G_Ctrl                        | T_Ctrl | CLK | TY <sup>(7:0)</sup> | Y <sup>(1:0)</sup> | FBOUT |
| L                             | X      | L   | L                   | L                  | L     |
| L                             | X      | H   | L                   | L                  | H     |
| see OUTPUT<br>SELECTION table |        | L   | L                   | L                  | L     |
|                               |        | H   | H                   | H                  | H     |

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol           | Parameter                                    | Test Conditions                         |            | Min.                     | Typ. <sup>(1)</sup> | Max                      | Unit |
|------------------|----------------------------------------------|-----------------------------------------|------------|--------------------------|---------------------|--------------------------|------|
| V <sub>IK</sub>  | Input Clamp Voltage                          | I <sub>I</sub> = -18mA                  |            |                          |                     | -1.2                     | V    |
| V <sub>IH</sub>  | Input HIGH Level                             | CLK, FBIN                               |            | 2                        |                     |                          | V    |
| V <sub>IL</sub>  | Input LOW Level                              | CLK, FBIN                               |            |                          |                     | 0.8                      | V    |
| V <sub>IHH</sub> | Input HIGH Voltage Level <sup>(2)</sup>      | 3-Level Inputs Only                     |            | V <sub>DD</sub> - 0.6    |                     |                          | V    |
| V <sub>IMM</sub> | Input MID Voltage Level <sup>(2)</sup>       | 3-Level Inputs Only                     |            | V <sub>DD</sub> /2 - 0.3 |                     | V <sub>DD</sub> /2 + 0.3 | V    |
| V <sub>ILL</sub> | Input LOW Voltage Level <sup>(2)</sup>       | 3-Level Inputs Only                     |            |                          |                     | 0.6                      | V    |
| V <sub>OH</sub>  | Output HIGH Voltage Level<br>(3.3V Outputs)  | I <sub>OH</sub> = -100μA                |            | V <sub>DD</sub> - 0.2    |                     |                          | V    |
|                  |                                              | I <sub>OH</sub> = -12mA                 |            | 2.4                      |                     |                          |      |
| V <sub>OH</sub>  | Output HIGH Voltage Level<br>(2.5V Outputs)  | I <sub>OH</sub> = -100μA                |            | V <sub>DD</sub> - 0.1    |                     |                          | V    |
|                  |                                              | I <sub>OH</sub> = -12mA                 |            | 2                        |                     |                          |      |
| V <sub>OL</sub>  | Output LOW Voltage Level<br>(3.3V Outputs)   | I <sub>OL</sub> = 100μA                 |            |                          |                     | 0.2                      | V    |
|                  |                                              | I <sub>OL</sub> = 12mA                  |            |                          |                     | 0.4                      |      |
| V <sub>OL</sub>  | Output LOW Voltage Level<br>(2.5V Outputs)   | I <sub>OL</sub> = 100μA                 |            |                          |                     | 0.1                      | V    |
|                  |                                              | I <sub>OL</sub> = 12mA                  |            |                          |                     | 0.4                      |      |
| I <sub>3</sub>   | 3-Level Input DC Current<br>(G_Ctrl, T_Ctrl) | V <sub>IN</sub> = V <sub>DD</sub>       | HIGH Level |                          |                     | +200                     | μA   |
|                  |                                              | V <sub>IN</sub> = V <sub>DD</sub> /2    | MID Level  | -50                      |                     | +50                      |      |
|                  |                                              | V <sub>IN</sub> = GND                   | LOW Level  | -200                     |                     |                          |      |
| I <sub>I</sub>   | Input Current                                | V <sub>I</sub> = V <sub>DD</sub> or GND |            |                          |                     | ±5                       | μA   |

### NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
- These inputs are normally wired to V<sub>DD</sub>, GND, or left floating. Internal termination resistors bias floating inputs to V<sub>DD</sub>/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t<sub>LOCK</sub> time before all datasheet limits are achieved.

## POWER SUPPLY CHARACTERISTICS

| Symbol            | Parameter                                  | Test Conditions                                                                                           | Typ. <sup>(1)</sup> | Max | Unit   |
|-------------------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------|---------------------|-----|--------|
| I <sub>DDPD</sub> | Power Down Supply Current                  | V <sub>DD</sub> = 3.6, V <sub>DDQ</sub> = 2.7V / 3.3V, AV <sub>DD</sub> = 0V                              | 8                   | 40  | μA     |
| I <sub>DDA</sub>  | AV <sub>DD</sub> Supply Current            | V <sub>DD</sub> = AV <sub>DD</sub> = 3.6V, V <sub>DDQ</sub> = 2.7V / 3.3V, CLK = 0 or V <sub>DD</sub>     | 3.5                 | 10  | mA     |
| I <sub>DD</sub>   | Dynamic Power Supply Current               | V <sub>DD</sub> = AV <sub>DD</sub> = 3.6V, V <sub>DDQ</sub> = 2.7V / 3.3V, C <sub>L</sub> = 0pF           | 500                 | —   | μA/MHz |
| I <sub>DDD</sub>  | Dynamic Power Supply<br>Current per Output | V <sub>DD</sub> = AV <sub>DD</sub> = V <sub>DDQ</sub> = 3.6V<br>C <sub>L</sub> = 30pF, CLK = 100MHz       | 15                  | —   | mA     |
|                   |                                            | V <sub>DD</sub> = AV <sub>DD</sub> = 3.6V, V <sub>DDQ</sub> = 2.7V<br>C <sub>L</sub> = 20pF, CLK = 100MHz | 12                  | —   |        |

### NOTE:

- For nominal voltage and temperature.

## INPUT TIMING REQUIREMENTS OVER OPERATING RANGE

|                   |                                   | 5V2528 |     | 5V2528A |     | Units |
|-------------------|-----------------------------------|--------|-----|---------|-----|-------|
|                   |                                   | Min    | Max | Min     | Max |       |
| f <sub>CLK</sub>  | Clock frequency                   | 25     | 140 | 25      | 167 | MHz   |
|                   | Input clock duty cycle            | 40%    | 60% | 40%     | 60% |       |
| t <sub>LOCK</sub> | Stabilization time <sup>(1)</sup> |        | 1   |         | 1   | ms    |

**NOTE:**  
 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 5V2528<sup>(1)</sup>

| Symbol                                           | Parameter <sup>(2)</sup>                                                   | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|----------------------------------------------------------------------------|------|------|------|------|
| t <sub>PHASE ERROR</sub>                         | Phase Error from Rising Edge CLK to Rising Edge FBIN (100MHz-133MHz)       | −150 | —    | 150  | ps   |
| t <sub>PHASE ERROR - jitter</sub> <sup>(3)</sup> | Phase Error minus Jitter from Rising Edge CLK to Rising Edge FBIN (133MHz) | −50  | —    | 50   | ps   |
| tsk1(0) <sup>(4)</sup>                           | Output Skew between 3.3V Outputs                                           | —    | —    | 150  | ps   |
| tsk2(0) <sup>(4)</sup>                           | Output Skew between 2.5V Outputs                                           | —    | —    | 150  | ps   |
| tsk3(0) <sup>(4,5)</sup>                         | Output Skew between 2.5V and 3.3V Outputs                                  | —    | —    | 200  | ps   |
| t <sub>j</sub>                                   | Cycle-to-Cycle Output Jitter (Peak-to-Peak) at 133MHz                      | −75  | —    | 75   | ps   |
|                                                  | Duty Cycle                                                                 | 45   | —    | 55   | %    |
| t <sub>R</sub>                                   | Output Rise Time for 3.3V Outputs (20% to 80%)                             | 0.8  | —    | 2.1  | ns   |
| t <sub>F</sub>                                   | Output Fall Time for 3.3V Outputs (20% to 80%)                             | 0.8  | —    | 2.1  | ns   |
| t <sub>R</sub>                                   | Output Rise Time for 2.5V Outputs (20% to 80%)                             | 0.5  | —    | 1.5  | ns   |
| t <sub>F</sub>                                   | Output Fall Time for 2.5V Outputs (20% to 80%)                             | 0.5  | —    | 1.5  | ns   |

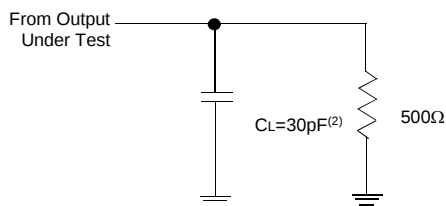
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - 5V2528A<sup>(1)</sup>

| Symbol                                           | Parameter <sup>(2)</sup>                                                   | Min.             | Typ. | Max. | Unit |
|--------------------------------------------------|----------------------------------------------------------------------------|------------------|------|------|------|
| t <sub>PHASE ERROR</sub>                         | Phase Error from Rising Edge CLK to Rising Edge FBIN (100MHz-166MHz)       | −150             | —    | 150  | ps   |
| t <sub>PHASE ERROR - jitter</sub> <sup>(3)</sup> | Phase Error minus Jitter from Rising Edge CLK to Rising Edge FBIN (166MHz) | −50              | —    | 50   | ps   |
| tsk1(0) <sup>(4)</sup>                           | Output Skew between 3.3V Outputs                                           | —                | —    | 150  | ps   |
| tsk2(0) <sup>(4)</sup>                           | Output Skew between 2.5V Outputs                                           | —                | —    | 150  | ps   |
| tsk3(0) <sup>(4,5)</sup>                         | Output Skew between 2.5V and 3.3V Outputs                                  | 25MHz to 133MHz  | —    | 200  | ps   |
|                                                  |                                                                            | 133MHz to 166MHz | —    | 250  |      |
| t <sub>j</sub>                                   | Cycle-to-Cycle Output Jitter (Peak-to-Peak) at 166MHz                      | −75              | —    | 75   | ps   |
|                                                  | Duty Cycle                                                                 | 45               | —    | 55   | %    |
| t <sub>R</sub>                                   | Output Rise Time for 3.3V Outputs (20% to 80%)                             | 0.8              | —    | 2.1  | ns   |
| t <sub>F</sub>                                   | Output Fall Time for 3.3V Outputs (20% to 80%)                             | 0.8              | —    | 2.1  | ns   |
| t <sub>R</sub>                                   | Output Rise Time for 2.5V Outputs (20% to 80%)                             | 0.5              | —    | 1.5  | ns   |
| t <sub>F</sub>                                   | Output Fall Time for 2.5V Outputs (20% to 80%)                             | 0.5              | —    | 1.5  | ns   |

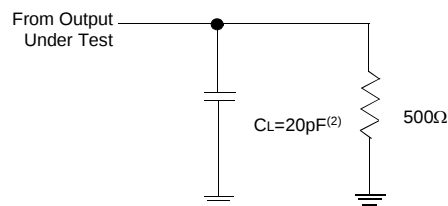
**NOTES:**

1. All parameters are measured with the following load conditions: 30pF || 500Ω for 3.3V outputs and 20pF || 500Ω for 2.5V outputs.
2. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
3. Phase error does not include jitter.
4. All skew parameters are only valid for equal loading of all outputs.
5. Measured for V<sub>DDQ</sub> = 2.3V and 3V, 2.5V and 3.3V, or 2.7V and 3.6V.

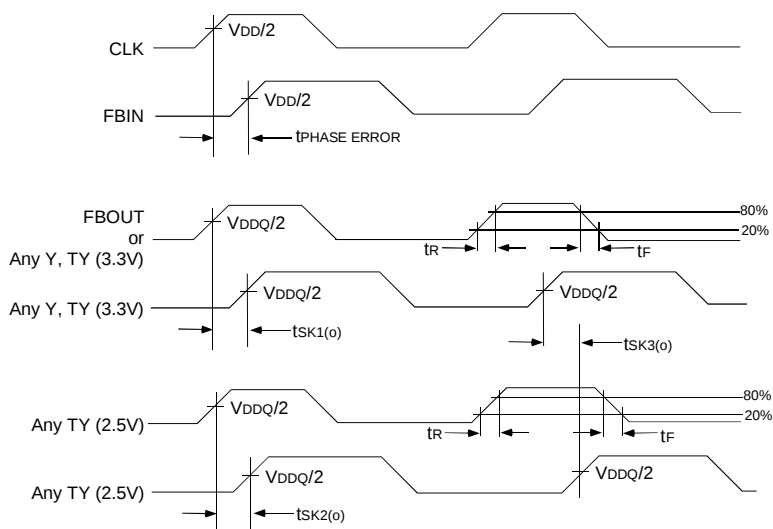
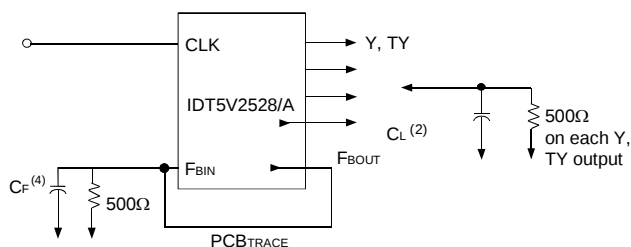
## TEST CIRCUIT AND VOLTAGE WAVEFORMS



*Test Circuit for 3.3V Outputs*



*Test Circuit for 2.5V Outputs*



### PHASE ERROR AND SKEW CALCULATIONS<sup>(3,4)</sup>

#### NOTES:

1. All inputs pulses are supplied by generators having the following characteristics:  $\text{PRR} \leq 100\text{MHz}$ ,  $Z_0 = 50\Omega$ ,  $t_R \leq 1.2\text{ ns}$ ,  $t_F \leq 1.2\text{ ns}$ .
2.  $C_L$  includes probe and jig capacitance.
3. The outputs are measured one at a time with one transition per measurement.
4. Phase error measurements require equal loading at outputs Y, TY, and FBOU.  $C_F = C_L - C_{\text{FBIN}} - C_{\text{PCBtrace}}$ ;  $C_{\text{FBIN}} \cong 5\text{pF}$ .

## ORDERING INFORMATION

| IDT         | XXXXX   | XX      | X                 |  |                                                    |
|-------------|---------|---------|-------------------|--|----------------------------------------------------|
| Device Type | Package | Process |                   |  |                                                    |
|             |         |         | I                 |  | -40°C to +85°C (Industrial)                        |
|             |         |         | PG<br>PGG         |  | Thin Shrink Small Outline Package<br>TSSOP - Green |
|             |         |         | 5V2528<br>5V2528A |  | 2.5V / 3.3V Phase-Lock Loop Clock Driver           |



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