

# NCP5208

## DDR-I/II Termination Regulator

The NCP5208 is a linear regulator specifically designed for the active termination of DDR-I/II SDRAM. The device can be operated from a single supply voltage as low as 1.7 V. For DDR-I applications, the device is capable of sourcing and sinking current up to 1.5 A with the output voltage regulated to within  $\pm 3\%$  or better. A separate voltage feedback pin ensures superior load regulation against load and line changes.

Protective features include soft-start, source/sink current limits and thermal shutdown. Open-drain VTT OK output ( $\overline{POK}$ ) is added for system monitoring. The shutdown pin can tri-state the regulator output for Suspend To RAM (STR) state. This device is available in a SO-8 package.

### Features

- Supports Both DDR-I and DDR-II SDRAM Requirements
- Single Supply Voltage Operation as Low as 1.7 V
- Integrated Power MOSFETs
- Few External Components Needed
- Source and Sink Current Up to 1.5 A
- Load Regulation Within  $\pm 3\%$
- Both Source and Sink Current Limits
- Open-Drain VTT OK ( $\overline{POK}$ ) Pin
- Shutdown Pin
- Thermal Shutdown
- Housed in SO-8 Package

### Typical Applications

- DDR Termination Voltage
- Active Bus Termination (SSTL-2, SSTL-3)

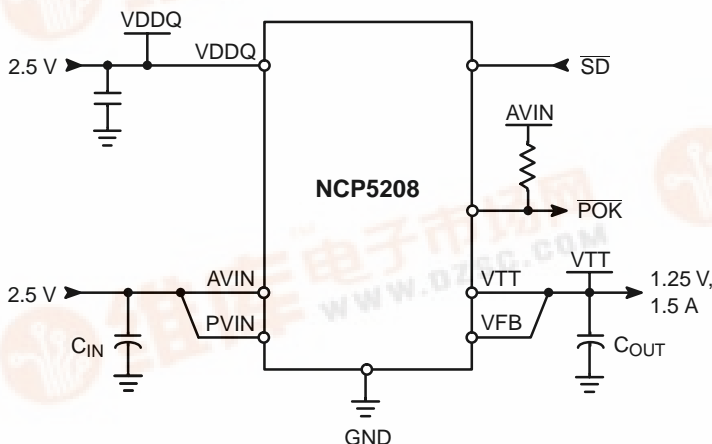


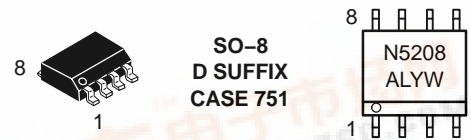
Figure 1. Typical Application Circuit



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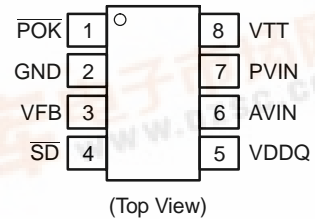
<http://onsemi.com>

### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

### PIN CONNECTIONS



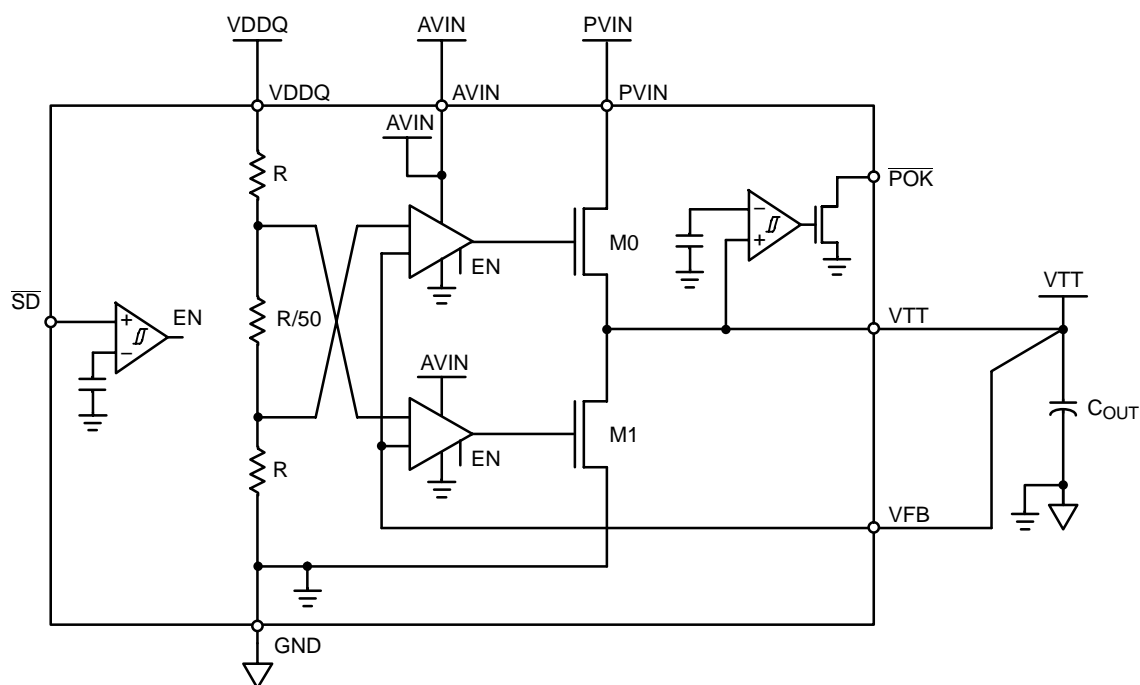
### ORDERING INFORMATION

| Device     | Package | Shipping†        |
|------------|---------|------------------|
| NCP5208DR2 | SO-8    | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



## NCP5208



**Figure 2. Simplified Functional Block Diagram**

### PIN FUNCTION DESCRIPTION

| Pin | Symbol                  | Description   |
|-----|-------------------------|---|
| 1   | $\overline{\text{POK}}$ | Open-drain VTT Power OK output  |
| 2   | GND                     | Ground  |
| 3   | VFB                     | Remote sensing Feedback pin for regulating VTT                                      |
| 4   | $\overline{\text{SD}}$  | Active low shutdown pin to tri-state VTT output, this pin is pulled high internally |
| 5   | VDDQ                    | Reference input for VTT regulator   |
| 6   | AVIN                    | Analog supply input, this powers all the internal control circuitry                 |
| 7   | PVIN                    | Power supply input, this provides the rail voltage for the VTT output               |
| 8   | VTT                     | Termination Regulator output  |

### MAXIMUM RATINGS

| Rating   | Symbol                   | Value            | Unit |
|--|--------------------------|------------------|------|
| AVIN, PVIN, VDDQ, VFB, VTT to GND  | –                        | –0.3, 6.0        | V    |
| Input/Output Pins  | $\overline{\text{SD}}$   | $V_{\text{IO}}$  | V    |
| Open Drain Output Pins   | POK                      | $V_{\text{POK}}$ | V    |
| Thermal Characteristics<br>SO–8 Package<br>Thermal Resistance, Junction–to–Air | $R_{\theta\text{JA\_T}}$ | 151              | °C/W |
| Operating Junction Temperature Range   | $T_{\text{J}}$           | –10 to +150      | °C   |
| Operating Ambient Temperature Range  | $T_{\text{A}}$           | 0 to +70         | °C   |
| Storage Temperature Range  | $T_{\text{stg}}$         | –55 to +150      | °C   |

- This device series contains ESD protection and exceeds the following tests:  
Human Body Model (HBM)  $\leq 2.0$  kV per JEDEC standard: JESD22–A114.  
Machine Model (MM)  $\leq 200$  V per JEDEC standard: JESD22–A115.
- Latch-up Current Maximum Rating:  $\pm 150$  mA per JEDEC standard: JESD78.

## NCP5208

**ELECTRICAL CHARACTERISTICS** (AVIN = 2.5 V, PVIN = 2.5 V, VDDQ = 2.5 V, C<sub>OUT</sub> = 220 μF, for typical values T<sub>A</sub> = 25°C, for min/max values T<sub>A</sub> = 0 to 70°C, unless otherwise noted.)

| Characteristic                 | Symbol            | Conditions   | Min      | Typ    | Max     | Unit |
|--------------------------------|-------------------|--|----------|--------|---------|------|
| Analog Supply Input            | AVIN              | –  | 1.7      | –      | 5.5     | V    |
| Power Supply Input             | PVIN              | –  | 1.7      | –      | AVIN    | V    |
| Termination Voltage Output     | VTT               | AVIN = 2.5 V, VDDQ = PVIN = 1.8 V<br>IVTT = –0.6 A to +0.6 A         | 0.870    | 0.900  | 0.930   | V    |
|                                |                   | AVIN = PVIN = VDDQ = 2.5 V<br>IVTT = –1.5 A to 1.5 A                 | 1.215    | 1.250  | 1.285   | V    |
| Load Regulation                | ΔVTT              | VDDQ = 1.8 V, IVTT = 0 to +0.6 A<br>VDDQ = 1.8 V, IVTT = 0 to –0.6 A | –<br>–18 | –<br>– | 15<br>– | mV   |
|                                |                   | VDDQ = 2.5 V, IVTT = 0 to +1.5 A<br>VDDQ = 2.5 V, IVTT = 0 to –1.5 A | –<br>–20 | –<br>– | 20<br>– | mV   |
| Analog Current Consumption     | I <sub>AVIN</sub> | No Load  | –        | –      | 10      | mA   |
| VDDQ Input Impedance           | Z <sub>VDDQ</sub> | –  | –        | 50     | –       | kΩ   |
| VFB Feedback Pin Input Current | I <sub>VFB</sub>  | Note 3   | –        | –      | 20      | nA   |

### SHUTDOWN CONTROL

|                                |                    |                           |      |      |      |    |
|--------------------------------|--------------------|---------------------------|------|------|------|----|
| Shutdown Pin Enable Threshold  | VSD                | –                         | 1.14 | 1.24 | 1.34 | V  |
| Shutdown Pin Hysteresis        | VSD <sub>hys</sub> | –                         | 0.40 | 0.55 | 0.68 | V  |
| Shutdown Pin Input Current     | ISD                | VDDQ = 2.5 V, VSD = 0 V   | –15  | –    | –    | μA |
|                                |                    | VDDQ = 2.5 V, VSD = 2.5 V | –    | –    | 10   |    |
|                                |                    | VDDQ = 2.5 V, VSD = 5.5 V | –    | –    | 12   |    |
| Shutdown Analog Supply Current | I <sub>shut</sub>  | VDDQ = 2.5 V, VSD = 0 V   | –    | –    | 15   | μA |

### VTT POWER OK INDICATOR

|                                    |                      |  |     |                       |     |    |
|------------------------------------|----------------------|--|-----|-----------------------|-----|----|
| VTT Power OK Window Low Threshold  | POKL <sub>th</sub>   | Note 4                                 | –   | VDDQ ×<br>(1/2–0.02)  | –   | V  |
| VTT Power OK Window High Threshold | POKH <sub>th</sub>   | Note 4                                 | –   | VDDQ ×<br>(1/2+ 0.02) | –   | V  |
| POK Pull–LOW Resistance            | R <sub>POKL</sub>    | I <sub>POK</sub> = 5.0 mA              | 7.0 | –                     | 20  | Ω  |
| POK Leakage Current                | I <sub>POKleak</sub> | VDDQ = 2.5 V, V <sub>POK</sub> = 6.0 V | –   | –                     | 0.1 | μA |

### OVER CURRENT PROTECTION

|                      |                     |   |      |      |       |   |
|----------------------|---------------------|---|------|------|-------|---|
| Source Current Limit | I <sub>LIMsrc</sub> | – | 1.65 | 2.1  | 2.9   | A |
| Sink Current Limit   | I <sub>LIMsnk</sub> | – | –2.9 | –2.0 | –1.65 | A |

### OVER TEMPERATURE PROTECTION

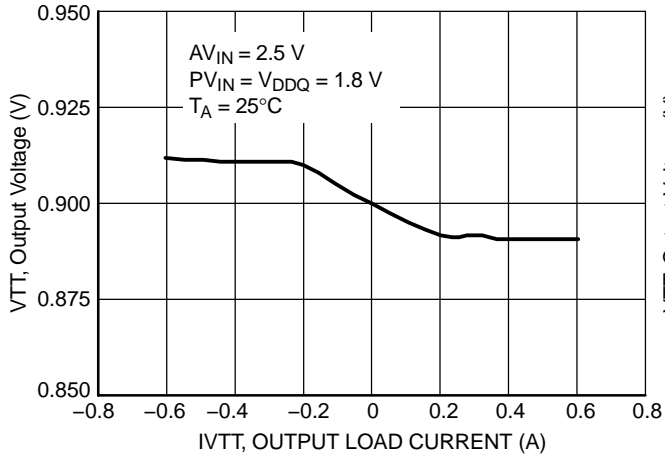
|                              |                    |        |     |     |     |    |
|------------------------------|--------------------|--------|-----|-----|-----|----|
| Thermal Shutdown Temperature | TSD                | Note 3 | 120 | 135 | 150 | °C |
| Thermal Shutdown Hysteresis  | TSD <sub>hys</sub> | Note 3 | –   | 30  | –   | °C |

3. Values are not tested in production, guaranteed by design only.

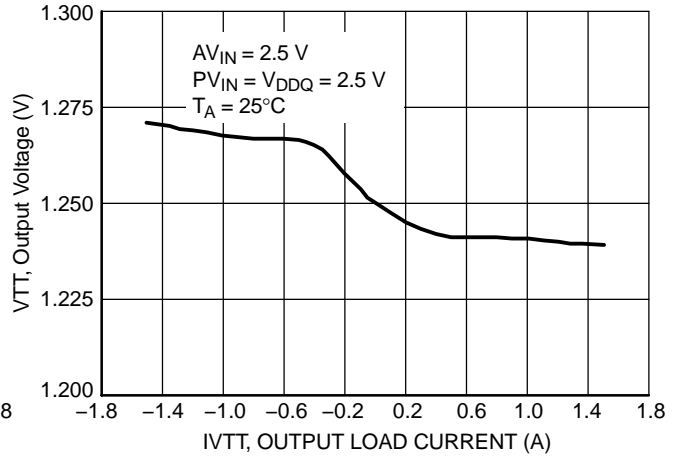
4. Production test performed for AVIN = PVIN = VDDQ = 2.5 V only, 1.8 V performance guaranteed by design.

# NCP5208

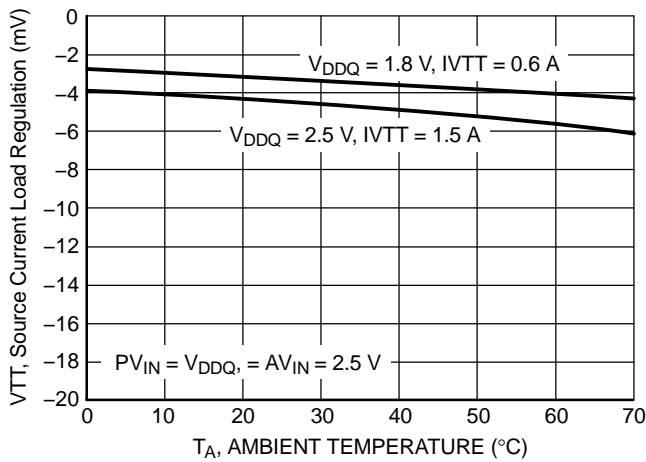
## TYPICAL OPERATING CHARACTERISTICS



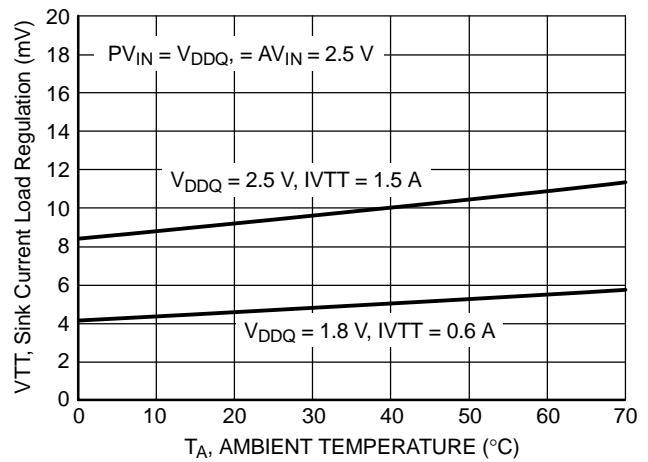
**Figure 3. VTT Output Voltage vs. Load Current ( $V_{DDQ} = 1.8\text{ V}$ )**



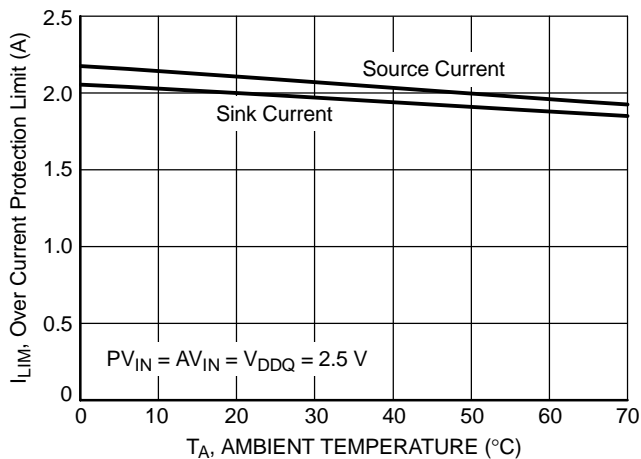
**Figure 4. VTT Output Voltage vs. Load Current ( $V_{DDQ} = 2.5\text{ V}$ )**



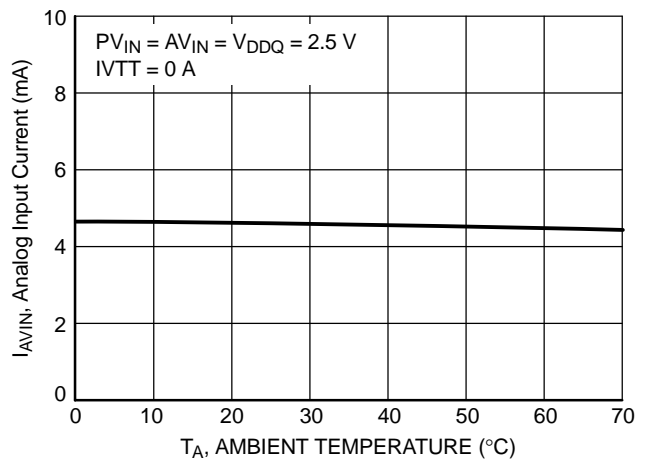
**Figure 5. Source Current Load Regulation vs. Ambient Temperature**



**Figure 6. Sink Current Load Regulation vs. Ambient Temperature**



**Figure 7. Over Current Protection Limit vs. Ambient Temperature**



**Figure 8. Analog Input Current vs. Ambient Temperature**

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## TYPICAL OPERATING CHARACTERISTICS

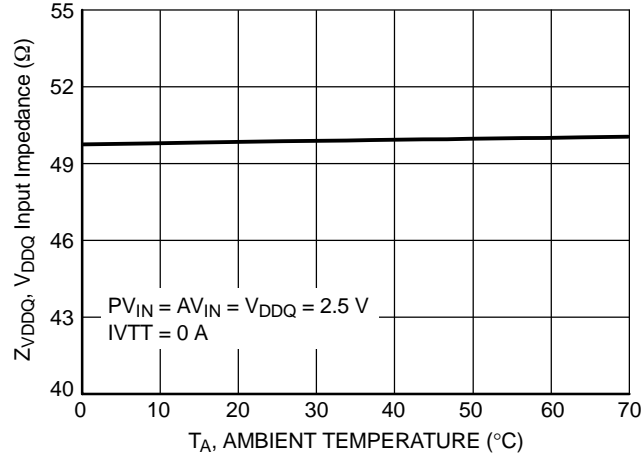


Figure 9.  $V_{DDQ}$  Input Impedance vs. Ambient Temperature

## TYPICAL OPERATING WAVEFORMS

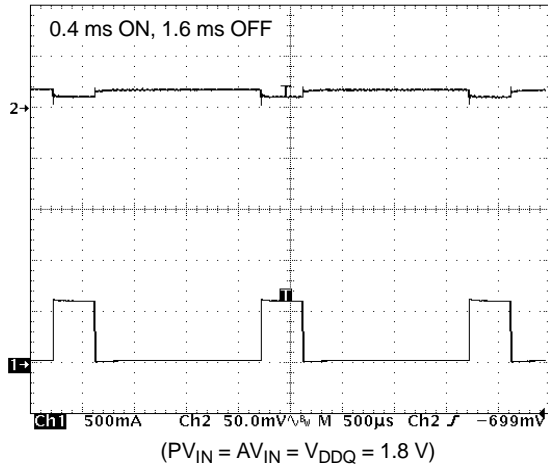


Figure 10. VTT Current Source Transient

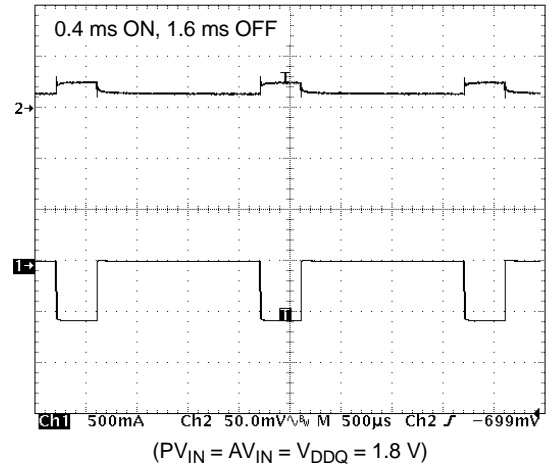


Figure 11. VTT Current Sink Transient

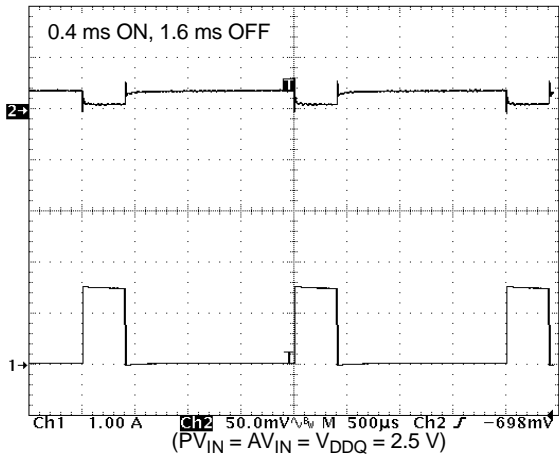


Figure 12. VTT Current Source Transient

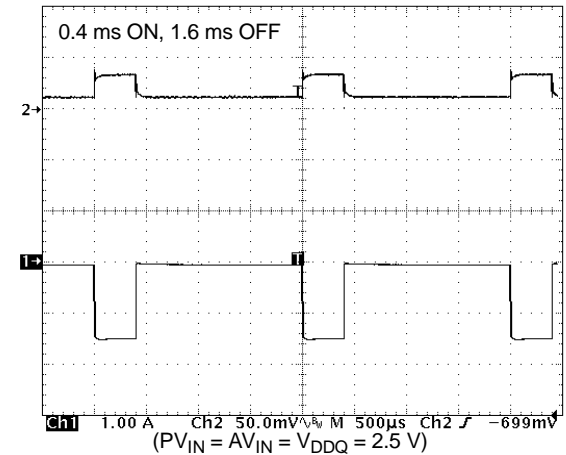
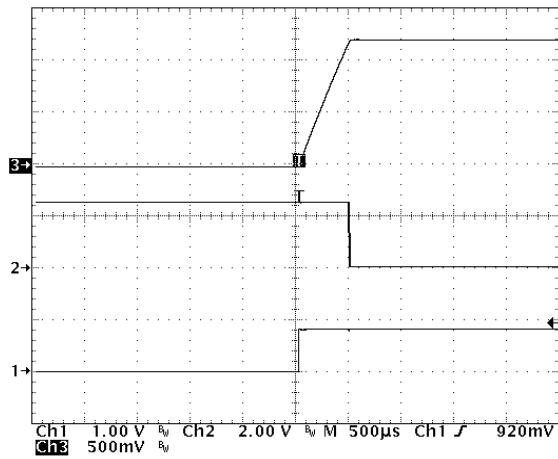


Figure 13. VTT Current Sink Transient

# NCP5208

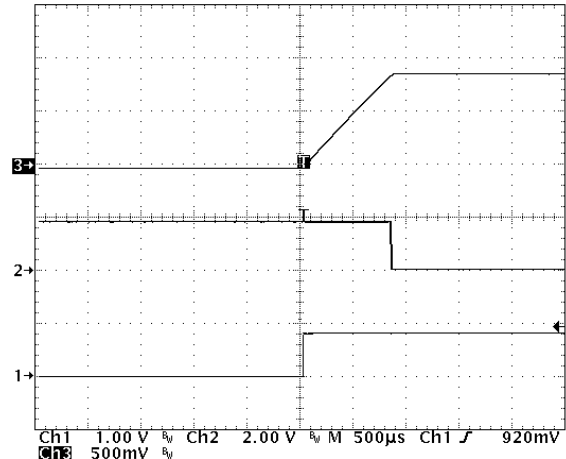
## TYPICAL OPERATING WAVEFORMS



( $PV_{IN} = AV_{IN} = V_{DDQ} = 2.5\text{ V}$ ,  $IV_{TT} = 0\text{ A}$ )

Upper Trace: VTT Output Waveform, 500 mV/Division  
Middle Trace: VTT Power OK Output, 2 V/Division  
Lower Trace: Shut-down Signal, 1 V/Division  
Time Scale: 500  $\mu\text{s}$ /Division

**Figure 14. VTT Start-up Waveform ( $V_{DDQ} = 2.5\text{ V}$ )**



( $PV_{IN} = AV_{IN} = V_{DDQ} = 1.8\text{ V}$ ,  $IV_{TT} = 0\text{ A}$ )

Upper Trace: VTT Output Waveform, 500 mV/Division  
Middle Trace: VTT Power OK Output, 2 V/Division  
Lower Trace: Shut-down Signal, 1 V/Division  
Time Scale: 500  $\mu\text{s}$ /Division

**Figure 15. VTT Start-up Waveform ( $V_{DDQ} = 1.8\text{ V}$ )**

# NCP5208

## DETAILED OPERATING DESCRIPTIONS

### General

The NCP5208 is a linear regulator with both sink and source current capabilities used for active termination of fast switching logic, DDR-I/II SDRAM terminations and active buses termination of SSTL-2/3 logic. This device can be operated from a single supply voltage as low as 1.7 V. For DDR-I applications, the device is capable of sourcing and sinking current up to 1.5 A with output voltage regulated to within  $\pm 3\%$ . The separate voltage remote feedback pin ensures superior load and line regulation with fast tracking capability.

Protective features include Soft-Start, Source/Sink Current Limits and internal Thermal Shutdown. Additionally, an open-drain VTT OK output signal ( $\overline{\text{POK}}$ ) is provided for system monitoring. The shutdown pin ( $\overline{\text{SD}}$ ) can be used to tri-state the regulator output for Suspend To RAM (STR) state. This device is available in a low profile, space saving SO-8 package.

### Supply Voltage Inputs

For added flexibility, separate input pins are provided for each required supply input. AVIN is the device operating voltage, VDDQ is used to generate the internal reference for VTT output voltage control and PVIN is the power rail for the linear regulator. The device will regulate the output voltage, VTT, with respect to the internal voltage reference generated from VDDQ input and track the VDDQ changes closely. The separate PVIN pin allows the designer to isolate the high current PVIN line changes from coupling into the noise sensitive AVIN and VDDQ inputs. Since the AVIN supplies the control to the output power MOSFETs, PVIN should always be lower than or equal to AVIN.

### Generation of Internal Reference Voltage

The prime function of a termination regulator is to provide a termination voltage, VTT at its output, which can track the mid-point of the logic voltage level closely, i.e.  $\frac{1}{2}(\text{VDDQ})$ . The VTT voltage is used to terminate the bus resistors. The NCP5208 generates a precise reference voltage internally with a built in dead-band to avoid upper and lower MOSFET shoot through.

### Remote Voltage Feedback Sensing

The NCP5208 has a separate feedback pin to monitor the output voltage at the remote point. With this capability, the output voltage can be controlled precisely at the output capacitor so that any noise and fluctuations along the power path can be eliminated.

### Termination Voltage Output Regulation

The NCP5208 includes a simple linear series regulator with a pair of control error amplifiers, which takes care of the current source and sink operations separately. The error amplifiers control a pair of MOSFETs to maintain the output voltage equal to the internal reference voltage for both current sink and source conditions. In order to avoid the MOSFETs turning on at the same time, a dead-band is implemented internally for safe operation.

### Regulator Shutdown Function

The operation of the NCP5208 can be suspended by pulling the Shutdown ( $\overline{\text{SD}}$ ) pin to ground. When the device is stopped, the regulator output will be tri-stated for Suspend To RAM (STR) state in PC applications. The shutdown pin is internally pulled high by a small current source, if this feature is not used, this pin can be left open.

### VTT Power OK for System Monitoring

NCP5208 provides an additional VTT power OK signal for system monitoring. The VTT Power OK ( $\overline{\text{POK}}$ ) pin goes low when the VTT voltage is in regulation and has settled within the allowed window. For memory termination applications, the system can check this pin to ensure the termination voltage quality before accessing the memory. The  $\overline{\text{POK}}$  output is connected to a open-drain switching FET and the designer is free to pull this pin to any logic voltage level externally. When the VTT output is in regulation, the internal FET is turned on and pulls the power OK pin to ground.

### Over-current Protection for Sink and Source Operation

In order to provide protection for the internal power MOSFETs, bi-directional current limit protection circuits are implemented. Current limit levels are internally set at 2.1 A typical for current source and 2.0 A typical for current sink at 2.5 V operation.

### Thermal Shutdown with Hysteresis

To guarantee safe operation, NCP5208 provides on-chip thermal shutdown protection. When the chip junction temperature exceeds 135°C typical, the part will shutdown. When the junction temperature falls back to 105°C typical, the device resumes normal operation.

# NCP5208

## APPLICATIONS INFORMATION

### Typical Application Circuit

The NCP5208 is a highly integrated termination regulator. For most applications, an input and output capacitor and a pull-up resistor for the power OK output, are the only external components needed. For typical application circuit, refer to Figure 1.

### AVIN and VDDQ Supply

AVIN provides power for the device to operate. This voltage must be kept clean and free from transients. A small capacitor, 1.0  $\mu\text{F}$  is recommended at this input to provide the required supply filtering and ripple rejection. VDDQ is primarily used to generate the internal voltage reference, so any noise or transient at this pin will be directly reflected at the VTT output. In order to avoid undesired interference injected into this pin, appropriate de-coupling and careful design of PCB layout is required.

### Input Capacitor Selection

The NCP5208 does not require an input capacitor for stability, however it is still recommended for better overall performance during large load transients that can cause sudden drop of the power rail voltage. The input capacitor must be located as close as possible to the PVIN pin to avoid a transient voltage dip affecting the quality of AVIN and VDDQ. For typical DDR-I applications, a low ESR electrolytic capacitor of 100  $\mu\text{F}$  or larger is recommended. By adding a small ceramic capacitor of 0.1  $\mu\text{F}$  in parallel, the best high frequency transient filtering will result. If the device is located near the main supply bulk capacitors, the input capacitance can be reduced accordingly.

### Output Capacitor Selection

The NCP5208 is internally compensated and stable for any output capacitor with capacitance greater than 220  $\mu\text{F}$  and with ESR ranging from 2 m $\Omega$  to 400 m $\Omega$ . The choice for this output capacitor is determined solely by the application and the requirements for load transient characteristic of VTT output. As a general recommendation, the capacitance should be larger than 220  $\mu\text{F}$  with low ESR for SSTL and DDR memory applications.

### Thermal Dissipation

The NCP5208 is a linear regulator, any current flow from/to VTT will result in internal power dissipation and generating heat. In order to prevent un-wanted shutdown of the device during operation, care should be taken to de-rate the power capability according to the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise,  $T_{R-MAX}$  can be calculated from the equation in below:

$$T_{R-MAX} = T_{J-MAX} - T_{A-MAX}$$

Where  $T_{J-MAX}$  is the maximum allowable junction temperature and  $T_{A-MAX}$  is the maximum expected ambient temperature.

The maximum allowable power dissipation for a specific condition is given by:

$$P_{D-MAX} = \frac{T_{R-MAX}}{R_{\theta JA\_T}}$$

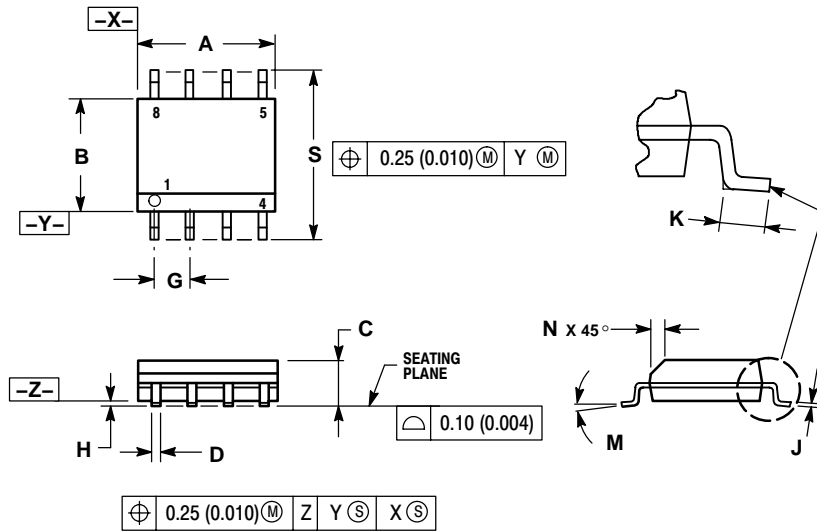
Where  $P_{D-MAX}$  is the maximum allowable power dissipation and  $R_{\theta JA\_T}$  is Junction-to-Air thermal resistance for specific package.

The thermal handling capability depends on several variables. Increasing the thickness and area of the copper and adding vias and airflow can improve the thermal performance.

# NCP5208

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
CASE 751-07  
ISSUE AA




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0° - 8°     |      | 0° - 8°   |       |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

# NCP5208

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