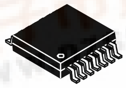
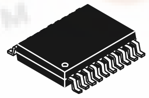
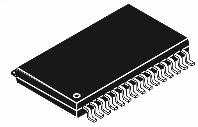




PC CARD POWER-INTERFACE SWITCH FOR PCMCIA CONTROLLERS

FEATURES

- Fully Integrated V_{CC} and V_{PP}/V_{CORE} Switching
- Meets PC Card Standards
- V_{PP}/V_{CORE} Output Programmed Independent of V_{CC}
- TTL-Logic Compatible Inputs
- Short Circuit and Thermal Protection
- 20-Pin HTSSOP or 30-Pin SSOP (Dual With Serial Interface) Package
- 14-pin HTSSOP Package (Single With Parallel Interface)
- 95 µA Typ Quiescent Current on 3.3 VIN Input (Dual With Serial Interface)
- 64 µA Typ Quiescent Current on 3.3 VIN Input (Single With Parallel Interface)
- Break-Before-Make Switching
- Power On Reset
- –40°C to 85°C Ambient Operating Temperature Range

APPLICATIONS

- Notebook/Desktop Computers
- Personal Digital Assistants (PDAs)
- Digital Cameras
- Bar-code Scanners

DESCRIPTION

The TPS2228 and TPS2221 PC card power interface switches provide an integrated power management solution for both dual and single PC card sockets. The TPS2228 is a dual-slot power interface switch for serial PCMCIA controllers. The TPS2221 is a single-slot power interface switch for parallel PCMCIA controllers. These power interface switches support the distribution of 3.3 V, 5 V and 1.8 V to the PC card slot while providing current-limiting protection with overcurrent reporting.

ORDERING INFORMATION(1)

T_A	PACKAGED DEVICES	
	DUAL HTSSOP, SSOP	SINGLE HTSSOP
–40°C to 85°C	TPS2228PWP (20)	TPS2221PWP (14)
	TPS2228DB (30)	

(1) Both DB and PWP packages are available taped and reeled (indicated by the R suffix on the device type; e.g., TPS2228PWPR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS2228, TPS2221
Input voltage range for card power	$V_{I(3.3VIN)}$	–0.3 V to 6 V
	$V_{I(5VIN)}$	–0.3 V to 6 V
	$V_{I(1.8VIN)}$	–0.3 V to 6 V
Logic input/output voltage		–0.3 V to 6 V
Output voltage range	$V_{O(XVCC)}$	–0.3 V to 6 V
	$V_{O(XVPP/VCORE)}$	–0.3 V to 6 V
Continuous total power dissipation		See Dissipation Rating Table
Output current	$I_{O(XVCC)}$	Internally Limited
	$I_{O(XVPP/VCORE)}$	
Operating virtual junction temperature range, T_J		–40°C to 100°C
Storage temperature range, T_{stg}		–55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
$\overline{OC}$ sink current		10 mA

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE (THERMAL RESISTANCE = °C/W)(1)

PACKAGE(2)	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le$ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
20-PWP	30.67 mW/°C	2300 mW	920.25 mW	460.12 mW
14-PWP	26.67 mW/°C	2000 mW	800 mW	400 mW
DB-30	10.95 mW/°C	821.47 mW	328.59 mW	164.3 mW

(1) Reference *Calculating Junction Temperature* in the application information section of this data sheet.
(2) These devices are mounted on an JEDEC low-k board (2 oz. traces on surface) (Based on the maximum recommended junction temperature of 100°C)

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage, V_I 3.3VIN is required for all circuit operations. 5VIN and 1.8VIN are only required for their respective functions.	$V_{I(3.3VIN)}$	3.0	3.6	V
	$V_{I(5VIN)}$	2.7	5.5	V
	$V_{I(1.8VIN)}$	1.7	1.9	V
Output current	$I_{O(XVCC)}$ at T_J =100°C		1	A
	$I_{O(XVPP/VCORE)}$ when switched to 5VIN at T_J =100°C		100	mA
	$I_{O(XVPP/VCORE)}$ when switched to 3.3VIN or 1.8VIN at T_J =100°C		500	mA
Clock frequency			2.5	MHz
Pulse duration	Data	200		ns
	Latch	250		ns
	Clock	100		ns
	Reset	100		ns
Data to clock hold time (Figure 2)		100		ns
Data to clock setup time (Figure 2)		100		ns
Latch delay time (Figure 2)		100		ns
Clock delay time (Figure 2)		250		ns
Operating virtual junction temperature, T_J (maximum to be calculated at worst case PD at 85°C ambient)		–40	100	°C

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 100°C, $V_{I(5VIN)}$ = 5 V, $V_{I(3.3VIN)}$ = 3.3 V, $V_{I(1.8VIN)}$ = 1.8 V, all outputs unloaded (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
Switch resistance	3.3VIN to XVCC with two switches on for dual		T_J = 25°C, I = 750 mA each		72	95	mΩ
			T_J = 100°C, I = 750 mA each			120	
	5VIN to XVCC with two switches on for dual		T_J = 25°C, I = 500 mA each		97	125	mΩ
			T_J = 100°C, I = 500 mA each			160	
	1.8VIN to XVPP/VCORE with two switches on for dual		T_J = 25°C, I = 375 mA each		69	95	mΩ
			T_J = 100°C, I = 375 mA each			120	
	3.3VIN to XVPP/VCORE with two switches on for dual		T_J = 25°C, I = 250 mA each		196	260	mΩ
			T_J = 100°C, I = 250 mA each			325	
	5VIN to XVPP/VCORE with two switches on for dual		T_J = 25°C, I = 100 mA each		0.9	1.3	Ω
			T_J = 100°C, I = 100 mA each			1.6	
$R_{O(XVCC)}$ discharge resistance			Idischarge = 1 mA	0.1		0.5	kΩ
$R_{O(XVPP/VCORE)}$ discharge resistance			Idischarge = 1 mA	0.1		0.5	kΩ
I_{OS} Short-circuit output current(1)	$I_{O(XVCC)}$ 3.3VIN or 5VIN to XVCC	Limit (limit is the steady state value.)	T_J at 25°C, output powered into a short	1	1.5		A
			T_J [–40, 100°C], output powered into a short	1		2.5	
	$I_{O(XVPP/VCORE)}$ 5VIN to XVPP/VCORE	Limit	T_J at 25°C, output powered into a short	120	175		mA
			T_J [–40, 100°C], output powered into a short	120		300	
	$I_{O(XVPP/VCORE)}$ 1.8VIN or 3.3VIN to XVPP/VCORE	Limit	T_J at 25°C, output powered into a short	500	680		mA
		Limit	T_J [–40, 100°C], output powered into a short	500		1250	
Thermal shutdown	Trip point, T_J		Rising temperature, not in overcurrent condition	155	165		°C
			Overcurrent condition	120	130		
	Hysteresis				10		
Current limit response time(2)(3)			$V_{O(xVCC)}$ = 5 V, 100 mΩ short to GND, T_J = 25°C		10		µs
			$V_{O(xVCC)}$ = 3.3 V, 100 mΩ short to GND, T_J = 25°C		20		
			$V_{O(xVPP/VCORE)}$ = 5 V, 100 mΩ short to GND, T_J = 25°C		2		
			$V_{O(xVPP/VCORE)}$ = 3.3 V, 100 mΩ short to GND T_J = 25°C		35		
			$V_{O(xVPP/VCORE)}$ = 1.8 V, 100 mΩ short to GND, T_J = 25°C		250		
I_i Input Quiescent current	Normal operation of TPS2228	$I_{I(3.3VIN)}$	$V_{O(xVCC)} = V_{O(xVPP/VCORE)} = V_{I(3.3VIN)}$, Output pins are floated		95	140	µA
		$I_{I(5VIN)}$			5	10	
		$I_{I(1.8VIN)}$				5	
	Normal operation of TPS2221	$I_{I(3.3VIN)}$	$V_{O(xVCC)} = V_{O(xVPP/VCORE)} = V_{I(3.3VIN)}$, Output pins are floated		64	100	µA
		$I_{I(5VIN)}$			5	10	
		$I_{I(1.8VIN)}$				5	
	Shutdown mode (based on control data)	$I_{I(3.3VIN)}$	Output pins are floated			5	µA
	$V_{O(xVCC)}$ = Hi-Z	$I_{I(5VIN)}$				5	
	$V_{O(xVPP/VCORE)}$ = Hi-Z	$I_{I(1.8VIN)}$				5	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design, not tested in production.
(3) From application of short to 110% of final current limit.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 100°C, $V_{I(5VIN)}$ = 5 V, $V_{I(3.3VIN)}$ = 3.3 V, $V_{I(1.8VIN)}$ = 1.8 V, all outputs unloaded (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH (continued)						
Forward leakage current I_{lkg_FWD} (current measured from output pins to ground)	$I_{O(xVCC)}$	All switches are in Hi-Z state xVCC and xVPP/VCORE are grounded		1	10	µA
	$I_{O(xVPP/VCORE)}$			1	10	
Reverse leakage current I_{lkg_RVS} (current measured from output pins going in)	$I_{O(3.3VIN)}$	All switches are in Hi-Z state, 3.3VIN, 5VIN, and 1.8VIN are grounded $V_{O(xVPP/VCORE)} = V_{O(xVCC)}$ = 5 V		1	10	µA
	$I_{O(5VIN)}$			1	10	
	$I_{O(1.8VIN)}$			1	10	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Specified by design, not tested in production.
(3) From application of short to 110% of final current limit.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 100°C, $V_{I(5VIN)}$ = 5 V, $V_{I(3.3VIN)}$ = 3.3 V, $V_{I(1.8VIN)}$ = 1.8 V, all outputs unloaded (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
LOGIC SECTION (CLOCK, DATA, LATCH, RESET, SHDN, OC, VDO, VD1, VD2, VD3)						
Logic input current	I(RESET)(3)	RESET = 5.5 V, sinking or sourcing		0	1	µA
		RESET = 0 V, sourcing	10		30	
	I(SHDN)(3) Or I(SHDN_RST)(3)	SHDN or SHDN_RST = 5.5 V, sinking or sourcing		0	1	
		SHDN or SHDN_RST = 0 V, sourcing	10		30	
	I(LATCH)(1)	LATCH = 5.5 V, sinking			50	
		LATCH = 0 V, sinking or sourcing			1	
	I(CLOCK,DATA, VD0, VD1, VD2, VD3)	0 V to 5.5 V, sinking or sourcing			1	
Logic input high level(4)			2			V
Logic input low level(4)					0.8	
OC output saturation voltage		I_O = 2 mA			0.4	
OC leakage current		$V_{O(OC)}$ = 5.5 V			1	µA
OC deglitch(2)	Falling edge	Falling into overcurrent condition	5		15	mS
	Rising edge	Coming out of overcurrent condition	5		15	

PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
UVLO					
3.3VIN UVLO	3.3VIN level below which all switches are in Hi-Z state	2.2		2.9	V
3.3VIN Hysteresis(2)			0.1		
5VIN UVLO	5VIN level below which only 5VIN switches are in Hi-Z state	2.0		2.6	
5VIN Hysteresis(2)			80		mV
1.8VIN UVLO	1.8VIN level below which only 1.8VIN switches are in Hi-Z state	1.25		1.62	V
1.8VIN Hysteresis(2)			50		mV

(1) Refer to Parameter Measurement Information, Figure 1.
(2) Specified by design, not tested in production.
(3) RESET and SHDN (or SHDN/RST for TPS2221) have low current pullup; LATCH has low current pulldown.
(4) For recommended operating ranges only.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 100°C, $V_{I(5VIN)}$ = 5 V, $V_{I(3.3VIN)}$ = 3.3 V, $V_{I(1.8VIN)}$ = 1.8 V, all outputs unloaded (unless otherwise noted)(1)

PARAMETER(1)		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
t_r Output rise times(2)	5VIN to xVCC	$C_{L(xVCC)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0 A,		0.5		2	ms
	3.3VIN to xVCC			0.5		2	
	1.8VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A		0.5		2	
	3.3VIN to xVPP/VCORE			0.15		1	
	5VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A		0.05		0.14	
	5VIN to xVCC	$C_{L(xVCC)}$= 150 µF, $I_{O(xVCC)}$ = 0.75A		0.75		2.0	
	3.3VIN to xVCC			0.75		2.0	
	1.8VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 150 µF, $I_{O(xVPP/VCORE)}$ = 0.375A		0.50		2.0	
	3.3VIN to xVPP/VCORE			0.50		1.15	
	5VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 10 µF, $I_{O(xVPP/VCORE)}$ = 0.05A		0.15		0.375	
t_f Output fall times(2)	5VIN to xVCC	$C_{L(xVCC)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0 A,		0.25		1.0	ms
	3.3VIN to xVCC			0.35		1.0	
	1.8VIN to xVPP/VCORE	$C_{L(xVCC)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0 A,		0.25		1.0	
	3.3VIN to xVPP/VCORE			0.1		0.5	
	5VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A		0.075		0.15	
	5VIN to xVCC	$C_{L(xVCC)}$ = 150 µF, $I_{O(xVCC)}$ = 0.75A		1.4		2.5	
	3.3VIN to xVCC			1.4		1.7	
	1.8VIN to xVPP/VCORE	$C_{L(xVCC)}$ = 150 µF, $I_{O(xVPP/VCORE)}$ = 0.375 A		1.4		2.0	
	3.3VIN to xVPP/VCORE			2.5		3.1	
	5VIN to xVPP/VCORE	$C_{L(xVPP/VCORE)}$ = 10 µF, $I_{O(xVPP/VCORE)}$ = 0.05 A		1.7		2.1	
t_{pd} Propagation delay(2)	Latch↑ to xVPP/VCORE (1.8 V)	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A	t_{pdon}	0.15		1.4	ms
			t_{pdoff}	2.5		8.6	
	Latch↑ to xVPP/VCORE (3.3 V)	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A	t_{pdon}	0.05		0.5	
			t_{pdoff}	0.5		2.5	
	Latch↑ to xVPP/VCORE (5 V)	$C_{L(xVPP/VCORE)}$ = 0.1 µF, $I_{O(xVPP/VCORE)}$ = 0 A	t_{pdon}	0.02		0.3	
			t_{pdoff}	0.10		0.3	
	Latch↑ to xVCC (5 V)	$C_{L(xVCC)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0 A	t_{pdon}	0.15		0.85	
			t_{pdoff}	1.3		3.7	
	Latch↑ to xVCC (3.3 V)	$C_{L(xVCC)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0 A	t_{pdon}	0.15		1.0	
			t_{pdoff}	1.7		5.3	
t_{pd} Propagation delay(2)	Latch↑ to xVPP/VCORE (1.8 V)	$C_{L(xVPP/VCORE)}$ = 150 µF, $I_{O(xVPP/VCORE)}$ = 0.375 A	t_{pdon}	0.35		1.9	ms
			t_{pdoff}	2.4		8.5	
	Latch↑ to xVPP/VCORE (3.3 V)	$C_{L(xVPP/VCORE)}$ = 150 µF, $I_{O(xVPP/VCORE)}$ = 0.375 A	t_{pdon}	0.2		0.75	
			t_{pdoff}	0.5		2.5	
	Latch↑ to xVPP/VCORE (5 V)	$C_{L(XVPP/VCORE)}$ = 10 µF, $I_{O(xVPP/VCORE)}$ = 0.05 A	t_{pdon}	0.05		0.15	
			t_{pdoff}	0.15		0.35	
	Latch↑ to xVCC (5 V)	$C_{L(XVCC)}$ = 150 µF, $I_{O(xVCC)}$ = 0.75 A	t_{pdon}	0.35		1.2	
			t_{pdoff}	1.3		3.7	
	Latch↑ to xVCC (3.3 V),	$C_{L(XVCC)}$ = 150 µF, $I_{O(xVCC)}$ = 0.75 A	t_{pdon}	0.4		1.4	
			t_{pdoff}	1.5		5.2	

(1) Refer to Parameter Measurement Information, Figure 1.
(2) Specified by design, not tested in production

PARAMETER MEASUREMENT INFORMATION

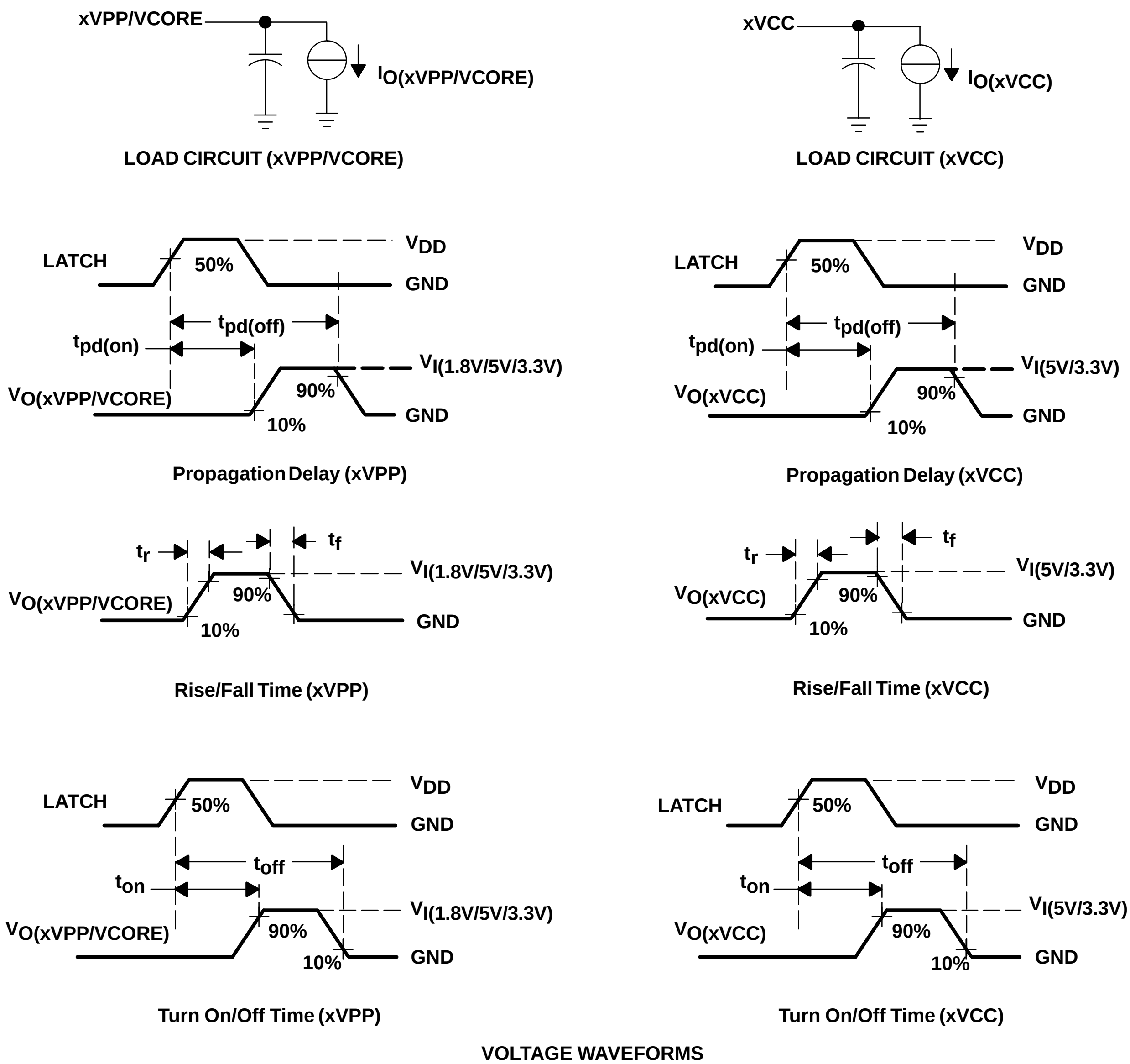
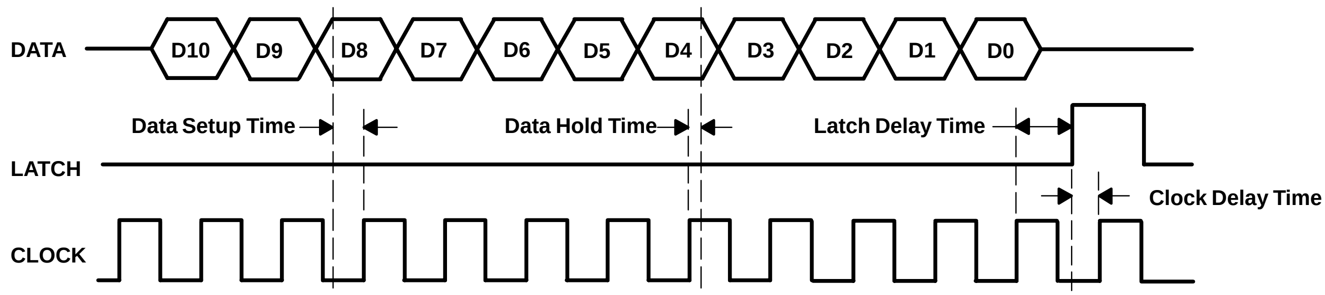


Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for TPS2228/TPS2221 Power Interface Switch

TABLE OF GRAPHS FOR POWER MEASUREMENT INFORMATION

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Short-Circuit Current Limit, 1.8VIN to xVPP/VCORE Switch	vs Junction Temperature	19

PARAMETER MEASUREMENT INFORMATION

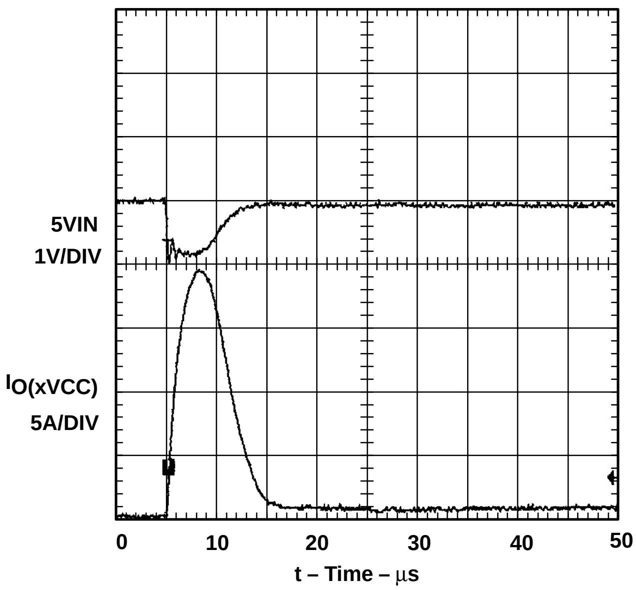


Figure 3. Short-Circuit Response, Short Applied to Powered-on 5VIN-to-xVCC Switch Output

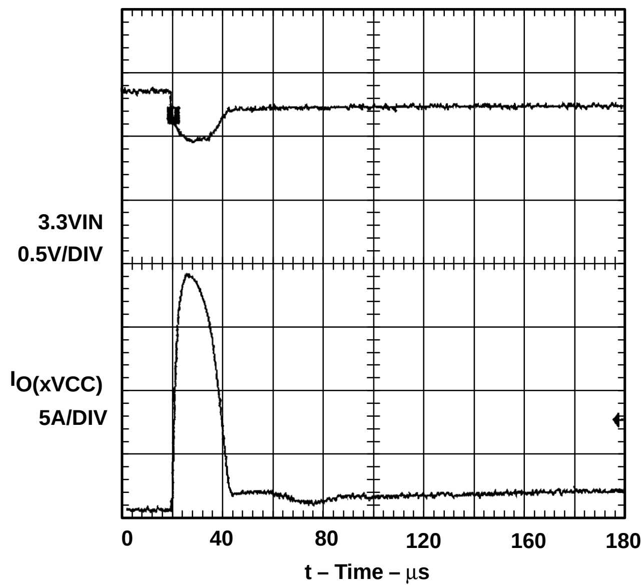


Figure 4. Short-Circuit Response, Short Applied to Powered-on 3.3VIN-to-xVCC-Switch Output

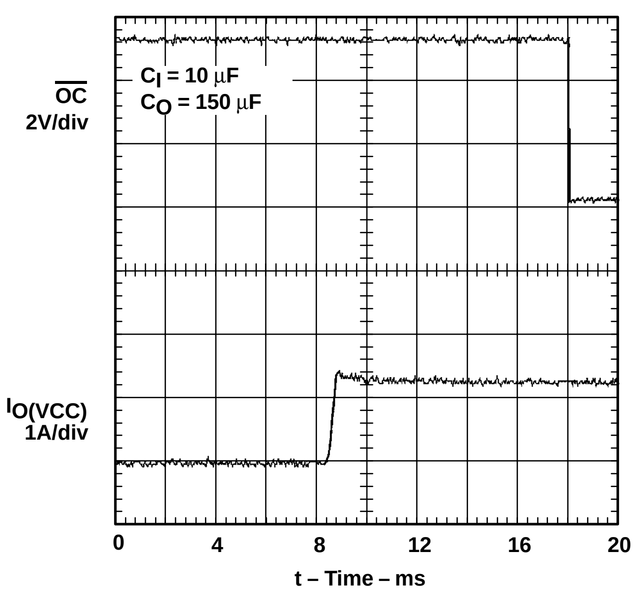


Figure 5. $\overline{OC}$ Response With 5VIN-to-xVCC Switch Output Turned on Into a Short

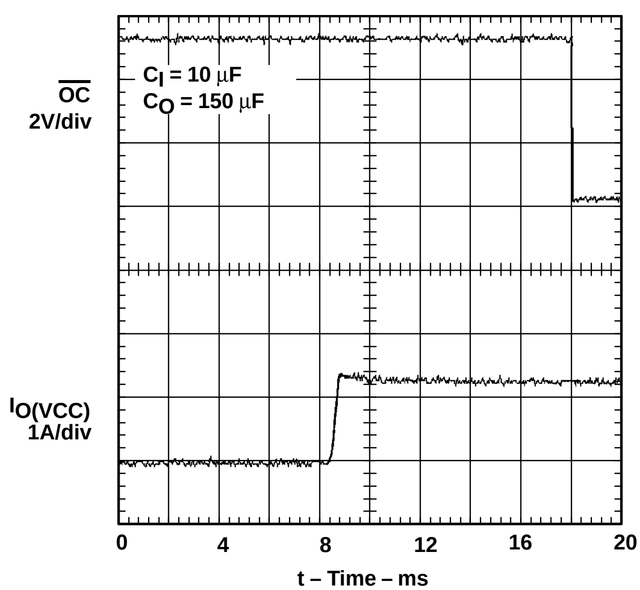


Figure 6. $\overline{OC}$ Response With 3.3VIN-to-xVCC Switch Output Turned on Into a Short

PARAMETER MEASUREMENT INFORMATION

3.3VIN AND 5VIN INPUT CURRENT
vs
JUNCTION TEMPERATURE

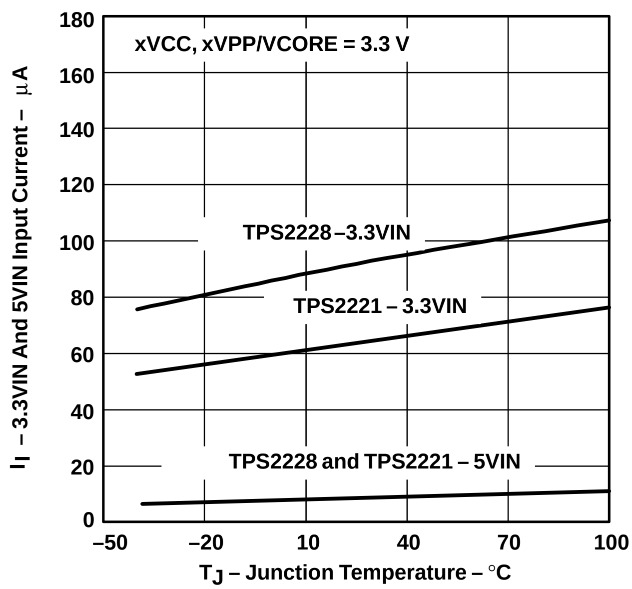


Figure 7

3.3VIN AND 5VIN INPUT CURRENT
vs
JUNCTION TEMPERATURE

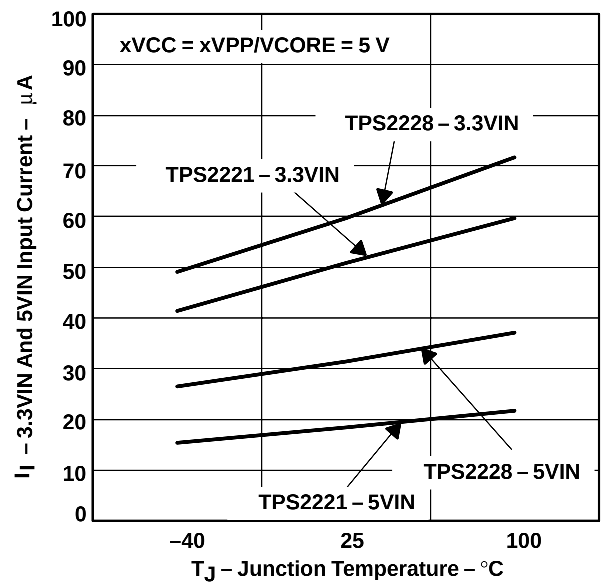


Figure 8

1.8VIN INPUT CURRENT
vs
JUNCTION TEMPERATURE

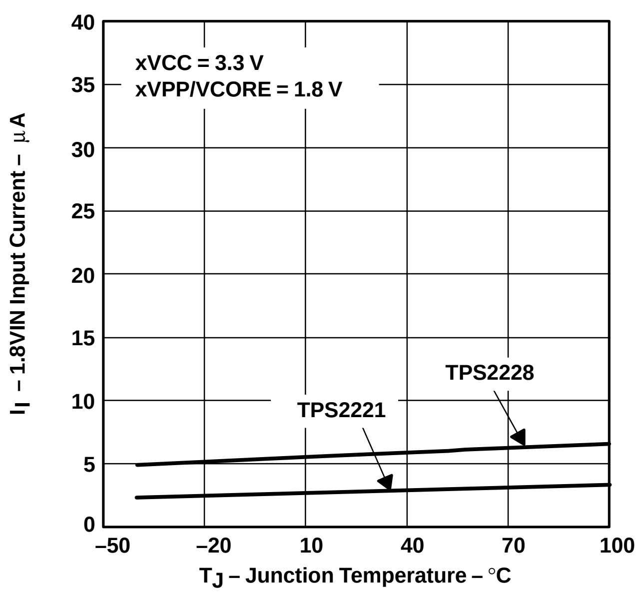


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
(3.3VIN TO xVCC SWITCH)
vs
JUNCTION TEMPERATURE

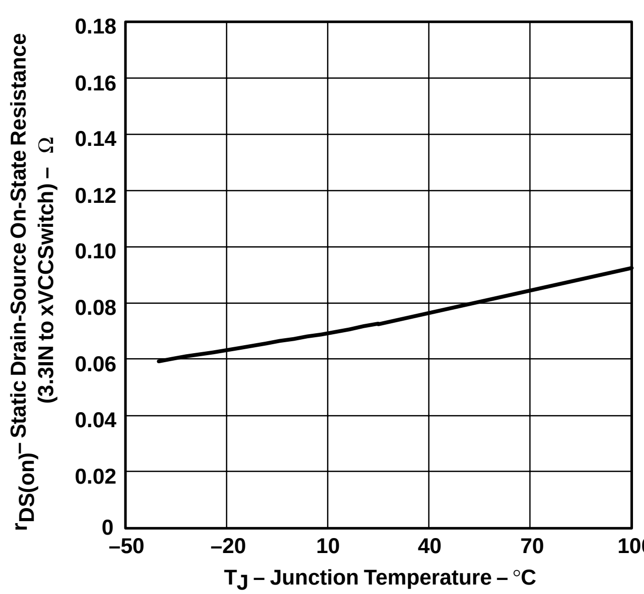


Figure 10

PARAMETER MEASUREMENT INFORMATION

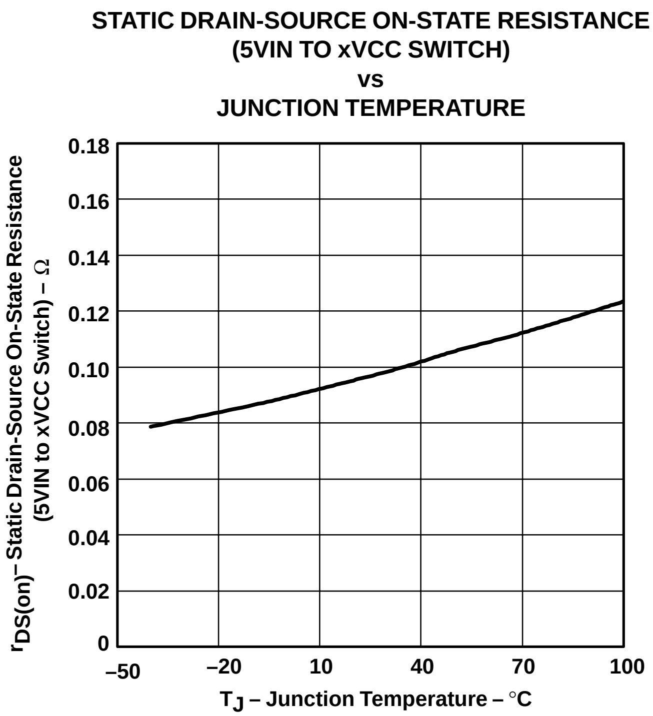


Figure 11

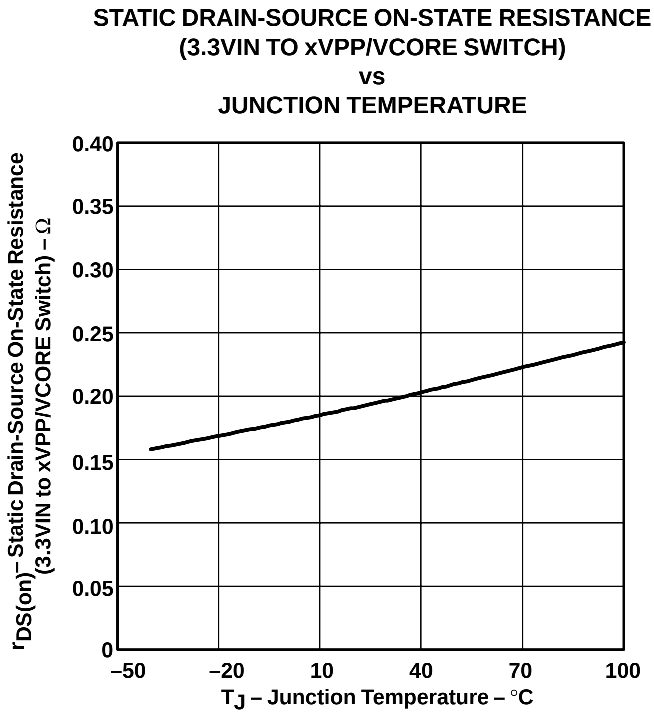


Figure 12

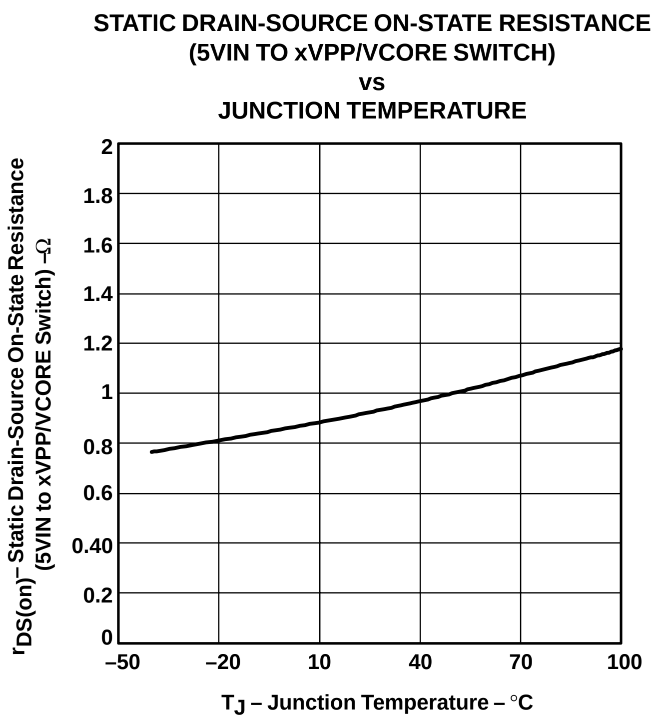


Figure 13

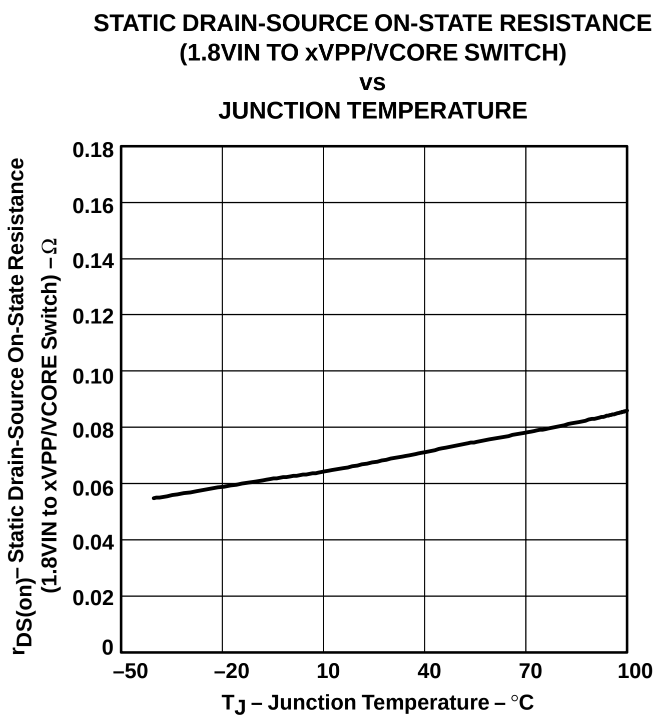


Figure 14

PARAMETER MEASUREMENT INFORMATION

SHORT-CIRCUIT CURRENT LIMIT (3.3VIN TO xVCC) vs JUNCTION TEMPERATURE

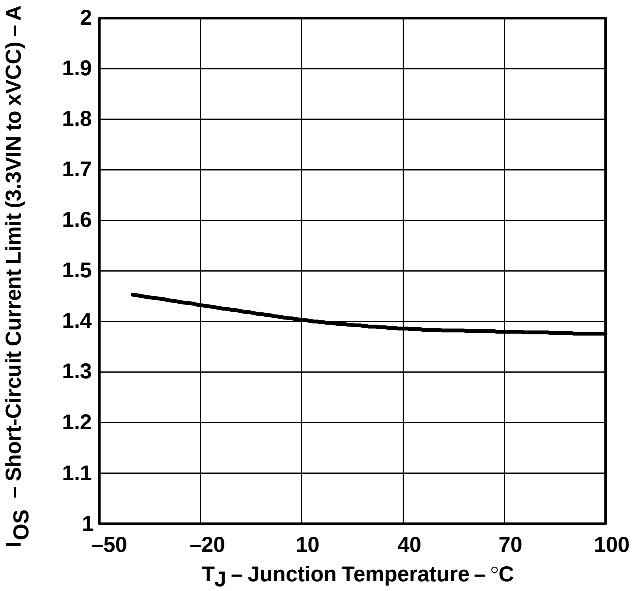


Figure 15

SHORT-CIRCUIT CURRENT LIMIT (5VIN TO xVCC) vs JUNCTION TEMPERATURE

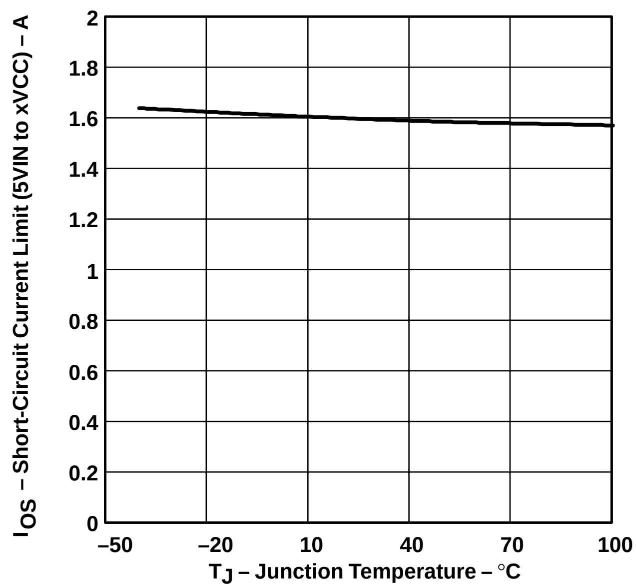


Figure 16

SHORT-CIRCUIT CURRENT LIMIT (3.3VIN TO xVPP/VCORE) vs JUNCTION TEMPERATURE

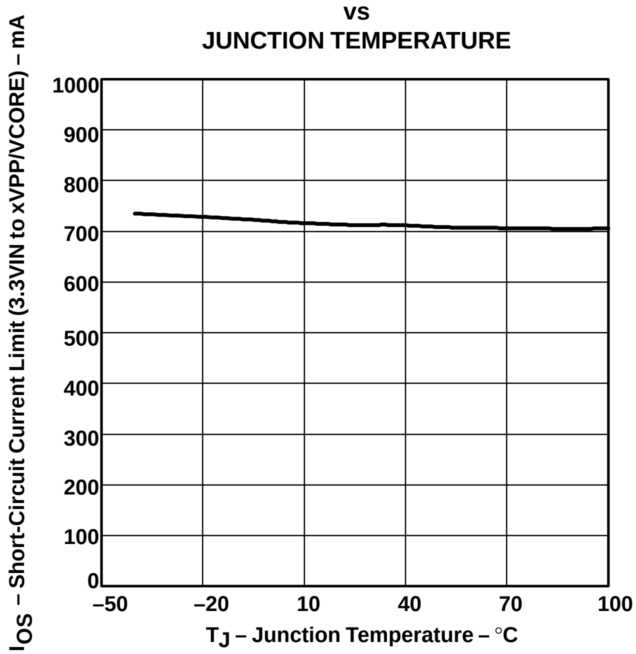


Figure 17

SHORT-CIRCUIT CURRENT LIMIT (5VIN TO xVPP/VCORE) vs JUNCTION TEMPERATURE

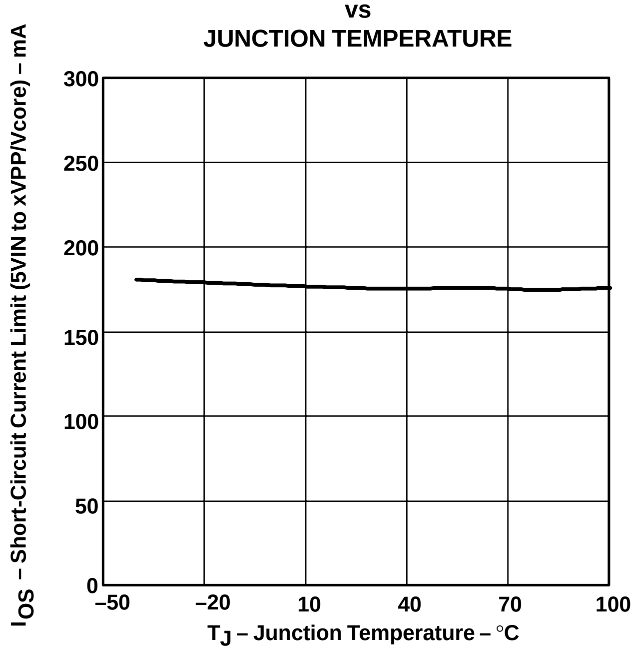


Figure 18

PARAMETER MEASUREMENT INFORMATION

SHORT-CIRCUIT CURRENT LIMIT
(1.8VIN TO xVPP/VCORE)
vs
JUNCTION TEMPERATURE

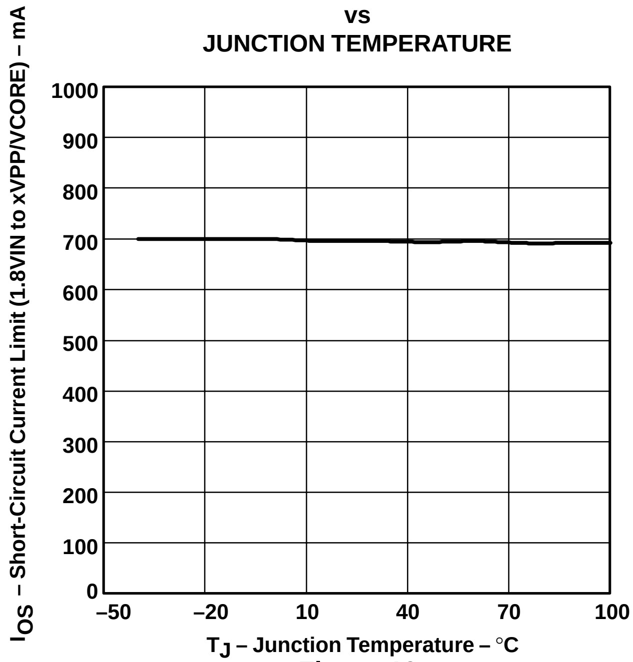
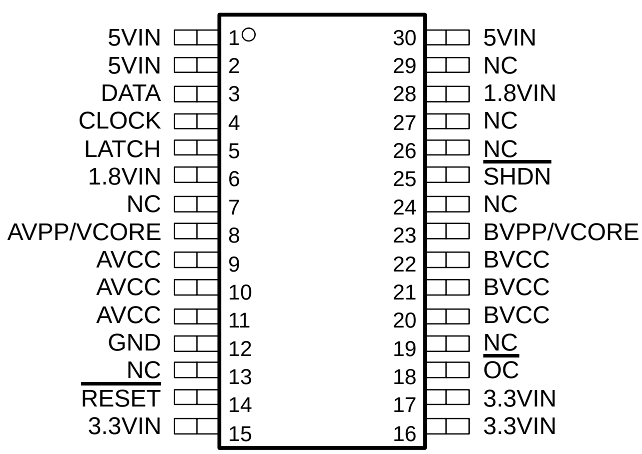


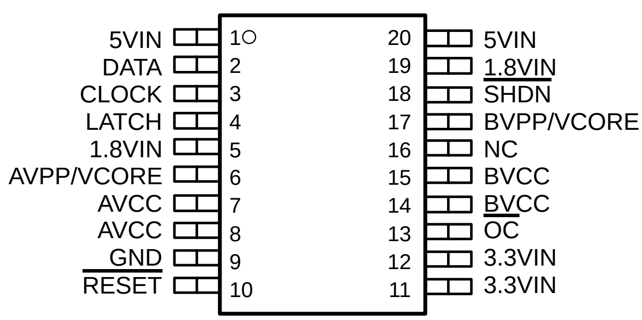
Figure 19

PIN ASSIGNMENTS

TPS2228DB

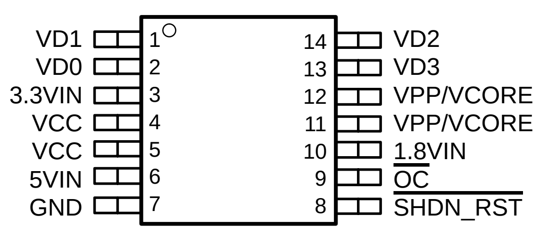


TPS2228PWP



NC – No internal connection

TPS2221PWP



PARAMETER MEASUREMENT INFORMATION

Terminal Functions (Dual-Serial)

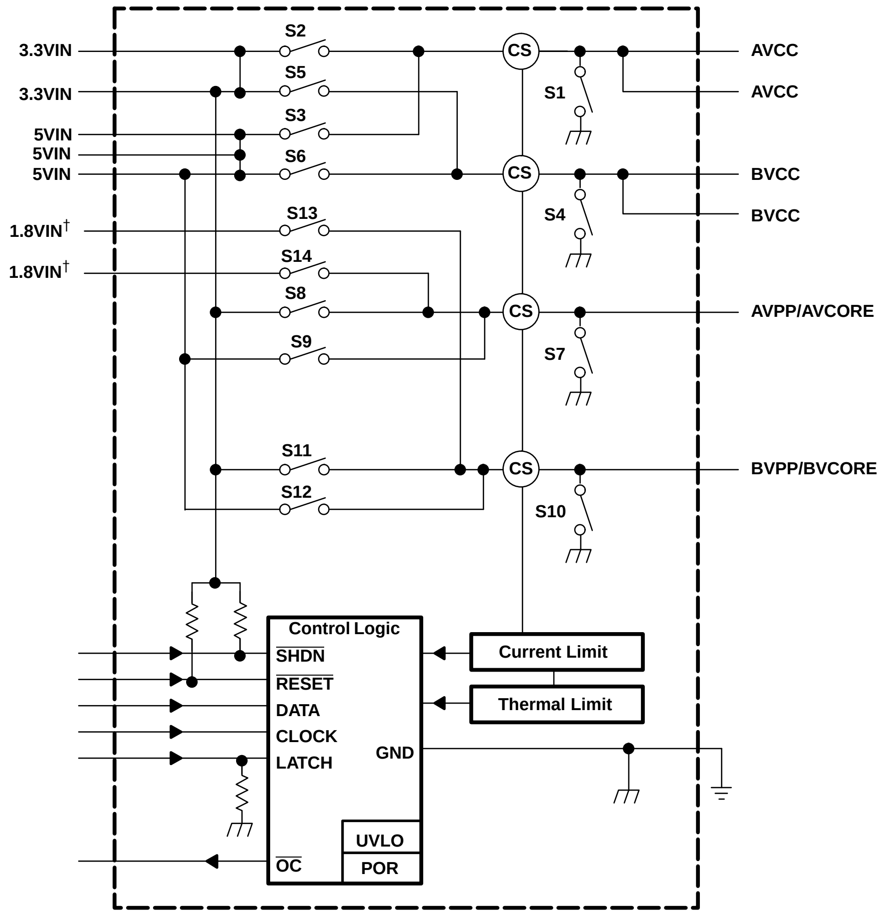
TERMINAL			I/O	DESCRIPTION
NAME	NO. 2228 (DB–30)	NO. 2228 (PWP–20)		
1.8VIN	6, 28	5, 19	I	1.8-V input for card power (xVPP/VCORE). Pins 6 and 28 must be connected together externally.
3.3VIN	15, 16, 17	11, 12	I	3.3-V input for card power (xVCC and xVPP/Vcore) and chip power (3.3VIN must be connected to a voltage source for the device to operate)
5VIN	1, 2, 30	1, 20	I	5-V input for card power (xVCC and xVPP/Vcore)
AVCC	9, 10, 11	7, 8	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
AVPP/VCORE	8	6	O	Switched output that delivers 0 V, 1.8 V, 3.3 V, 5 V, or high impedance to card
BVCC	20, 21, 22	14, 15	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
BVPP/VCORE	23	17	O	Switched output that delivers 0 V, 1.8 V, 3.3 V, 5 V, or high impedance to card
CLOCK	4	3	I	Logic-level clock for serial data word
DATA	3	2	I	Logic-level serial data word
GND	12	9		Ground
LATCH	5	4	I	Logic-level latch for serial data word, an internal pulldown is provided
NC	7,13,19, 24, 26, 27, 29	16		No internal connection
$\overline{OC}$	18	13	O	Open-drain output that is asserted low when an overcurrent condition exists.
$\overline{RESET}$	14	10	I	Logic-level RESET input. Asynchronous command active low. An internal pullup is provided. When active, all line switches are off and all the output discharge switches are on.
$\overline{SHDN}$	25	18	I	Hi-Z (open) all switches. Identical function to serial shutdown with D8=0. Asynchronous command active low. An internal pullup is provided.

Terminal Functions (Single – Parallel)

TERMINAL		I/O	DESCRIPTION
NAME	NO. 2221 (PWP–14)		
1.8VIN	10	I	1.8-V input for card power (VPP/VCORE)
3.3VIN	3	I	3.3-V input for card power (VCC and VPP/Vcore) and chip power (3.3VIN must be connected to a voltage source for the device to operate)
5VIN	6	I	5-V input for card power (VCC and VPP/Vcore)
GND	7		Ground
$\overline{OC}$	9	O	Open-drain output that is asserted low when an overcurrent condition exists.
$\overline{SHDN\_RST}$	8	I	Hi-Z (open) all switches. Identical function to serial shutdown mode by parallel data VD (3:0). Asynchronous command active low. An internal pullup is provided.
VCC	4, 5	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
VD0	2	I	Parallel control signal 0 (see Table 2. TPS2221 Control Logic)
VD1	1	I	Parallel control signal 1 (see Table 2. TPS2221 Control Logic)
VD2	14	I	Parallel control signal 2 (see Table 2. TPS2221 Control Logic)
VD3	13	I	Parallel control signal 3 (see Table 2. TPS2221 Control Logic)
VPP/VCORE	11, 12	O	Switched output that delivers 0 V, 1.8 V, 3.3 V, 5 V, or high impedance to card

FUNCTIONAL BLOCK DIAGRAM

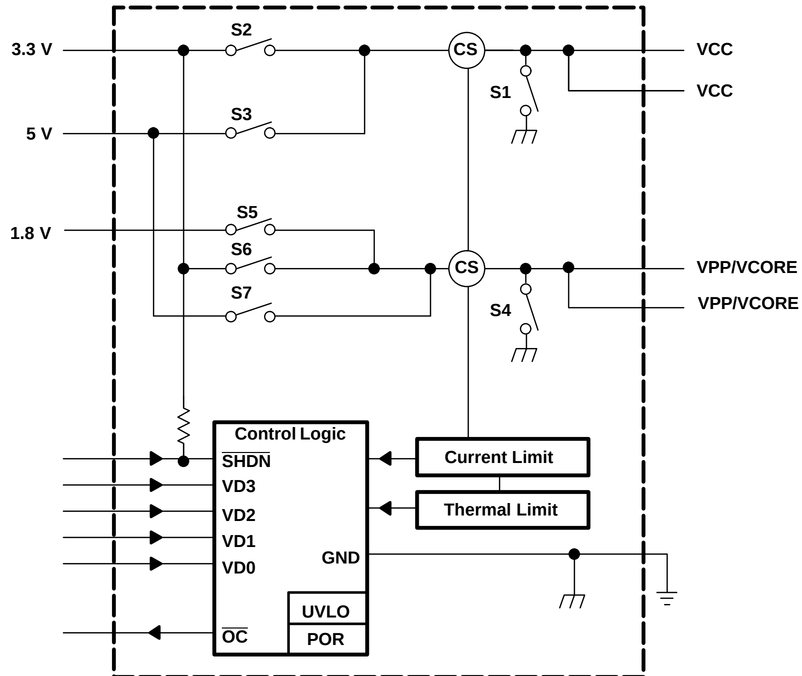
DUAL WITH SERIAL INTERFACE



† The two 1.8VIN pins must be connected together externally

FUNCTIONAL BLOCK DIAGRAM

SINGLE WITH PARALLEL INTERFACE



APPLICATION INFORMATION

OVERVIEW

PC cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. As a result, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, so that cards and hosts from different vendors could communicate with one another transparently.

PC CARD POWER SPECIFICATION

The current PC card standard set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the PC card connector's 68 terminals. This power interface consists of two V_{CC}, two V_{PP}/V_{CORE}, and four ground terminals. Multiple power and ground terminals minimize connector-terminal and line resistance. The two Vpp/ Vcore terminals were originally specified as separate signals, but the host is no longer required to provide separate programmable voltages on each pin. Primary power for the card is supplied through the V_{CC} terminals; flash- memory programming and erase voltage is supplied through the V_{PP}/V_{CORE} terminals. The V_{PP}/V_{CORE} terminals are also intended to be used as a supplemental source of power, such as a core voltage for integrated circuits.

OVERCURRENT AND OVER TEMPERATURE PROTECTION

PC cards are inherently subject to damage caused by mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC card, resulting in the rather sudden and unacceptable loss of system power. The TPS2228/2221 power interface switch is designed to respond quickly to an overcurrent condition to protect the system. During an overcurrent event, the current limit circuit of the TPS2228/2221 generates an internal error signal that linearly limits the output current of the affected output. The propogation delay associated with activating the current-limit circuit has an effect on the amount of current initially delivered to the output. During this time, the input voltage to the switch may droop a small amount. The amount of voltage droop is system dependent. Power supply bulk capacitors play an important role in minimizing this voltage droop.

Overcurrent sensing is applied to each output separately. As a result, only the affected output is current-limited during an overcurrent event. The TPS2228/2221 also has an overcurrent status output ($\overline{OC}$) that is asserted low to provide feedback that an overcurrent condition has occurred.

The TPS2228/2221 has two thermal shutdown circuits. The higher thermal shutdown circuit protects the device from a high junction temperature condition. In the event that the junction temperature exceeds a minimum of 155°C, the higher thermal shutdown circuit turns off all switches to protect the device. Normal switch operation resumes when the junction temperature cools down approximately 10°C.

In the event of an overcurrent condition, the lower thermal shutdown circuit activates when the junction temperature exceeds a minimum of 120°C. On the TPS2221, this lower thermal shutdown circuit disables both the VCC and the V_{PP}/V_{CORE} switches once the junction temperature exceeds the lower thermal trip point. On the TPS2228, only the channel in overcurrent (either AV_{CC} and AV_{PP}/V_{CORE}, or BV_{CC} and BV_{PP}/V_{CORE}) is disabled. For both the TPS2221 and the TPS2228, normal operation of the switches resumes once the junction temperature cools down approximately 10°C. This cycle continues until the overcurrent condition is removed.

VOLTAGE TRANSISTIONING REQUIREMENT

PC cards, like portables, are migrating from 5 V to 3.3 V and even 1.8 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2228/2221 power interface switch is designed to meet all combinations of power delivery as currently defined in the PC card standard. The latest protocol accommodates mixed 3.3 V/ 5 V systems by first powering the card with 5 V, then polling it to determine if it is compatible with 3.3-V power. The PC card standard requires that the capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3 V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The PC card standard requires that V_{CC} be discharged within 100 ms. PC card resistance can not be relied on to provide a discharge path for voltages stored on PC card capacitance because of possible high-impedance isolation by power-management schemes. The TPS2228/2221 power interface switch includes discharge transistors on all V_{CC} and V_{PP}/V_{CORE} outputs to meet the specification requirement.

SHUTDOWN MODE

In the shutdown mode, each of the V_{CC} and V_{PP}/V_{CORE} outputs is forced to a high-impedance state (Hi-Z). In this mode, the chip quiescent current is reduced to conserve battery power.

POWER SUPPLY CONSIDERATIONS

The TPS2228/2221 power interface switch has multiple pins for each of its power inputs and for the switched V_{CC} outputs. The two 1.8VIN pins must be connected together externally. It is recommended that all input and output power pins be parallel connected for optimum operation.

To increase the noise immunity of the TPS2228/2221 power interface switch, the power supply inputs should have a minimum of 1µF electrolytic or tantalum bypass capacitor connected in parallel with a 0.047 µF to 0.1 µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1 µF or larger ceramic capacitor. Doing so improves the immunity of the TPS2228/2221 power interface switch to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2228/2221 power interface switch and the load.

$\overline{\text{RESET}}$

To ensure that cards are in a known state after power brownouts or system initialization, the PC cards should be reset at the same time via the host, by applying low impedance paths from V_{CC} and V_{PP}/V_{CORE} terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC card filter capacitance, permitting the system (host and PC cards) to be powered up concurrently. The active low $\overline{\text{RESET}}$ input will program all outputs to 0 V. The TPS2228 power interface switch remains in the low-impedance output state until the signal is deasserted and new data is received. For the TPS2228, the input serial data cannot be latched during reset mode.

CALCULATING JUNCTION TEMPERATURE

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 10 through 14 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma P_D \times R_{\theta JA}\right) + T_A$$

Where $R_{\theta JA}$ is the inverse of the derating factor in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

LOGIC INPUTS AND OUTPUTS

For the TPS2228, the serial interface consists of DATA, CLOCK, and LATCH signals. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 11-bit (D0–D10) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The serial interface of the TPS2228 power interface switch is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

For the TPS2221, the parallel interface consists of four bits (D3:D0). These four bits must be driven continuously to select the desired voltage outputs based on the input bit pattern. During power up, these inputs can be connected to an external pulldown resistor to ensure that the outputs are at zero volts, especially if the device driving these inputs is in a high impedance state while initializing.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent or over-temperature condition in any of the V_{CC} and V_{PP}/V_{CORE} outputs as previously discussed.

ESD PROTECTION

All TPS2228/2221 power interface switch inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{PP}/V_{CORE} outputs can be exposed to potentially higher discharges from the external environment through the PC card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

Table 1. TPS2228 Power Interface Switch Control Logic

TPS2228 Serial Interface

xVPP/VCORE

	AVPP/VCORE CONTROL SIGNALS			OUTPUT V_AVPP/ VCORE	BVPP/VCORE CONTROL SIGNALS				OUTPUT V_BVPP/ VCORE
D8(SHDN)	D0	D1	D9		D8(SHDN)	D4	D5	D10	
1	0	0	X	0 V	1	0	0	X	0 V
1	0	1	0	3.3 V	1	0	1	0	3.3 V
1	0	1	1	5 V	1	0	1	1	5 V
1	1	0	X	Hi-Z	1	1	0	X	Hi-Z
1	1	1	0	1.8 V	1	1	1	0	1.8 V
1	1	1	1	1.8 V	1	1	1	1	1.8 V
0	X	X	X	Hi-Z	0	X	X	X	Hi-Z

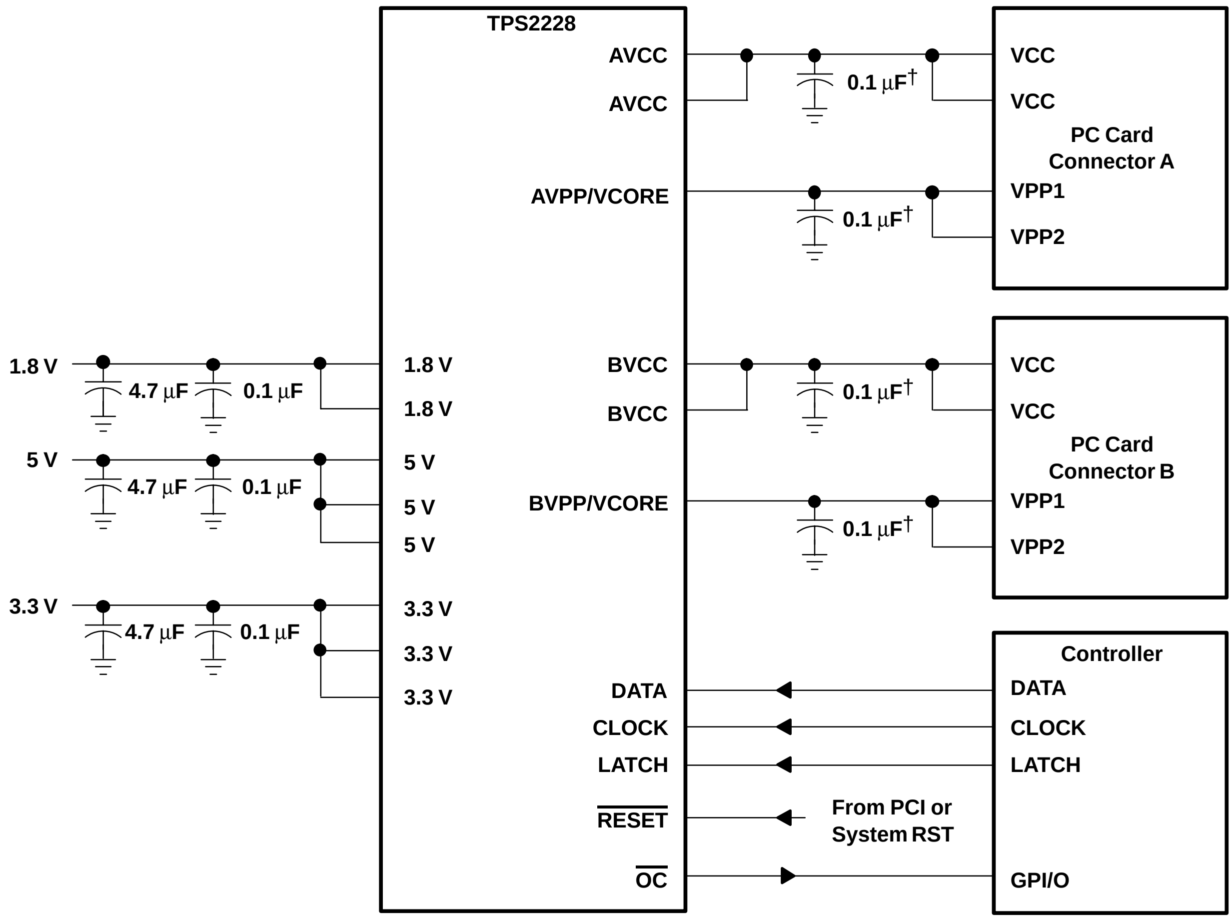
xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8(SHDN)	D3	D2		D8(SHDN)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

Table 2. TPS2221 Control Logic

TPAS2221 SINGLES					
D0	D1	D2	D3	VCC	VPP/CORE
0	0	0	0	0 V	0 V
0	0	0	1	Hi-Z	Hi-Z
0	0	1	0	Hi-Z	Hi-Z
0	0	1	1	Hi-Z	Hi-Z
0	1	0	0	3.3 V	0 V
0	1	0	1	3.3 V	3.3 V
0	1	1	0	3.3 V	5 V
0	1	1	1	3.3 V	1.8 V
1	0	0	0	5 V	0 V
1	0	0	1	5 V	3.3 V
1	0	1	0	5 V	5 V
1	0	1	1	5 V	1.8 V
1	1	0	0	Hi-Z	Hi-Z
1	1	0	1	3.3 V	Hi-Z
1	1	1	0	5 V	Hi-Z
1	1	1	1	Hi-Z	Hi-Z

NOTE: VCC = VPP/VCORE = Hi-Z indicates the device is in shutdown mode.



† Maximum recommended output capacitance for xVCC is 150 µF including card capacitance, and for xVPP is 10 µF, without $\overline{\text{OC}}$ glitch when switches are powered on.

Figure 20. TPS2228 Dual Slot Application

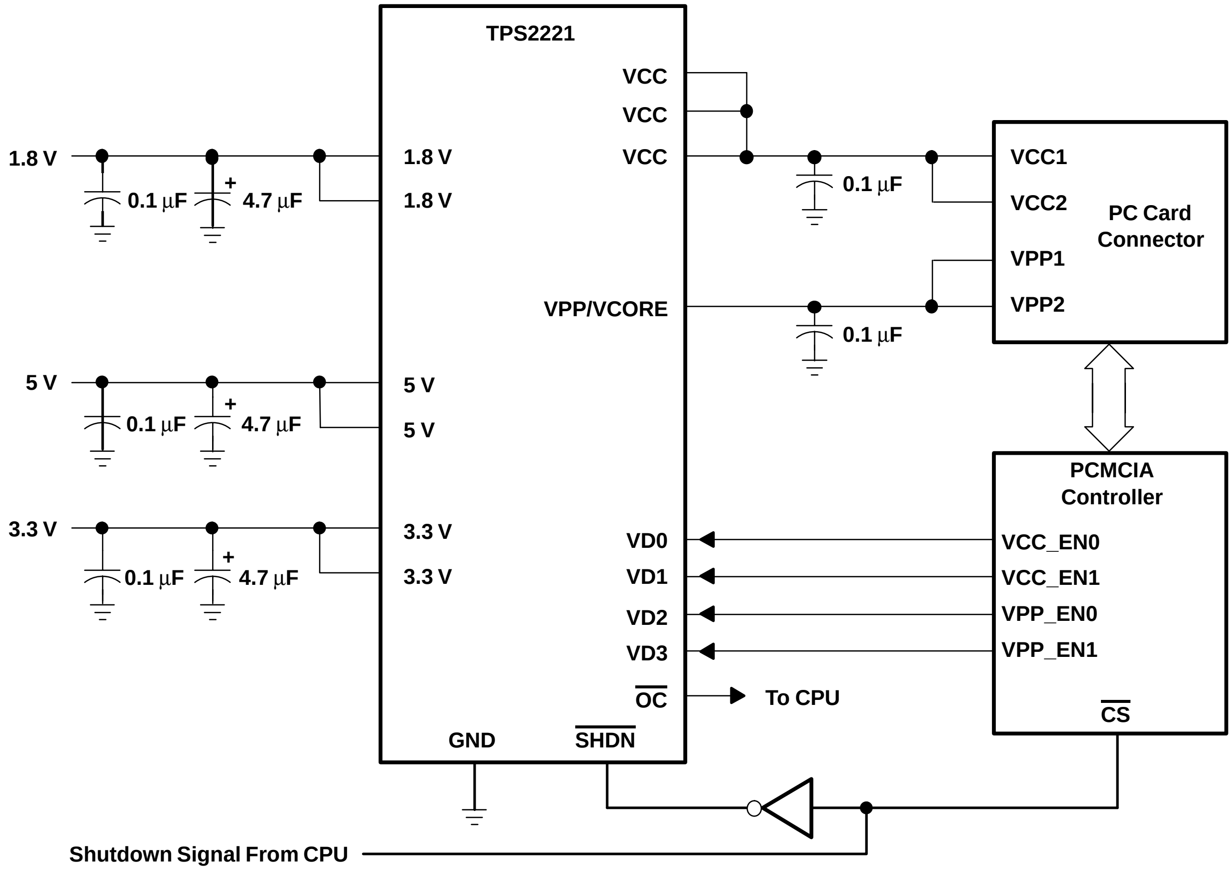
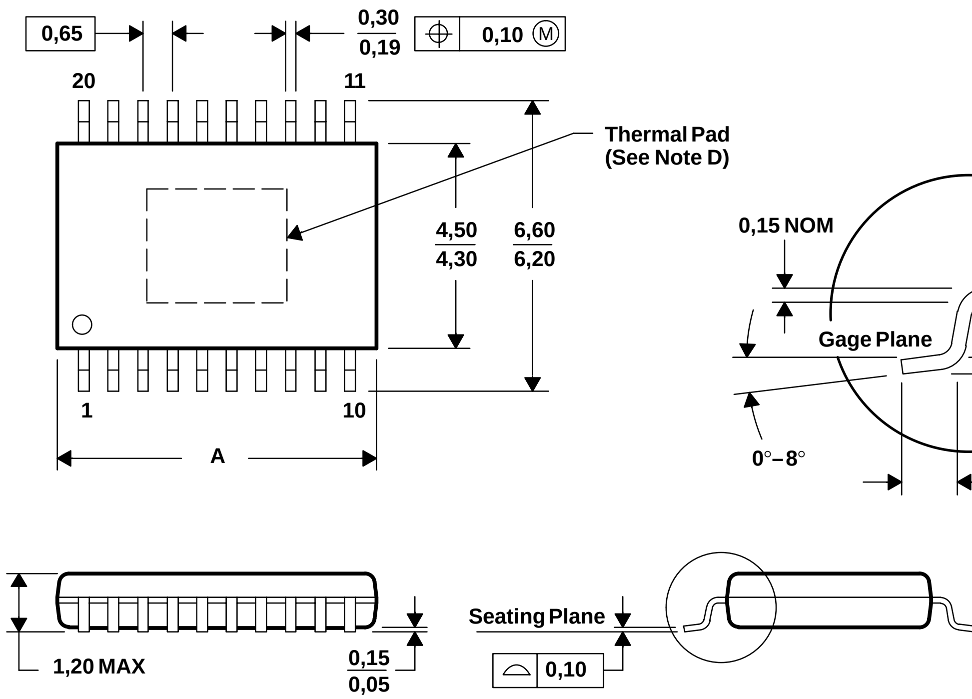


Figure 21. TPS2221 Single Slot Application

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F10/98

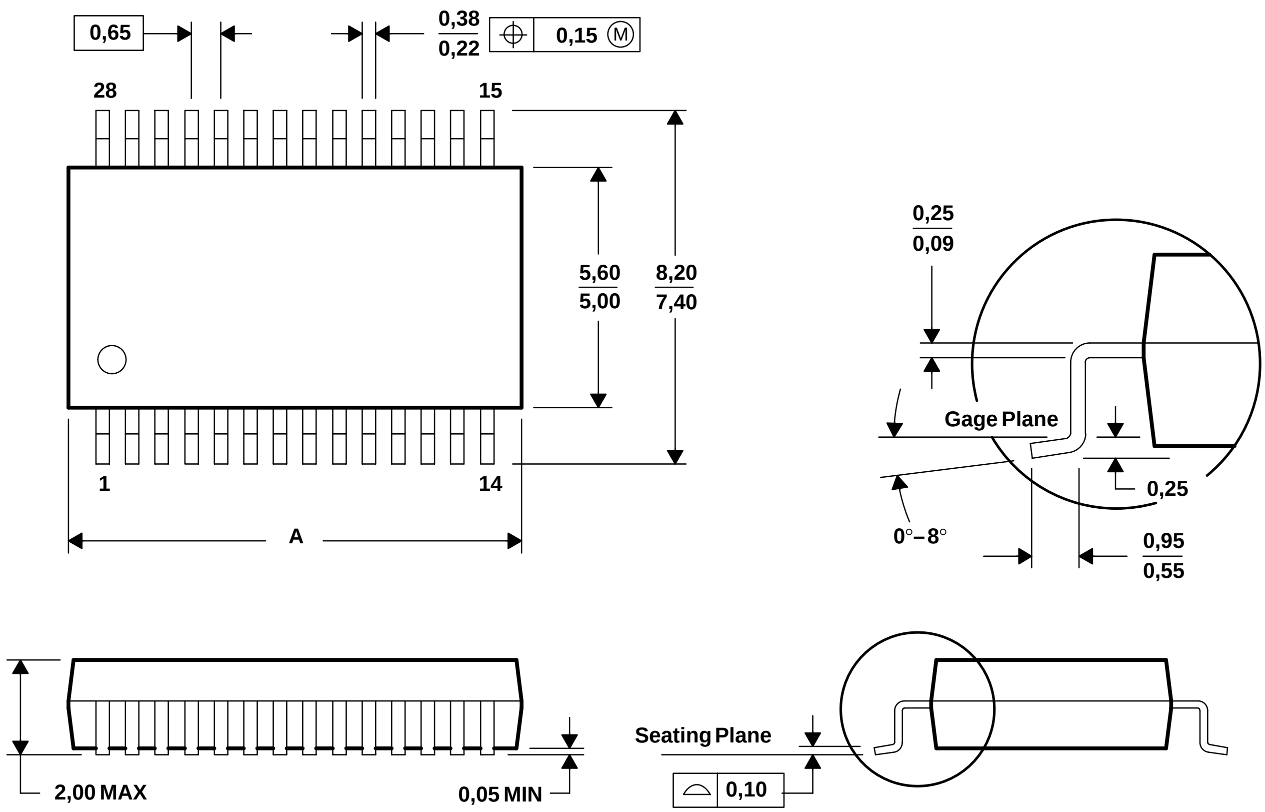
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065/E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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