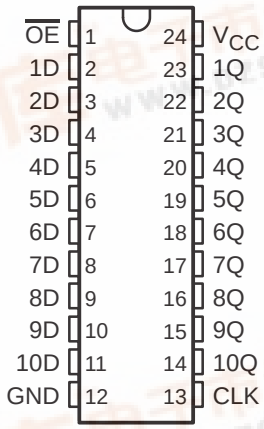
SN54ALS29821, SN74ALS29821
10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS145B – JANUARY 1986 – REVISED JANUARY 1995

- **Functionally Equivalent to AMD's AM29821**
- **Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity**
- **Outputs Have Undershoot-Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs Reduce dc Loading Effects**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54ALS29821 . . . JT PACKAGE
SN74ALS29821 . . . DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit edge-triggered D-type flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable ($\overline{OE}$) input can place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

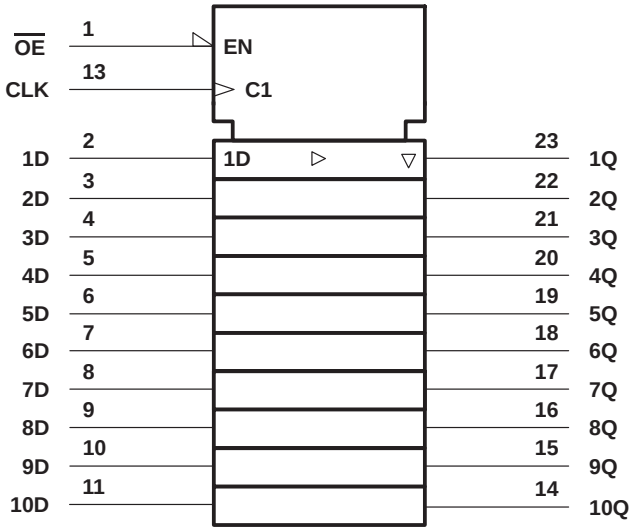
$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29821 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS29821 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each flip-flop)

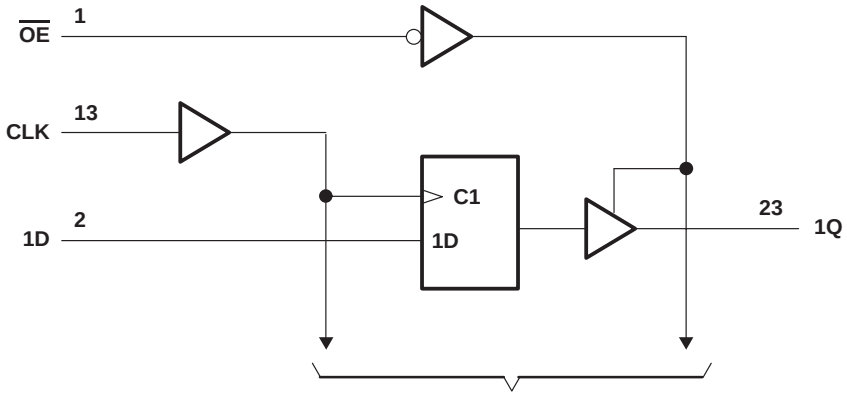
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS29821 . . . . . −55°C to 125°C
SN74ALS29821 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS29821			SN74ALS29821			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–24			–24	mA
I_{OL}	Low-level output current			48			48	mA
t_w	Pulse duration, CLK high or low	7			7			ns
t_{su}	Setup time, data before CLK↑	4			4			ns
t_h	Hold time, data after CLK↑	2			2			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS29821			SN74ALS29821			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.75 V	I_{OH} = –15 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = –24 mA	2	3.1		2	3.1		
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 48 mA		0.35	0.5		0.35	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V			50			20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			–50			–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.5			–0.2	mA
I_{OS}‡	V_{CC} = 5.25 V,	V_O = 0	–75		–250	–75		–250	mA
I_{CC}	V_{CC} = 5.25 V,	Outputs open		80	115		80	115	mA

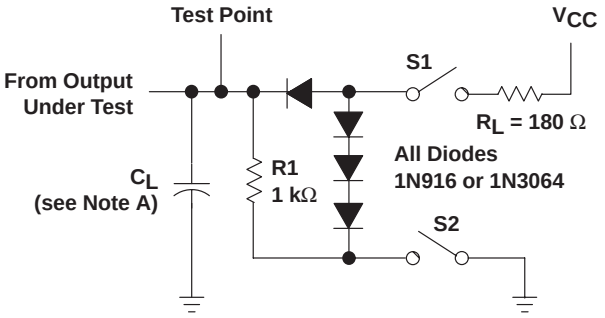
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = MIN to MAX†, T_A = MIN to MAX†				UNIT
				SN54ALS29821		SN74ALS29821		
				MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	C_L = 50 pF	2	11.5	2	10	ns
t_{PHL}				2	11.5	2	10	
t_{PLH}	CLK	Any Q	C_L = 300 pF	2	21		16	ns
t_{PHL}				2	21		16	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 50 pF	1	17		14	ns
t_{PZL}				1	17		14	
t_{PZH}	$\overline{OE}$	Any Q	C_L = 300 pF	1	25		20	ns
t_{PZL}				1	29.5		23	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 50 pF	1	16		14	ns
t_{PLZ}				1	14		12	
t_{PHZ}	$\overline{OE}$	Any Q	C_L = 5 pF	1	12		9	ns
t_{PLZ}				1	11		9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

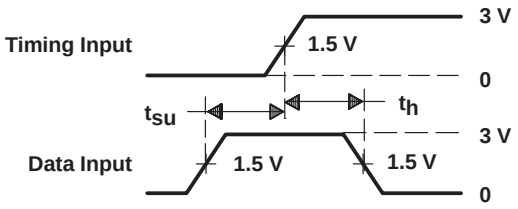
PARAMETER MEASUREMENT INFORMATION



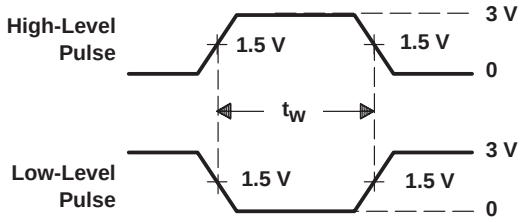
LOAD CIRCUIT

SWITCH POSITION TABLE

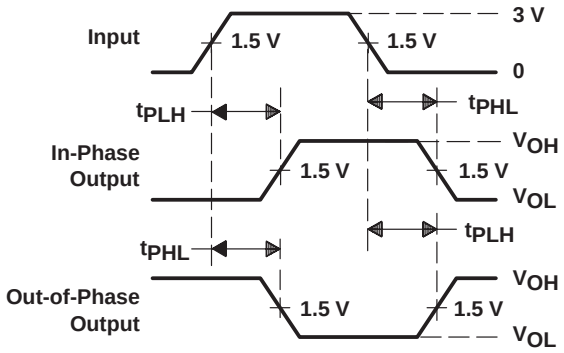
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



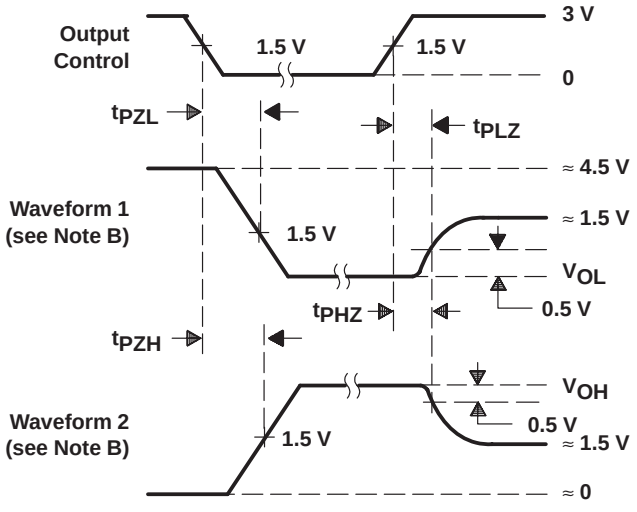
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

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