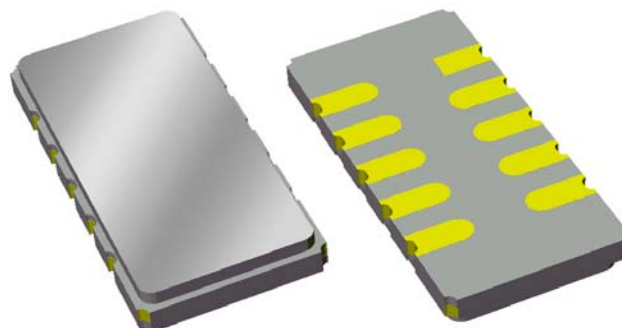


Preliminary Data Sheet

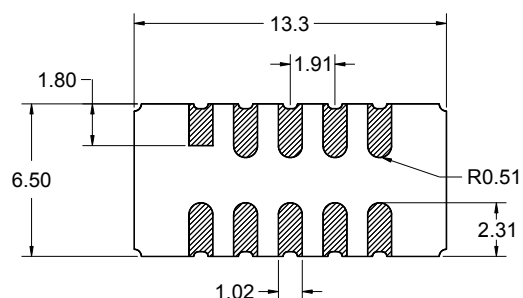
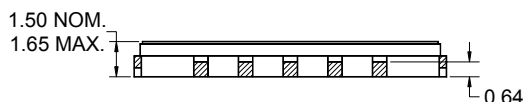
Features

- For GSM and EDGE applications
- Usable bandwidth of 0.22 MHz
- Typical 1 dB bandwidth of 0.34 MHz
- Low loss
- High attenuation
- Balanced operation at 200 Ω or Single-ended operation at 50 Ω (different matching required)
- Ceramic Surface Mount Package (SMP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



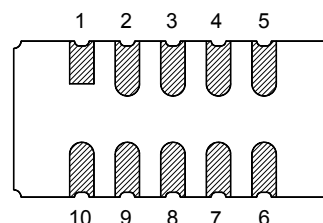
Package

Surface Mount 13.3 x 6.50 x 1.50 mm



Pin Configuration

Bottom View



Pin No.	Description
10,1	Input (Balanced)
5,6	Output (Balanced)
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters
 All tolerances are ± 0.15 mm except overall
 length and width ± 0.10 mm

Body: Al_2O_3 ceramic
 Lid: Kovar, Ni plated
 Terminations: Au plating 0.5 - 1.0 μ m,
 over a 2 - 6 μ m Ni plating

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

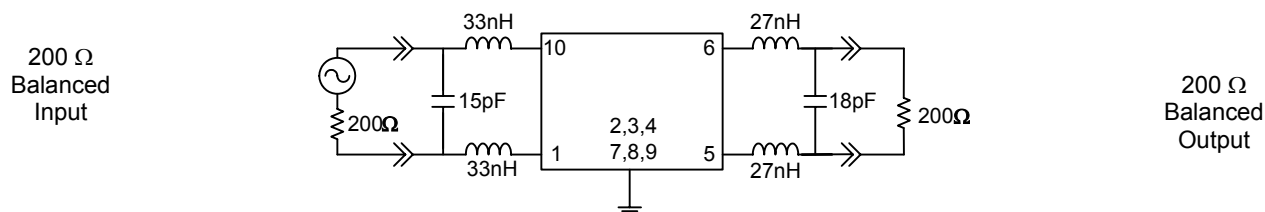
Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency (f_c)	-	201	-	MHz
Insertion Loss at 201 MHz	-	6.1	7	dB
1 dB Lower Bandedge	-	200.83	200.89	MHz
1 dB Upper Bandedge	201.11	201.17	-	MHz
Amplitude Variation ⁽⁴⁾ 200.89 - 201.11 MHz	-	0.6	1	dB p-p
Absolute Group Delay at f_c	2.05	2.3	2.55	μ s
Group Delay Variation 200.89 - 201.11 MHz	-	0.8	1.5	μ s
Stopband Attenuation ⁽⁵⁾				
$f_c \pm 0.3$ MHz to $f_c \pm 0.4$ MHz	16	25	-	dB
$f_c \pm 0.4$ MHz to $f_c \pm 0.6$ MHz	27	29	-	dB
$f_c \pm 0.6$ MHz to $f_c \pm 0.8$ MHz	28	32	-	dB
$f_c \pm 0.8$ MHz to $f_c \pm 1.5$ MHz	36	40	-	dB
$f_c \pm 1.5$ MHz to $f_c \pm 35$ MHz	38	40	-	dB
Source Impedance (Balanced) ⁽⁶⁾	-	200	-	Ω
Load Impedance (Balanced) ⁽⁶⁾	-	200	-	Ω

Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Amplitude variation is defined as the difference between the lowest loss and the highest loss within defined frequency points
5. Referenced to insertion loss at 201 MHz
6. This is the optimum impedance in order to achieve the performance shown

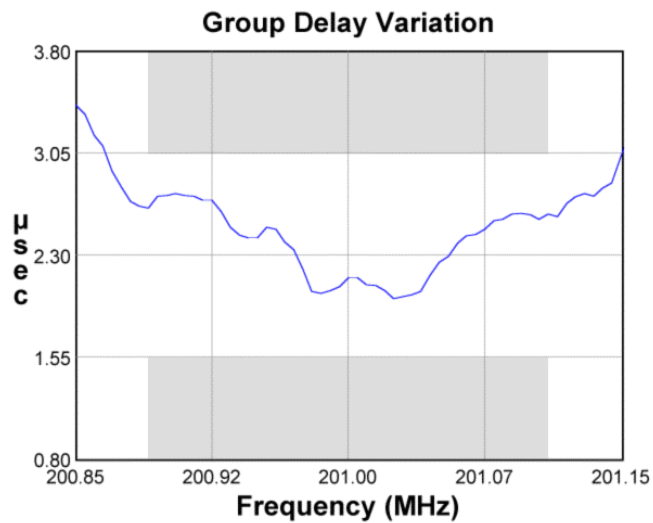
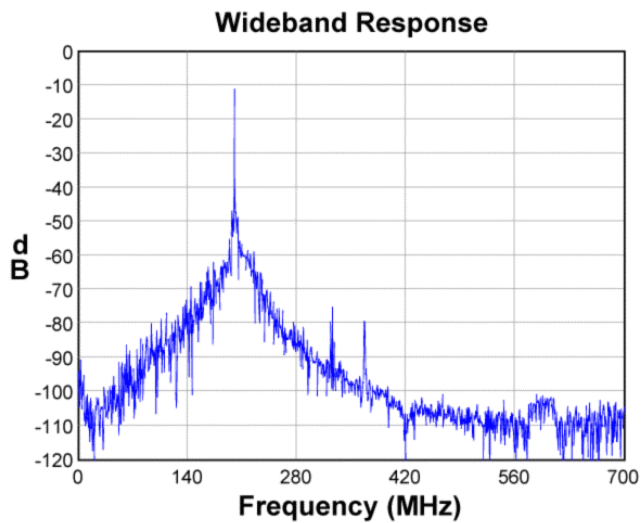
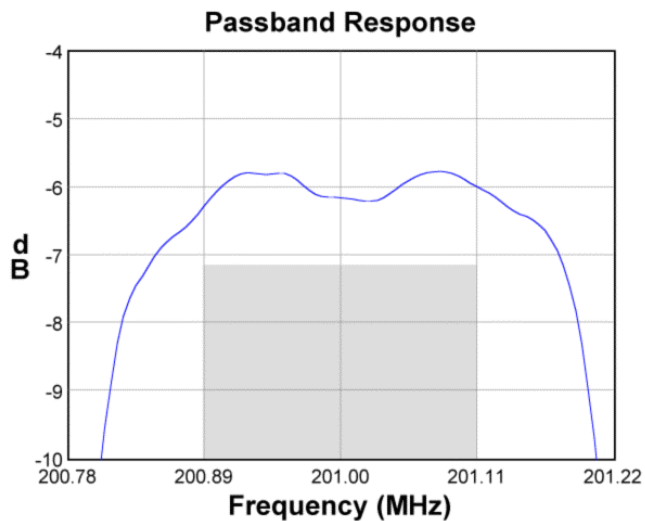
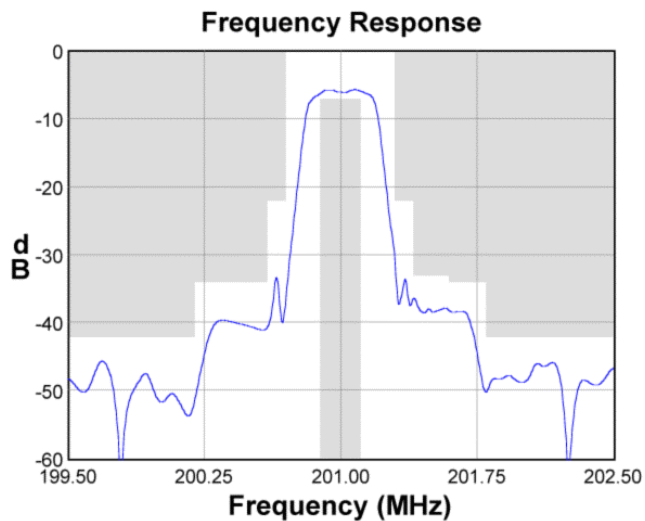
Test Circuit:

Actual matching values may vary due to PCB layout and parasitics

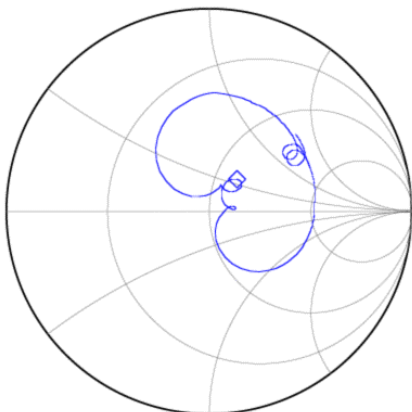


Preliminary Data Sheet

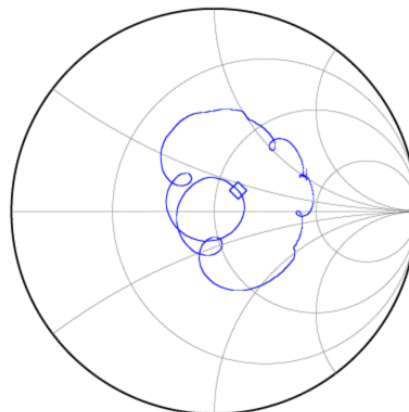
Typical Performance (at +25°C)



Input Smith Chart



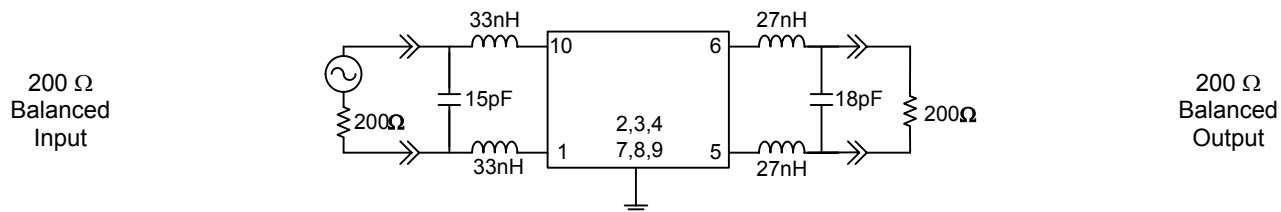
Output Smith Chart



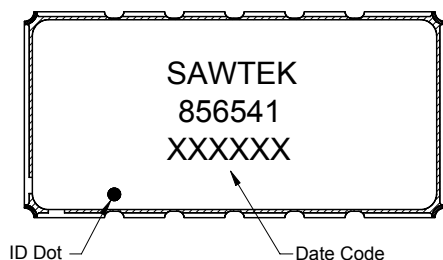
Preliminary Data Sheet

Matching Schematics

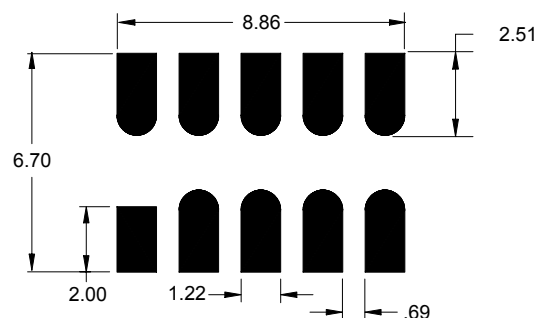
Actual matching values may vary due to PCB layout and parasitics



Marking



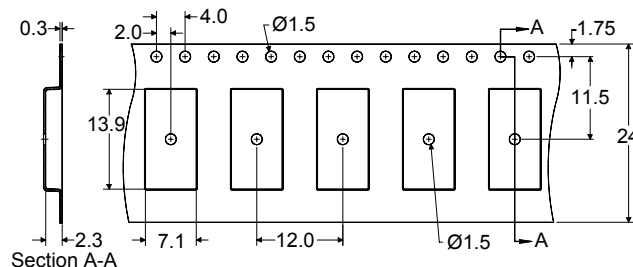
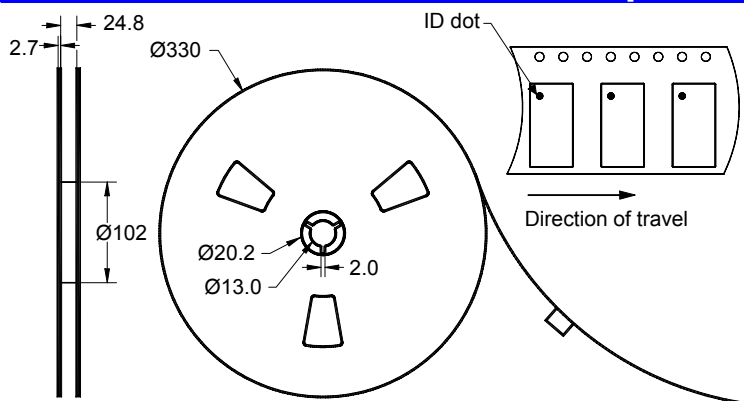
PCB Footprint



The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity:2000 units/reel

Preliminary Data Sheet

Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	0	+70	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)[Qualification Flowchart](#)[Soldering Profile](#)[S-Parameters](#)[RoHS information](#)[Other Technical Information](#)

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[representatives or distributors](#)