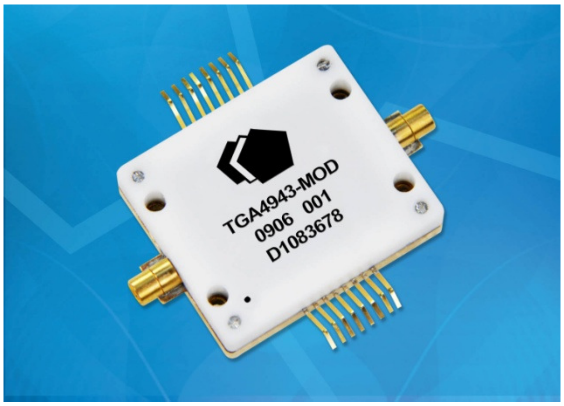
TGA4943-MOD

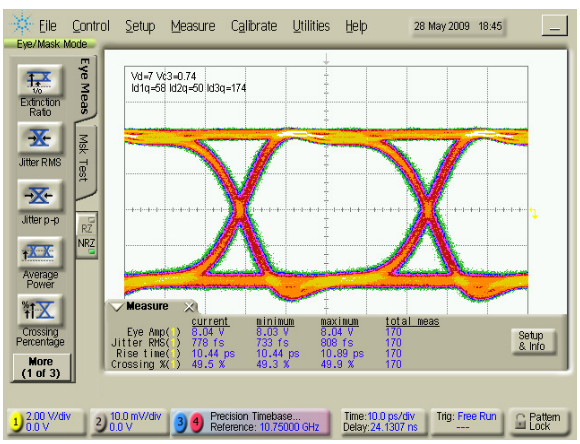
40 & 100 Gb/s 8Vpp Optical Modulator Driver Module

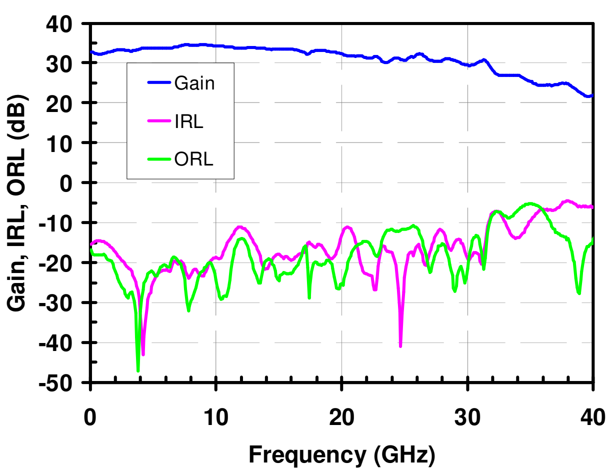


Measured Performance

Bias conditions: Vd1,2,3 = 7 V, Idq = 310 mA,
Vc1,2,3 = 0.7, 0.7, 0.8 V Typical

Vin = 0.5 Vpp, Vout = 8Vpp, 21.5 Gbps, PRBS 2^31 -1





Key Features

- 40 & 100 Gb/s Performance
- Single Ended Input and Output
- Adjustable Output Amplitude, 3 Vpp – 9 Vpp
- Low Additive RMS Jitter, 400 fsec
- High Output Drive, 8Vpp with 0.4 Vpp Input
- Gain, 32 dB at 20 GHz
- Low DC Power Dissipation, 1.7 W for Vout = 8Vpp at Vd=6 V
- Rise and Fall Times <12 psec
- Hot-Pluggable
- Module Size: 28.5 x 24 x 6.48 mm

Primary Applications

- 40 GB/s Optical Market: DQPSK (2x)
- 100 GB/s Optical Market: DP-QPSK (4x)

Product Description

The TriQuint TGA4943-MOD is a three stage optical modulator driver module designed to operate at frequencies that target the 40 and 100 Gb/s optical market.

The TGA4943-MOD consists of three high performance wideband amplifiers assembled in a module that includes all necessary components for operation. A single TGA4943-MOD placed between the MUX and Optical Modulator provides OEMs with a modulator driver solution.

The TGA4943-MOD provides Metro and Long Haul designers with system critical features such as: low power dissipation, low rail ripple, high voltage drive capability (3 Vpp amplitude adjustable up to 9 Vpp), low output jitter, and low input drive sensitivity (0.4 Vpp – 1 Vpp at Vout = 8Vpp).

The TGA4943-MOD is lead-free and RoHS compliant. TGA4943-MOD parts are available upon request for evaluation purposes.

Datasheet subject to change without notice.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd1, Vd2, Vd3	Drain Voltage	9 V	2/ 3/ 4/ 5/
Vd1-Vg1, Vd2-Vg2, Vd3-Vg3	Drain to Gate Voltage	10 V, 13 V, 13 V	2/ 3/ 4/ 5/
Vg1, Vg2, Vg3	Gate Voltage Range	-5 to 0 V	
Vc1, Vc2, Vc3	Control Voltage Range	(Vd-7) to +5.5 V	3/ 4/ 5/
Id1, Id2	Drain Current	80, 135 mA	2/
Id3	Drain Current	270 mA	2/
Ig1, Ig2, Ig3	Gate Current Range	-15 to 21 mA, -30 to 21 mA, -30 to 21 mA	5/
Ic1, Ic2, Ic3	Control Current Range	-15 to 21 mA	5/
Vin_pp	Peak-Peak Input Voltage	7 V	
Pin	Input Continuous Wave Power	24 dBm	2/
Pd	Max Power Dissipation	3.05	6/
Tch	Maximum Channel Temperature	200 °C	

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

3/ Assure Vd1 – (Vc1-Vg1) – Id1*50 ≤ 6.5 V,

Assure Vd2 – (Vc2-0.34*Vg2) – Id2*50 ≤ 6.5 V,

Assure Vd3 – (Vc3-0.34*Vg3) ≤ 6.5 V,

4/ Assure Vd-Vc >= -0.5.

5/ HOT PLUGGABLE: Comply with voltage and currents outlined in Max Ratings Table.

6/ Maximum Power Dissipation is based upon Baseplate temperature of 80 °C and Channel Temperature of 200 °C, using the thermal resistance published in Table IV.

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Table II
Recommended Operating Conditions
21.5 Gbps Operation

Output Voltage (Vpp)	Drain Voltage: Vd1, Vd2, Vd3 (V)	Quiescent Drain Current: Idq1, Idq2, Idq3 (mA)	Under RF Drive Drain Current: Id1+ Id2 + Id3 (mA)	Control Voltage: Vc1, Vc2, Vc3 (V)	Gate Voltage: Vg1, Vg2, Vg3 (V)*	Pdiss (W)
3.6	5	40, 30, 84	198	0.7, 0.7, -0.23	-0.56, -1.89, -1.34	0.96
4	5	40, 30, 100	207	0.7, 0.7, -0.01	-0.56, -1.89, -1.25	1.00
5	5	40, 30, 133	230	0.7, 0.7, 0.23	-0.56, -1.89, -1.09	1.09
6	5	40, 30, 160	254	0.7, 0.7, 0.42	-0.56, -1.89, -0.97	1.18
4	6	51, 51, 63	233	0.7, 0.7, -0.06	-0.51, -1.68, -1.53	1.32
5	6	51, 51, 100	257	0.7, 0.7, 0.14	-0.51, -1.68, -1.30	1.42
6	6	51, 51, 135	281	0.7, 0.7, 0.36	-0.51, -1.68, -1.11	1.51
7	6	51, 51, 167	305	0.7, 0.7, 0.59	-0.51, -1.68, -0.95	1.59
8	6	51, 51, 201	330	0.7, 0.7, 0.86	-0.51, -1.68, -0.78	1.66
6	7	62, 50, 98	302	0.7, 0.7, 0.24	-0.47, -1.74, -1.34	2.03
7	7	62, 50, 144	326	0.7, 0.7, 0.45	-0.47, -1.74, -1.09	2.16
8	7	62, 50, 179	348	0.7, 0.7, 0.66	-0.47, -1.74, -0.92	2.28
9	7	62, 50, 223	373	0.7, 0.7, 0.91	-0.47, -1.74, -0.69	2.4

* Gate and control voltages should be adjusted to reach target drain currents and optimal eye performance and may vary from above voltages.

Table III
RF Characterization Table

Bias: Vd = 7 V, Idq=300 mA, Vc1, Vc2 = +0.7 V, Vc3 = 0.8 V, typical

Small Signal Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Gain	Small Signal Gain	f = 0.1 - 20 GHz f = 20.1 - 30 GHz f = 30.1 - 36 GHz f = 36.1 – 40 GHz	- - - -	32 30 28 20	- - - -	dB
IRL	Input Return Loss	f = 0.1 - 10 GHz f = 10.1 - 20 GHz f = 20.1 – 30 GHz f = 30.1 – 40 GHz	- -	15 13 11 4	- -	dB
ORL	Output Return Loss	f = 0.1 - 24 GHz f = 24.1 - 34 GHz f = 34.1 – 40 GHz	- -	15 8 6	- -	dB
BW	3 dB Bandwidth	f(x) – f(1 GHz) = 3 dB x = freq of 3 dB BW	-	27	-	GHz

Table III - Cont.
RF Characterization Table

Bias: Vd = 7 V, Idq = 300 mA, Vc1, Vc2 = 0.6 V, Vc3 = 0.8 V, typical

Electrical Eye Test Conditions: Vin = 0.5 Vpp, PRBS 2^{31}-1, 21.5 Gbps, Crossing = 50% +/- 2%

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Vout_Max	Maximum Eye Amplitude	500 mVpp Input	-	10	-	Vpp
Tr	Risetime	8 Vpp Output	-	11	-	psec
Tf	Falltime	8 Vpp Output		11		psec
SNR	Signal to Noise Ratio	8 Vpp Output		20		dB
Eye Opening	1/	8 Vpp Output		85		%
Jrms_Add	Additive Jitter 2/	8 Vpp Output		400		fsec
Jpp	P-P Jitter	8 Vpp Output		7		psec
Id	Total Drain Current	8 Vpp Output	-	350	-	mA

1/ Eye Opening defined as: [Eye Height (Vpp)/Eye Amplitude (Vpp)] *100

2/ Additive Jitter defined as: Sqrt [(Total RMS Jitter)^2 – (Input RMS Jitter)^2]

Table IV
Power Dissipation and Thermal Properties

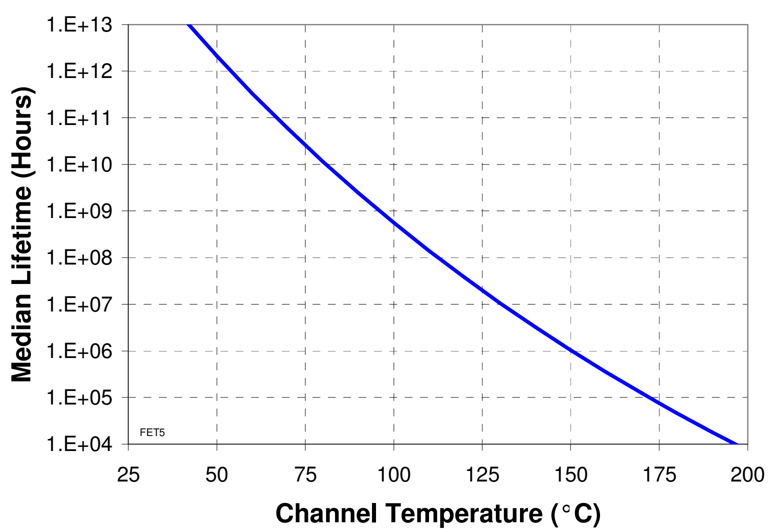
Parameter	Test Conditions	Value	Notes
Thermal Resistance, θjc	Vd = 7 V Idq_tot = 300 mA; Idq3=190 mA Pd_stage3 = 1.33 W Tbaseplate = 70 ºC	θjc = 55.8 (ºC/W) Tchannel = 144.2 ºC Tm = 1.9 E+6 Hrs	1/, 2/
Thermal Resistance, θjc Under RF Drive	Vout = 8 Vpp, Vd = 7V Id3 = 190 mA Pd_stage3 =1.17 W Tbaseplate = 70 ºC	θjc = 55.8 (ºC/W) Tchannel = 135.3 ºC Tm = 5.5 E+6 Hrs	
Storage Temperature		-65 to 150 ºC	

1/ Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

2/ θjc is modeled based upon hottest stage (stage 3) because there is negligible thermal coupling between stages. It is the thermal resistance of the part calculated from the junction to the bottom of the TGA4943-MOD package.

To calculate the temperature rise, calculate the dissipated power in the third stage (Pdiss = Idq3*Vd3) and multiply by θjc. For example: Tbase = 70 ºC, Idq3 = 190 mA, Vd3 = 7V. Pdiss_stage3 = 1.33 W. θjc=55.8 ºC/W. Temperature rise = θjc*Pdiss = 74.2 C; Tchannel = Tbase + Temp rise = 142.2 ºC

Median Lifetime (Tm) vs. Channel Temperature



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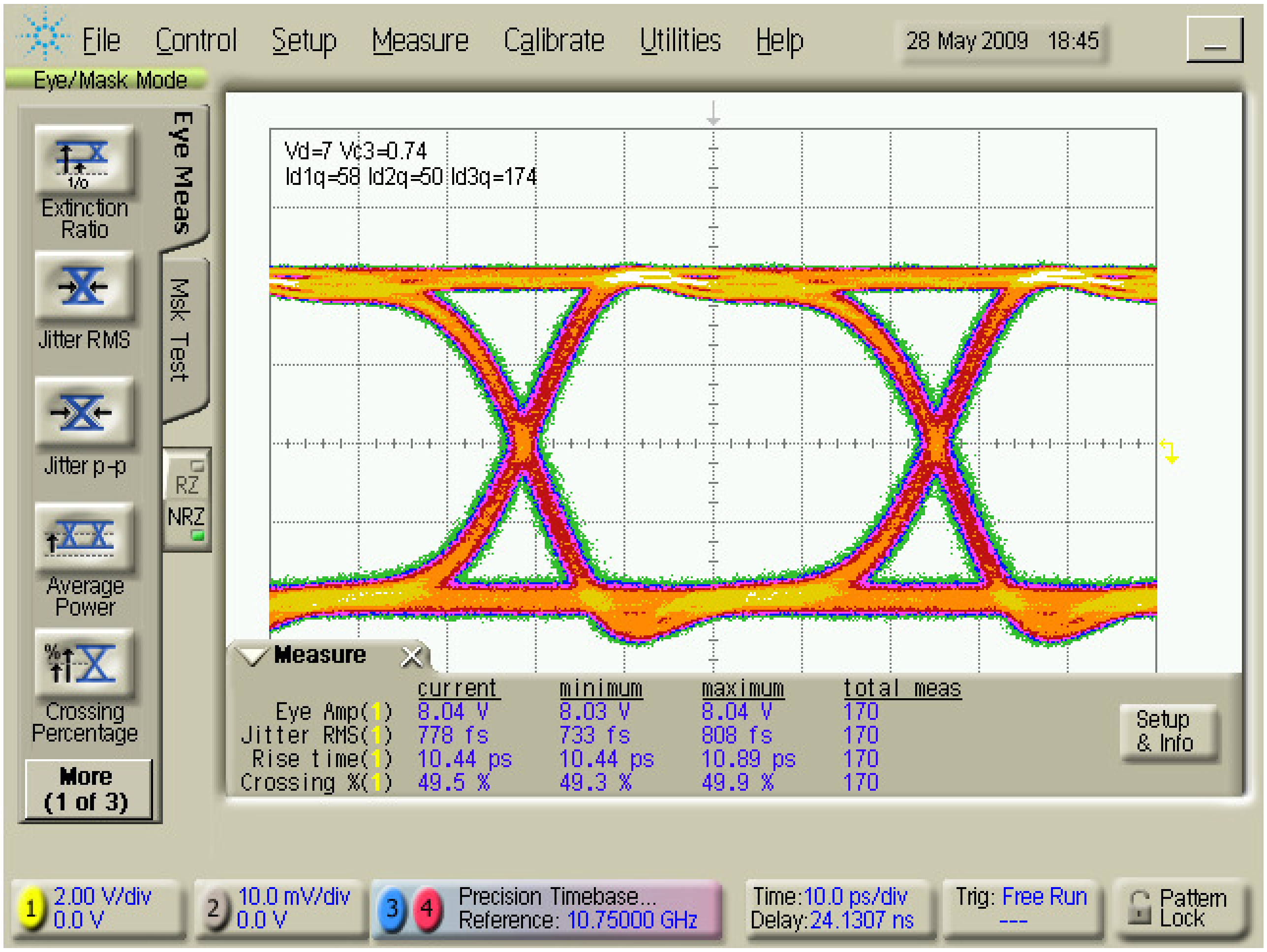
Vd = 7 V, Vin = 0.5 Vpp, Vout = 8 Vpp, 21.5 Gb/s, PRBS 2^{31} -1



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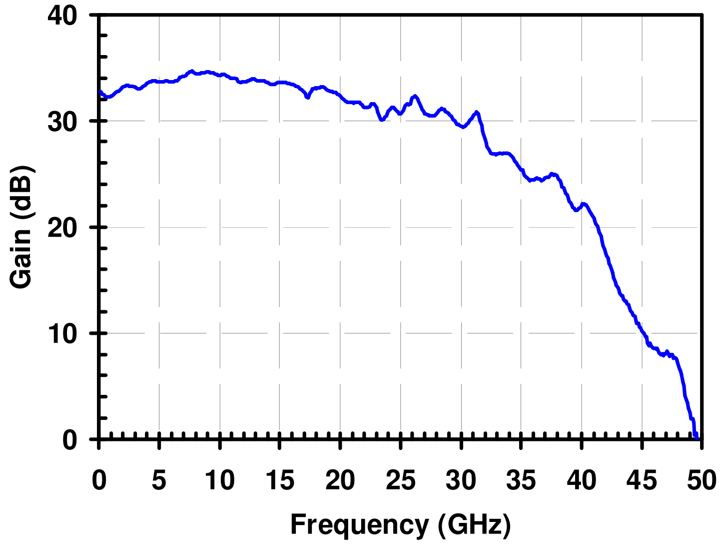
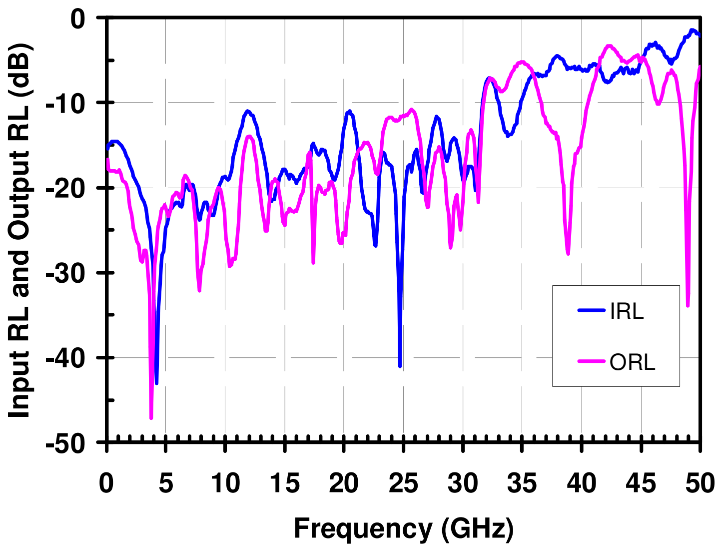
Measured Data
Bias Conditions: Vd = 7 V, Idq = 293 mA,
Vg1,2,3 = -0.5, -1.7, -0.9 V, Vc1,2,3 = 0.7, 0.7, 0.7 V Typical





Ordering Information

Part	Package Style
TGA4943-MOD	Module (RoHS)

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