ALPHA & OMEGA SEMICONDUCTOR

AO3404A
N-Channel Enhancement Mode Field Effect Transistor

General Description

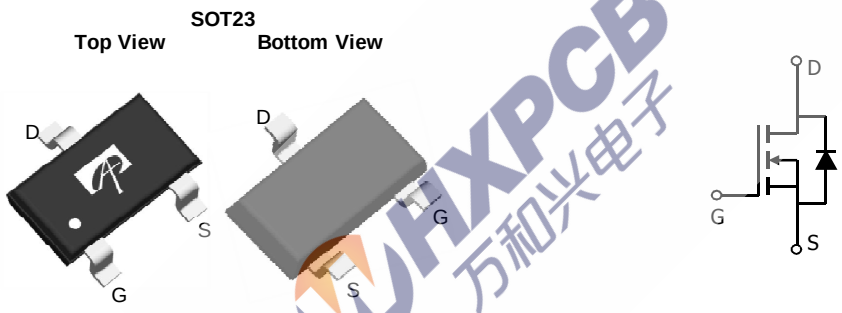
The AO3404A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. The source leads are separated to allow a Kelvin connection to the source, which may be used to bypass the source inductance.

Features

V_{DS} (V) = 30V
I_D = 5.8A (V_{GS} = 10V)
$R_{DS(ON)}$ < 25mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 35mΩ (V_{GS} = 4.5V)

Green Product

SOT23



Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A,F]	T_A=25℃	I_D	5.8	A
	T_A=70℃		4.9	
Pulsed Drain Current [B]		I_{DM}	64	
Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	65	90	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		85	125	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	63	80	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.5	2.1	2.6	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	64			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5.8A		18.4	25	mΩ
		T_J=125℃		26.2	36	
		V_{GS}=4.5V, I_D=4.8A		24.5	35	mΩ
g_{FS}	Forward Transconductance	VDS=5V, ID=5.8A		22		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		373	448	pF
C_{oss}	Output Capacitance			67		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.8	2.8	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	VGS=10V, VDS=15V, ID=5.8A		7.1	11	nC
Q_g(4.5V)	Total Gate Charge			3.3		nC
Q_{gs}	Gate Source Charge			1.4		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.6Ω, R_{GEN}=3Ω		4.5	6.5	ns
t_r	Turn-On Rise Time			2.4		ns
$t_{D(off)}$	Turn-Off DelayTime			14.8		ns
t_f	Turn-Off Fall Time			2.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5.8A, dI/dt=100A/µs		10.5	12.6	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5.8A, dI/dt=100A/µs		4.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.
F.The current rating is based on the t≤ 10s thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

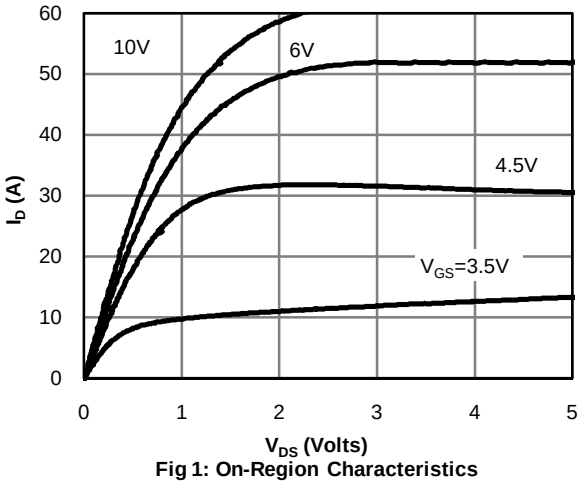

Fig 1: On-Region Characteristics

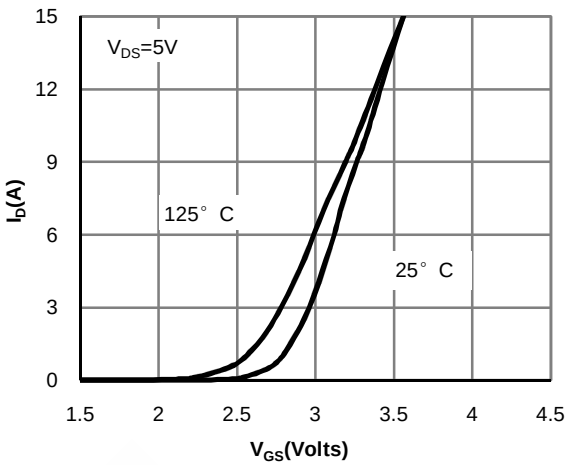

Figure 2: Transfer Characteristics

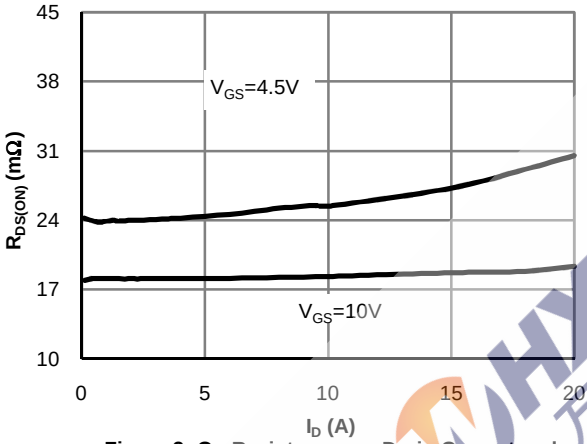

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

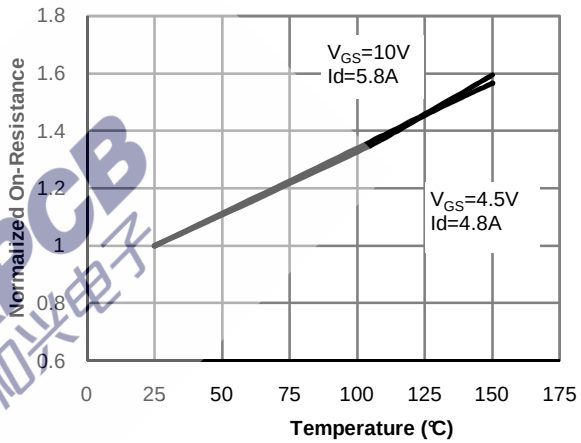

Figure 4: On-Resistance vs. Junction Temperature

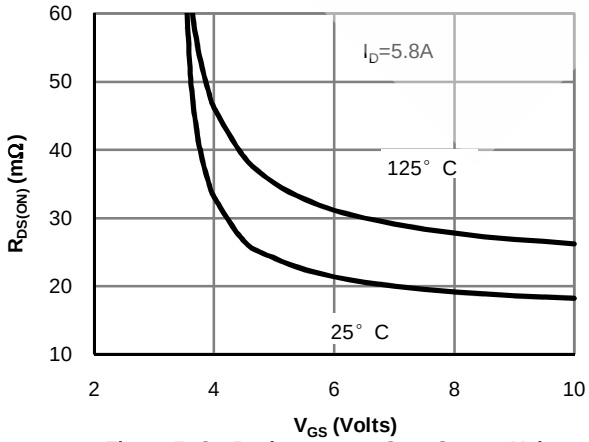

Figure 5: On-Resistance vs. Gate-Source Voltage

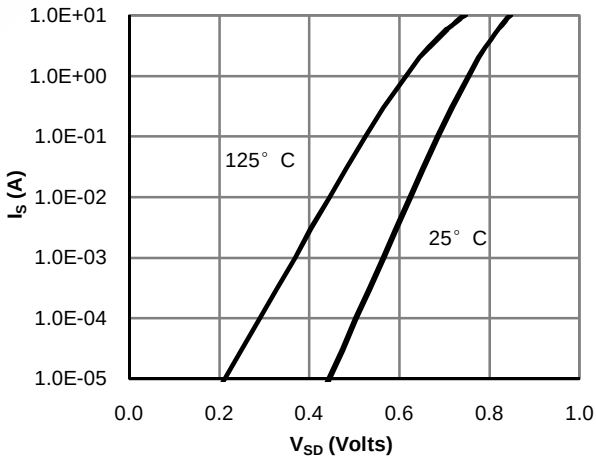

Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

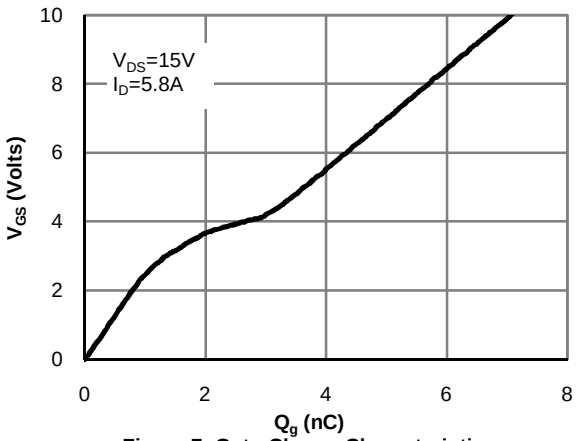

Figure 7: Gate-Charge Characteristics

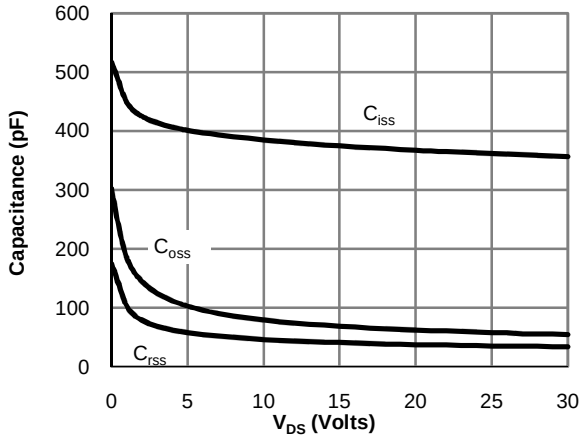

Figure 8: Capacitance Characteristics

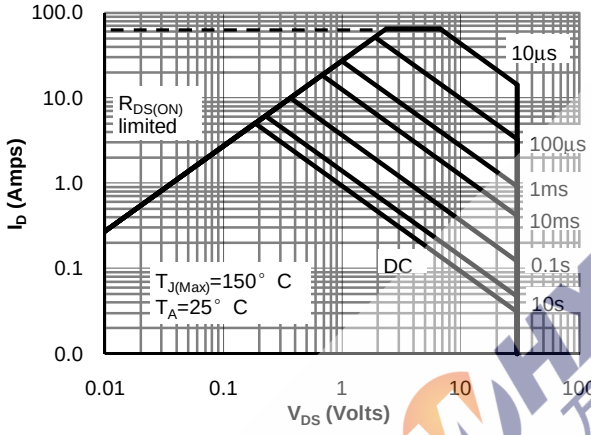

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

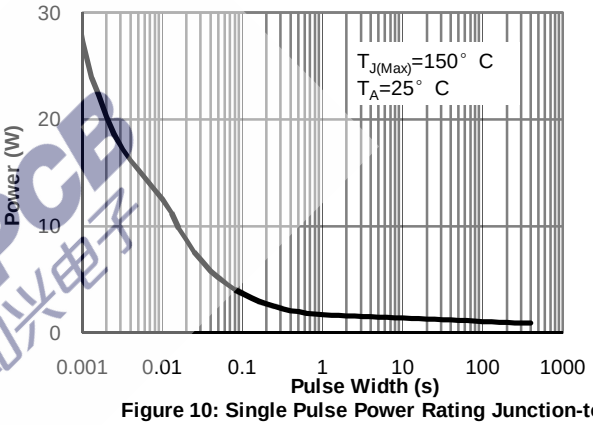

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

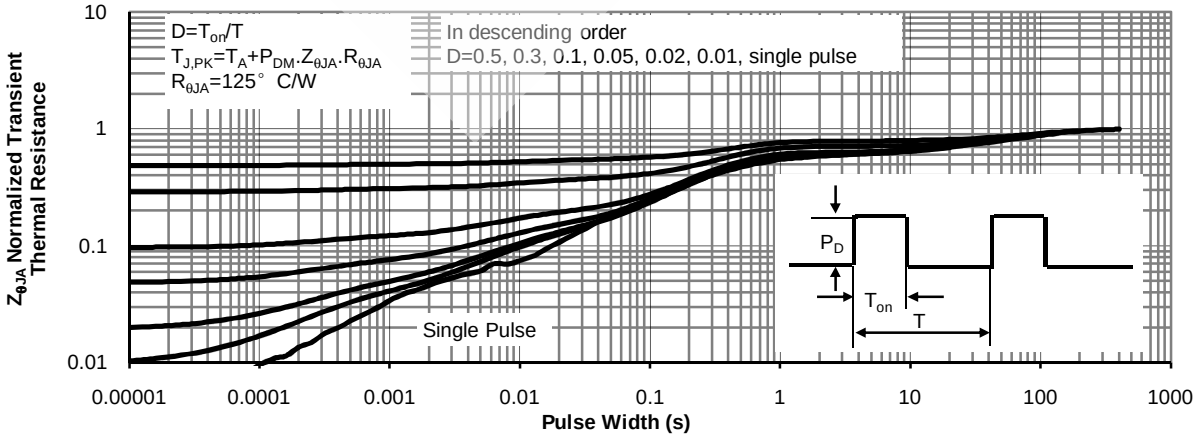

Figure 11: Normalized Maximum Transient Thermal Impedance