FAIRCHILD SEMICONDUCTOR™

August 1989
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100329A
Low Power Octal ECL/TTL Bidirectional Translator with Register

General Description

The 100329A is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is –2.0V, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus.

The 100329A is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

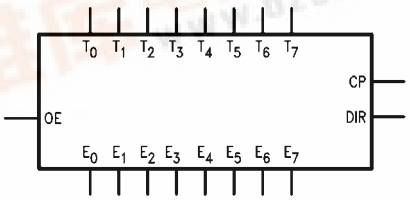
Features

- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- 3-STATE outputs
- Voltage compensated operating range = –4.2V to –5.7V
- High drive IOS

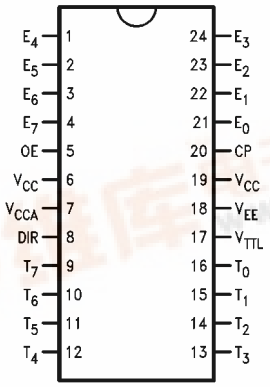
Ordering Code:

Order Number	Package Number	Package Description
100329APC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
CP	Clock Pulse Input (Active Rising Edge)
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

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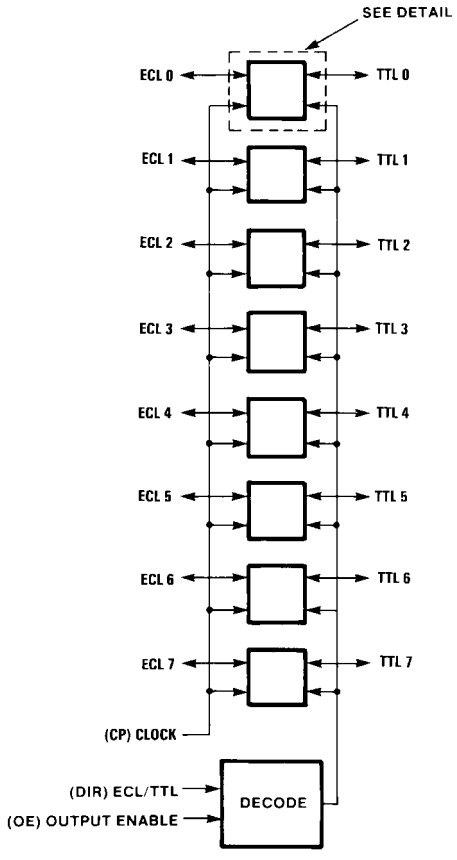
Truth Table

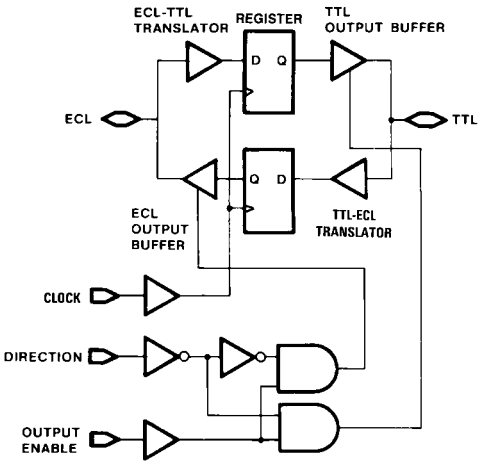
OE	DIR	CP	ECL Port	TTL Port	Notes
L	L	X	Input	Z	1, 3
L	H	X	LOW (Cut-Off)	Input	2, 3
H	L	[N]	L	L	1
H	L	[N]	H	H	1
H	L	L	X	NC	1, 3
H	H	[N]	L	L	2
H	H	[N]	H	H	2
H	H	L	NC	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
[N] = LOW-to-HIGH Clock Transition
NC = No Change

Functional Diagram



Detail



Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before CP.

Note: DIR and OE use ECL logic levels

Absolute Maximum Ratings (Note 4)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_j)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current	
(DC Output HIGH)	−50 mA
TTL Input Voltage (Note 6)	−0.5V to +6.0V
TTL Input Current (Note 6)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State	
3-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD (Note 5)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	0°C to +85°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Note 4: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: ESD testing conforms to MIL-STD-883, Method 3015.

Note 6: Either voltage limit or current limit is sufficient to protect inputs.

TTL-to-ECL DC Electrical Characteristics (Note 7)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	Loading with 50Ω to −2V
	Cutoff Voltage		−2000	−1950	mV	OE or DIR LOW, V_{IN} = V_{IH} (Max) or V_{IL} (Min) Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point HIGH	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max) Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point LOW			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current					LE LOW, OE and DIR HIGH Inputs OPEN
		−189		−94	mA	V_{EE} = −4.2V to −4.8V
		−199		−94		V_{EE} = −4.2V to −5.7V

Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

ECL-to-TTL DC Electrical Characteristics (Note 8)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7	3.1		V	I_{OH} = −3 mA, V_{TTL} = 4.75V
		2.4	2.9		V	I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current			350	µA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = V_{IL} (Min)
I_{OZHT}	3-STATE Current Output HIGH			70	µA	V_{OUT} = +2.7V
I_{OZLT}	3-STATE Current Output LOW	−700			µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−225		−100	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74	mA	TTL Outputs LOW
				49	mA	TTL Outputs HIGH
				67	mA	TTL Outputs in 3-STATE

Note 8: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

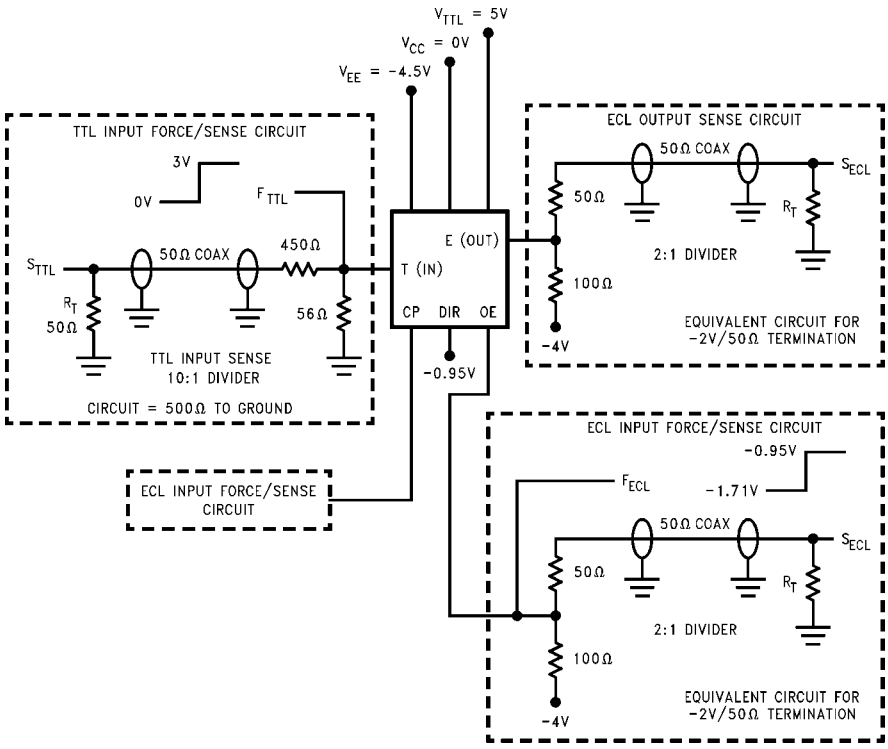
Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Max Toggle Frequency	350		350		350		MHz	
t_{PLH}	CP to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns	Figures 1, 2
t_{PHL}									
t_{PZH}	OE to E_n (Cut-off to HIGH)	1.3	4.2	1.5	4.4	1.7	4.8	ns	Figures 1, 2
t_{PHZ}	OE to E_n (HIGH to Cut-off)	1.5	4.5	1.6	4.5	1.6	4.6	ns	Figures 1, 2
t_{PHZ}	DIR to E_n (HIGH to Cut-off)	1.6	4.3	1.6	4.3	1.7	4.5	ns	Figures 1, 2
t_{set}	T_n to CP	1.1		1.1		1.1		ns	Figures 1, 2
t_{hold}	T_n to CP	1.7		1.7		1.9		ns	Figures 1, 2
t_{pw}(H)	Pulse Width CP	2.1		2.1		2.1		ns	Figures 1, 2
t_{TLH}	Transition Time	0.6	1.6	0.6	1.6	0.6	1.6	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

DIP ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50.pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Max Toggle Frequency	125		125		125		MHz	
t_{PLH}	CP to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	Figures 3, 4
t_{PHL}									
t_{PZH}	OE to T_n	3.4	8.45	3.7	8.95	4.0	9.7	ns	Figures 3, 5
t_{PZL}	(Enable Time)	3.8	9.2	4.0	9.2	4.3	9.95		
t_{PHZ}	OE to T_n	3.2	8.95	3.3	8.95	3.5	9.2	ns	Figures 3, 5
t_{PLZ}	(Disable Time)	3.0	7.7	3.4	8.7	4.1	9.95		
t_{PHZ}	DIR to T_n	2.7	8.2	2.8	8.7	3.1	8.95	ns	Figures 3, 6
t_{PLZ}	(Disable Time)	2.8	7.45	3.1	7.95	4.0	9.2		
t_{set}	E_n to CP	1.1		1.1		1.1		ns	Figures 3, 4
t_{hold}	E_n to CP	2.1		2.1		2.6		ns	Figures 3, 4
t_{pw}(H)	Pulse Width CP	4.1		4.1		4.1		ns	Figures 3, 4

Test Circuitry (TTL-to-ECL)



Note: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

Note: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note: V_{TTL} is decoupled to ground with 0.1 μF, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

FIGURE 1. TTL-to-ECL AC Test Circuit

Switching Waveforms (TTL-to-ECL)

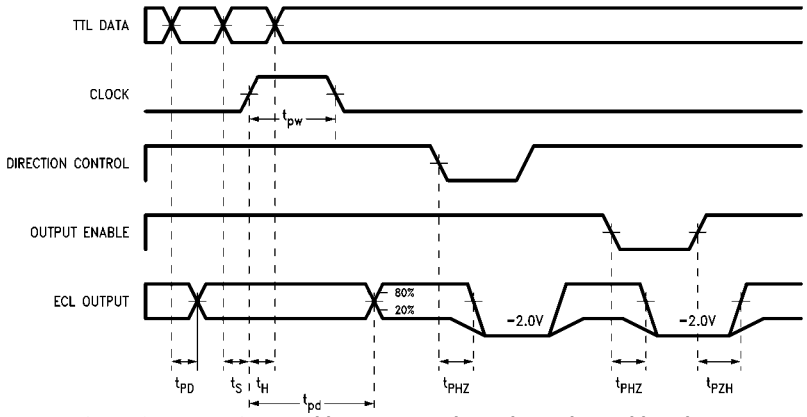
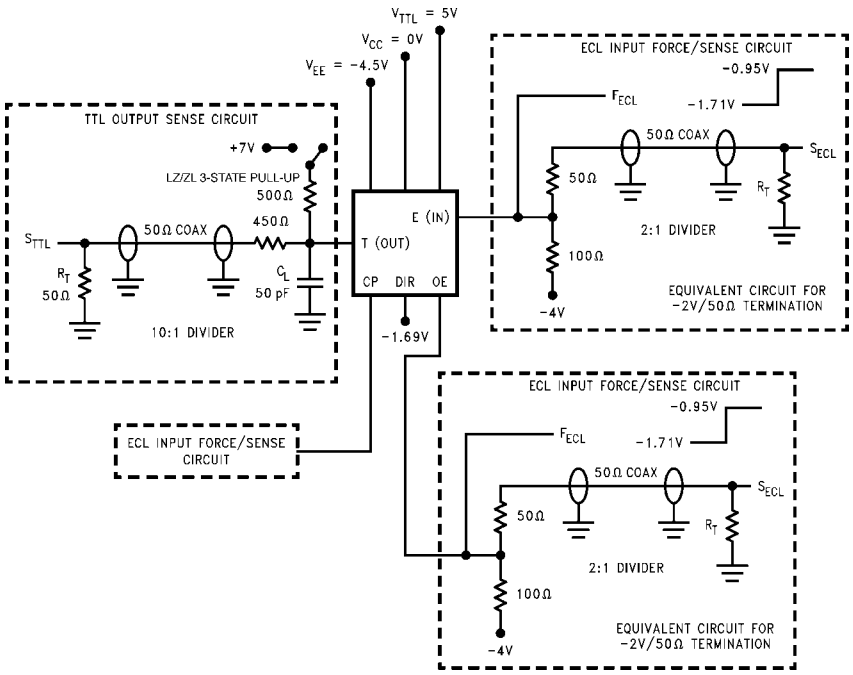


FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



Note: R_T = 50Ω termination resistive load. When an input or output is being monitored by a scope, $R_T$is supplied by the scope's 50Ω input resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

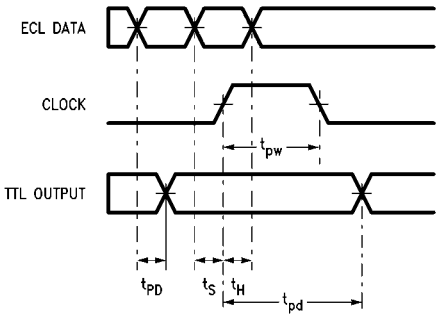
Note: The TTL 3-STATE pull-up switch is connected to +7V only for ZL and LZ tests.

Note: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note: V_{TTL} is decoupled to ground with 0.1 µF, V_{EE} is decoupled to ground with 0.01 µF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

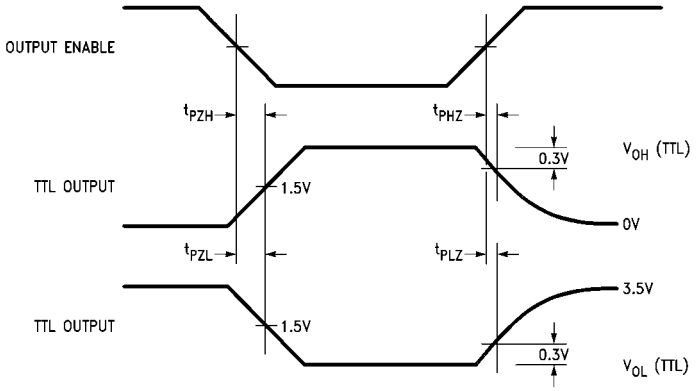
Switching Waveforms (ECL-to-TTL)



Note: DIR is LOW, OE is HIGH

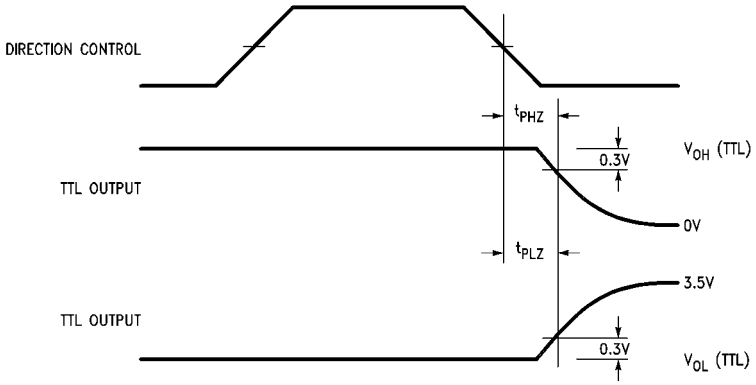
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times

Switching Waveforms (Continued)



Note: DIR is LOW

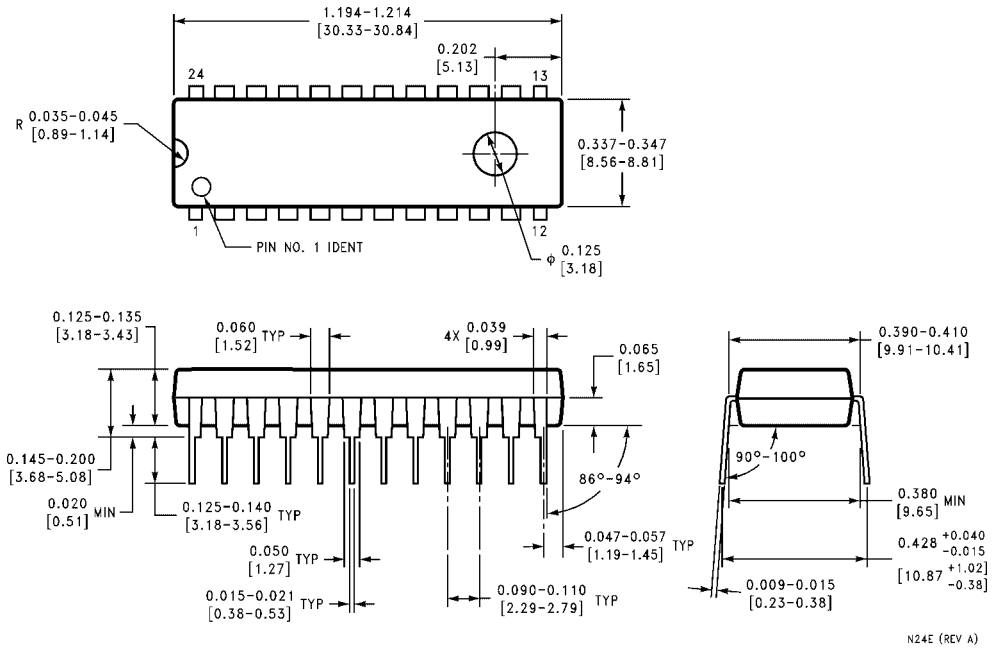
FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times



Note: OE is HIGH

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E