A5800 and A5801

BiMOS II Latched Drivers

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 2, 2005

Deadline for receipt of LAST TIME BUY orders: October 28, 2005

Recommended Substitutions:

For new customers or new applications, refer to the 6800 and 6801.

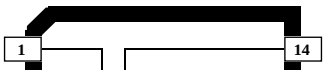
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

5800 AND 5801

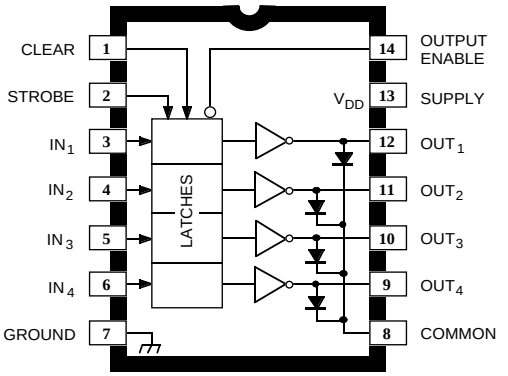
Data Sheet
26180.10B*

BiMOS II LATCHED DRIVERS

UCN5800L



UCN5800A



Dwg. PP-014A

Note the UCN5800A (DIP) and the UCN5800L (SOIC) are electrically identical and share a common terminal number assignment.

ABSOLUTE MAXIMUM RATINGS
at **+25°C Free-Air Temperature**

Output Voltage, V_{CE} . . . . . **50 V**
Supply Voltage, V_{DD} . . . . . **15 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Collector Current,
I_C . . . . . **500 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

The UCN5800A/L and UCN5801A/EP/LW latched-input BiMOS ICs merge high-current, high-voltage outputs with CMOS logic. The CMOS input section consists of 4 or 8 data ('D' type) latches with associated common CLEAR, STROBE, and OUTPUT ENABLE circuitry. The power outputs are bipolar npn Darlingtons. This merged technology provides versatile, flexible interface. These BiMOS power interface ICs greatly benefit the simplification of computer or microprocessor I/O. The UCN5800A and UCN5800L each contain four latched drivers; the UCN5801A, UCN5801EP, and UCN5801LW contain eight latched drivers.

The UCN5800A/L and UCN5801A/EP/LW supersede the original BiMOS latched-input driver ICs (UCN4400A and UCN4801A). These second-generation devices are capable of much higher data input rates and will typically operate at better than 5 MHz with a 5 V logic supply. Circuit operation at 12 V affords substantial improvement over the 5 MHz figure.

The CMOS inputs are compatible with standard CMOS and NMOS circuits. TTL circuits may mandate the addition of input pull-up resistors. The bipolar Darlington outputs are suitable for directly driving many peripheral/power loads: relays, lamps, solenoids, small dc motors, etc.

All devices have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The UCN5800A is furnished in a standard 14-pin DIP; the UCN5800L and UCN5801LW in surface-mountable SOICs; the UCN5801A in a 22-pin DIP with 0.400" (10.16 mm) row centers; the UCN5801EP in a 28-lead PLCC.

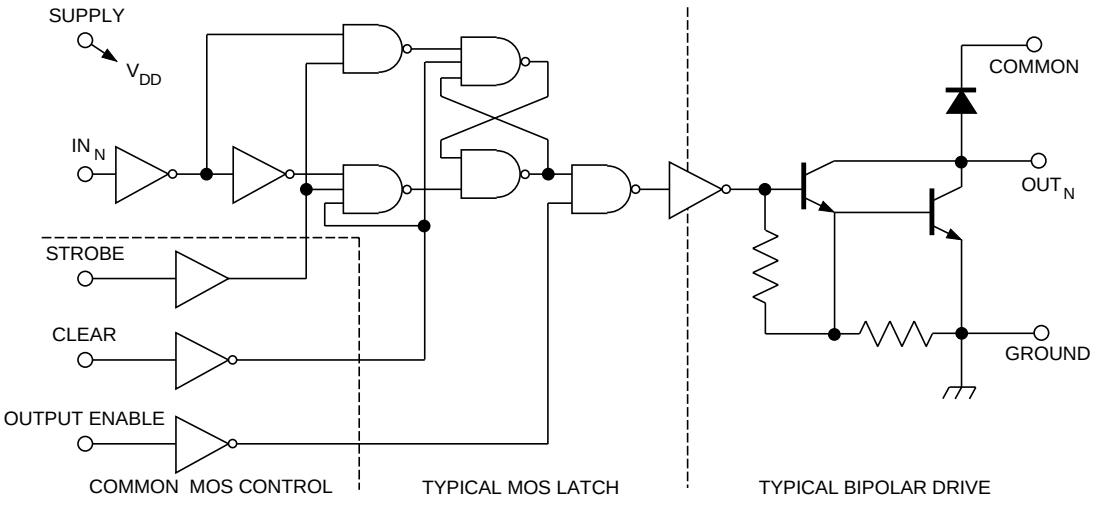
FEATURES

- To 4.4 MHz Data Input Rate
- High-Voltage, High-Current Outputs
- CMOS, NMOS, TTL Compatible Inputs
- Output Transient Protection
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Automotive Capable

Always order by complete part number, e.g., **UCN5801EP** .

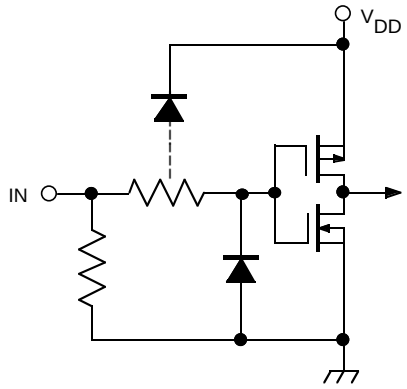
5800 AND 5801
BiMOS II
LATCHED DRIVERS

FUNCTIONAL BLOCK DIAGRAM

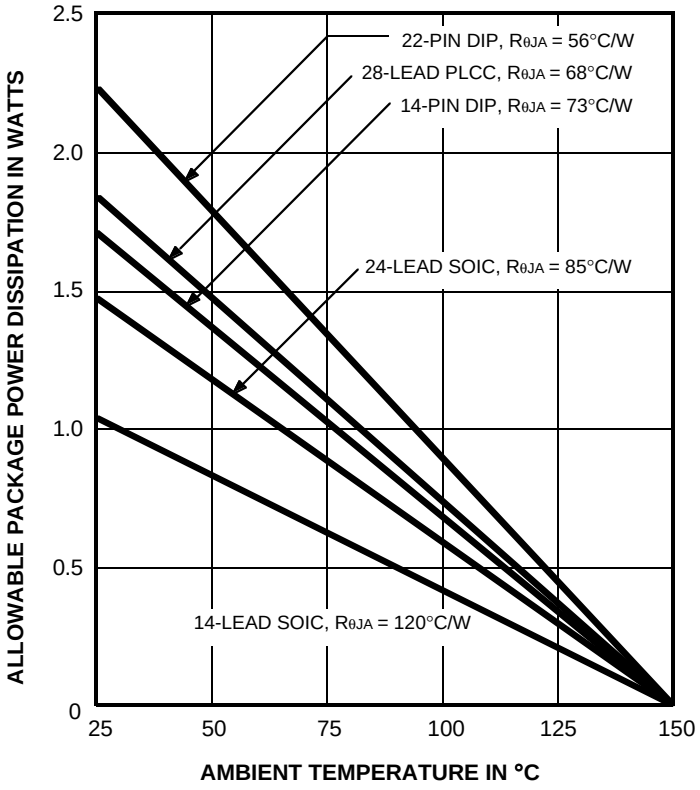


Dwg. FP-016-1

TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A



Dwg. GP-023-1A

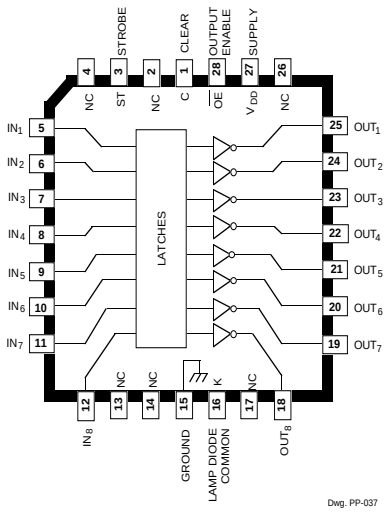
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	µA
		V_{CE} = 50 V, T_A = +70°C	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See Note)	3.5	—	—	V
Input Resistance	r_{IN}	V_{DD} = 12 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	V_{DD} = 12 V, Outputs Open	—	1.0	2.0	mA
		V_{DD} = 10 V, Outputs Open	—	0.9	1.7	mA
		V_{DD} = 5.0 V, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12 V, Outputs Open, Inputs = 0 V	—	—	200	µA
		V_{DD} = 5.0 V, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	µA
		V_R = 50 V, T_A = +70°C	—	—	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic “1”.

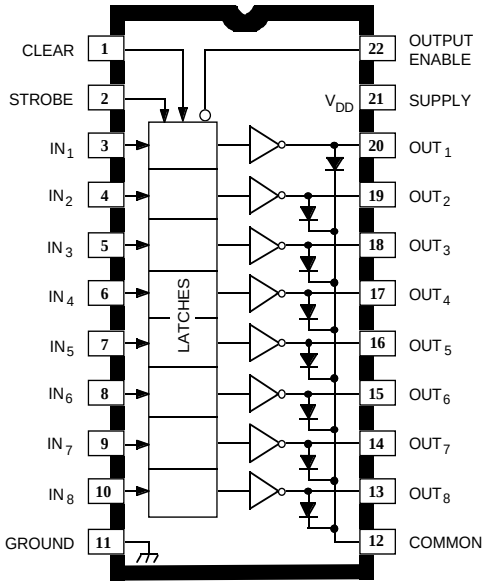
UCN5801EP

(additional pinout diagrams are on next page)



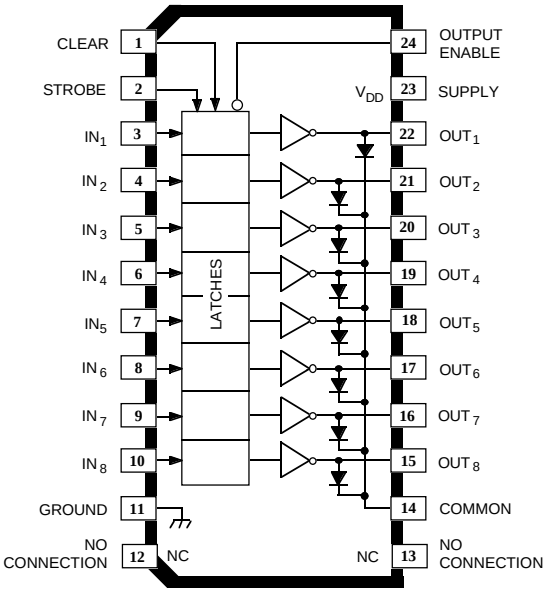
5800 AND 5801
BiMOS II
LATCHED DRIVERS

UCN5801A

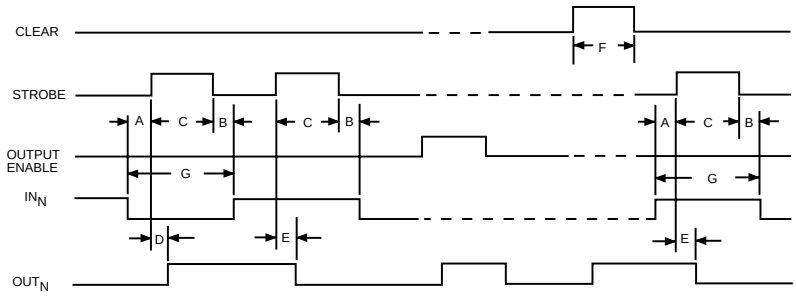


Dwg. PP-015

UCN5801LW



Dwg. PP-015-1



Dwg. No. A-10,895A

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... **50 ns**

B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... **50 ns**

C. Minimum Strobe Pulse Width ..... **125 ns**

D. Typical Time Between Strobe Activation and Output On to Off Transition ..... **500 ns**

E. Minimum Time Between Strobe Activation and Output Off to On Transition ..... **500 ns**

F. Minimum Clear Pulse Width ..... **300 ns**

G. Minimum Data Pulse Width ..... **225 ns**

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

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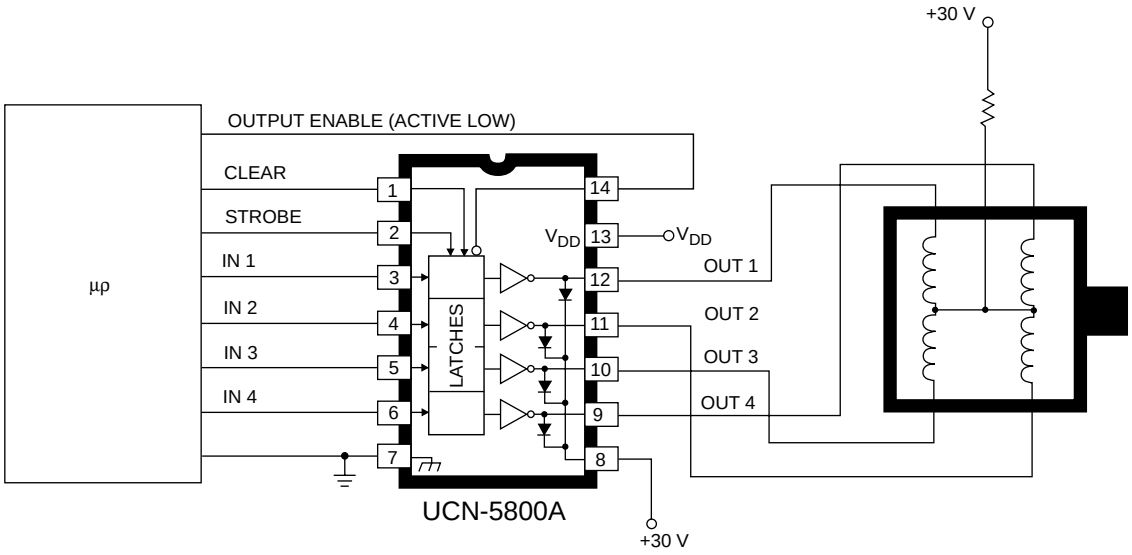
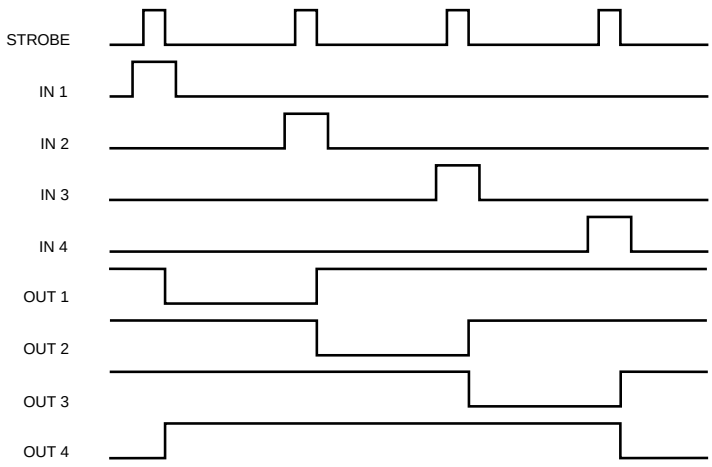
TYPICAL APPLICATION
UNIPOLAR STEPPER-MOTOR DRIVE



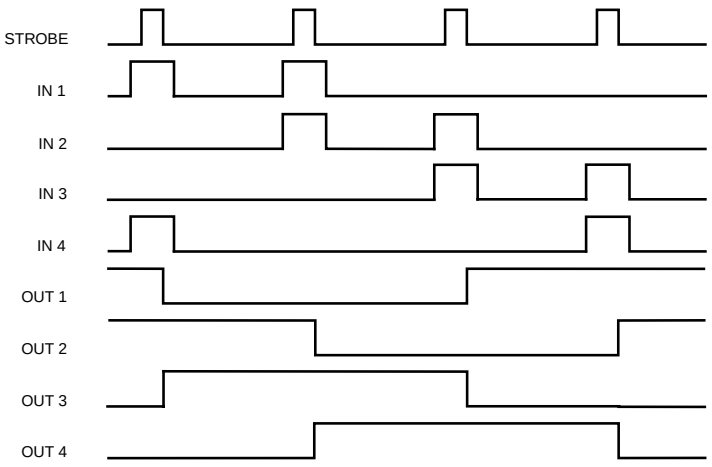
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



Dwg. GP-060

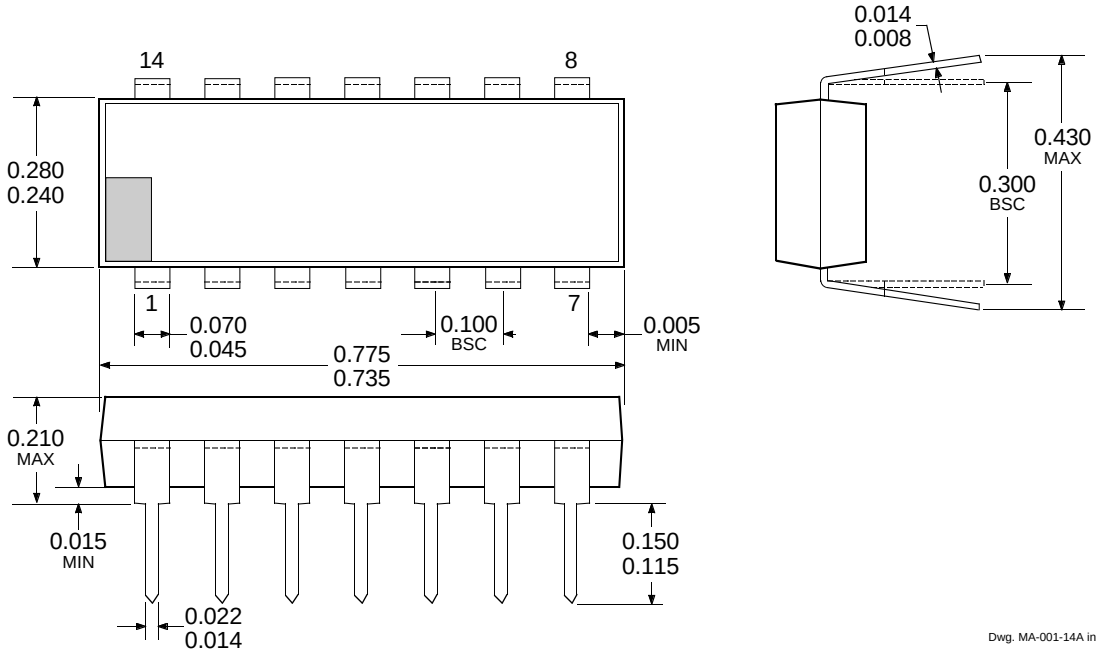
UNIPOLAR 2-PHASE DRIVE



Dwg. GP-060-1

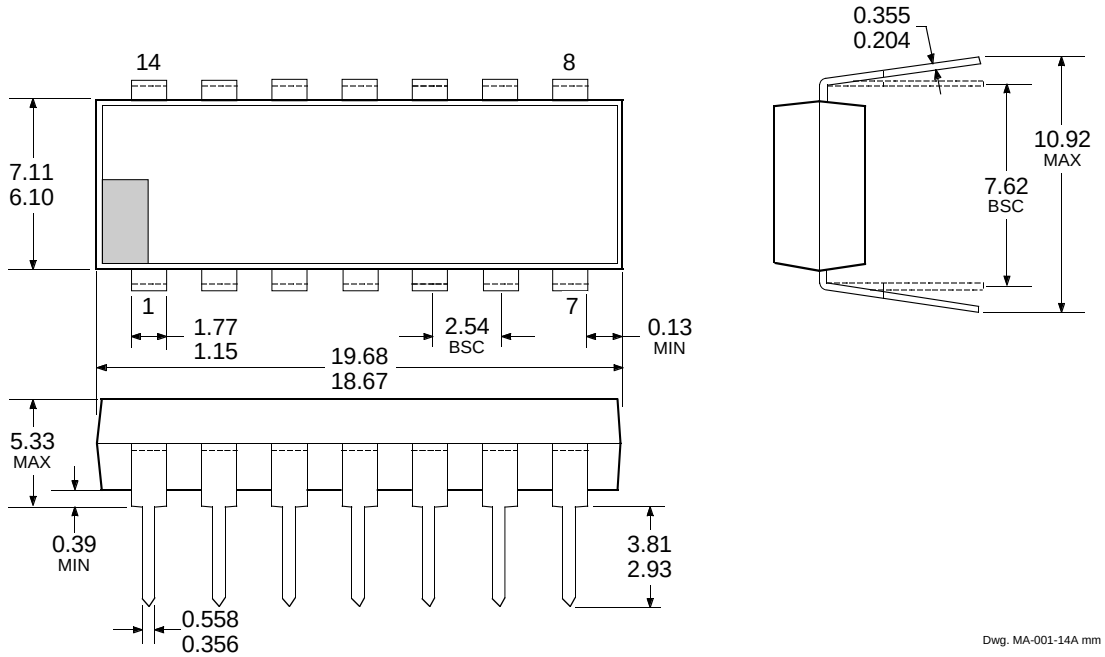
UCN5800A

Dimensions in Inches
(controlling dimensions)



Dwg. MA-001-14A in

Dimensions in Millimeters
(for reference only)

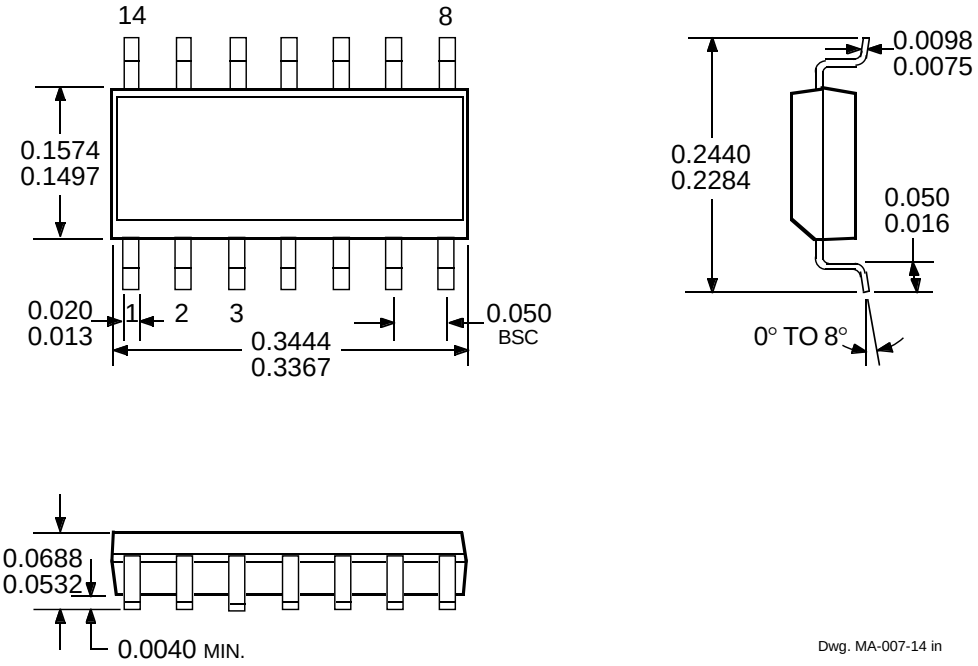


Dwg. MA-001-14A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

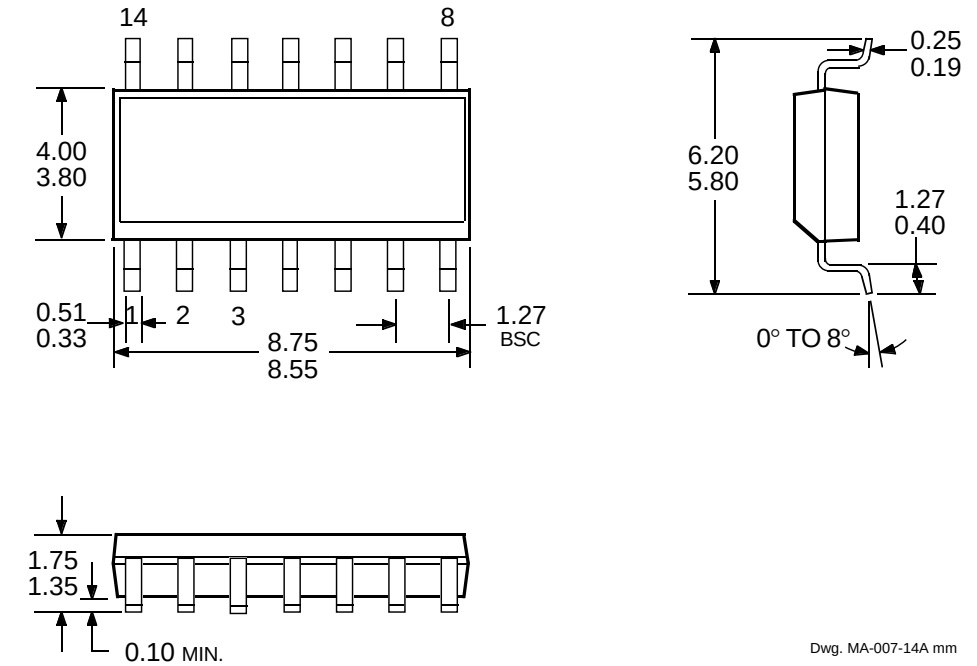
UCN5800L

Dimensions in Inches
(for reference only)



Dwg. MA-007-14 in

Dimensions in Millimeters
(controlling dimensions)

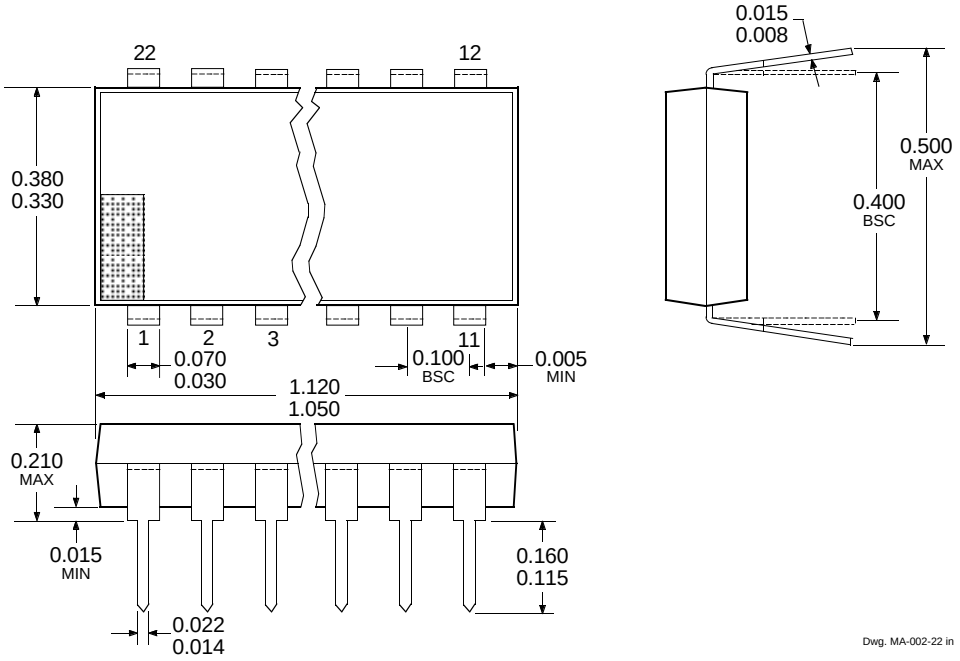


Dwg. MA-007-14A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

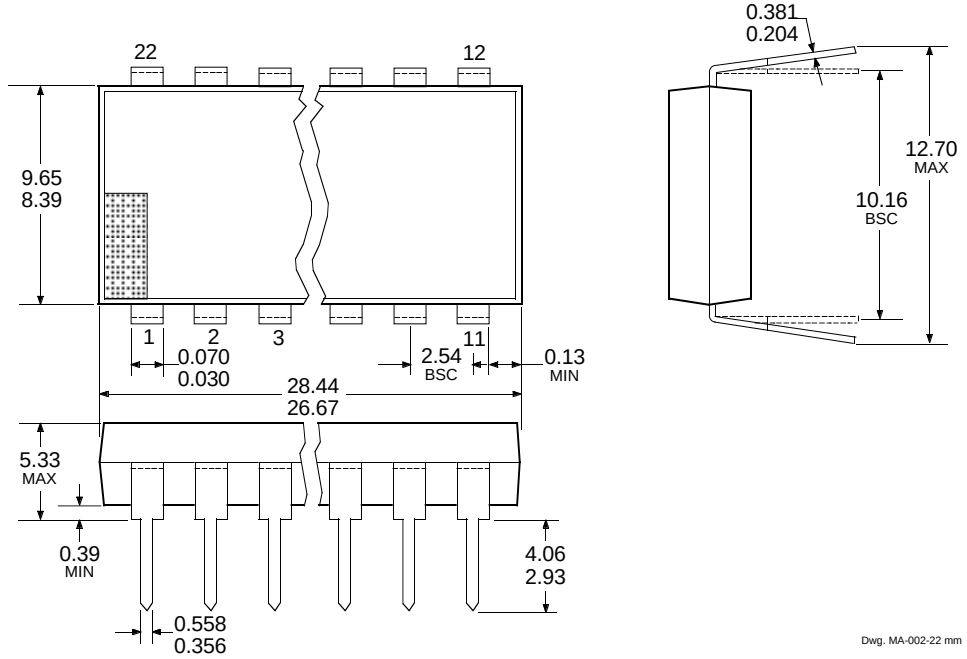
UCN5801A

Dimensions in Inches
(controlling dimensions)



Dwg. MA-002-22 in

Dimensions in Millimeters
(for reference only)

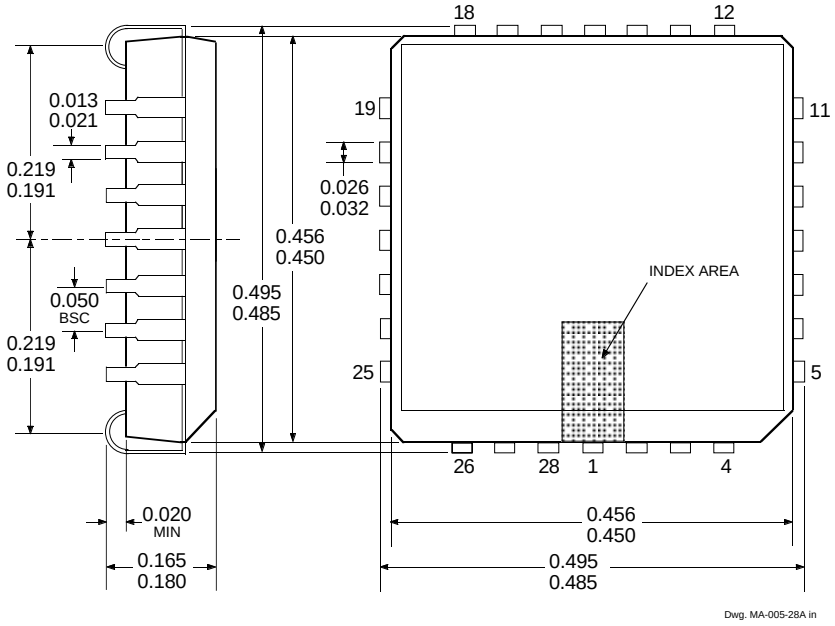


Dwg. MA-002-22 mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Lead thickness is measured at seating plane or below.

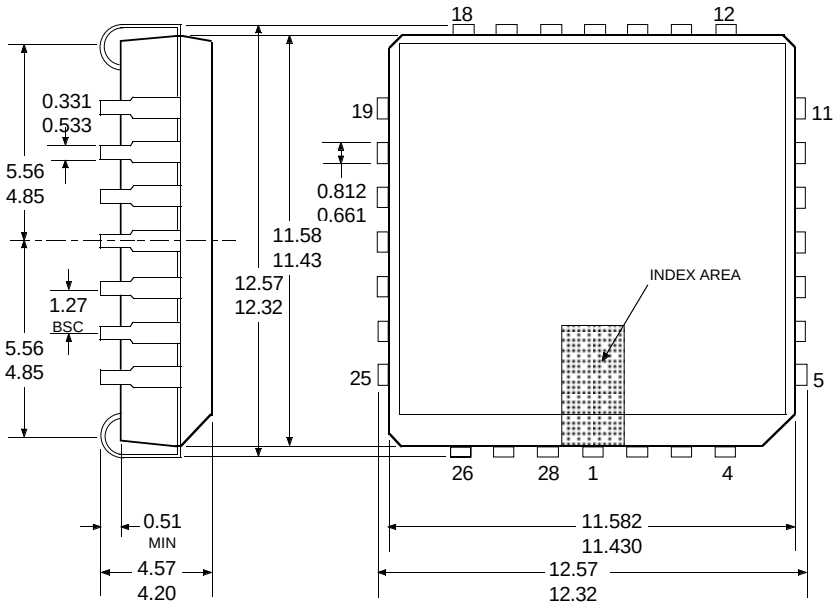
UCN5801EP

Dimensions in Inches
(controlling dimensions)



Dwg. MA-005-28A in

Dimensions in Millimeters
(for reference only)

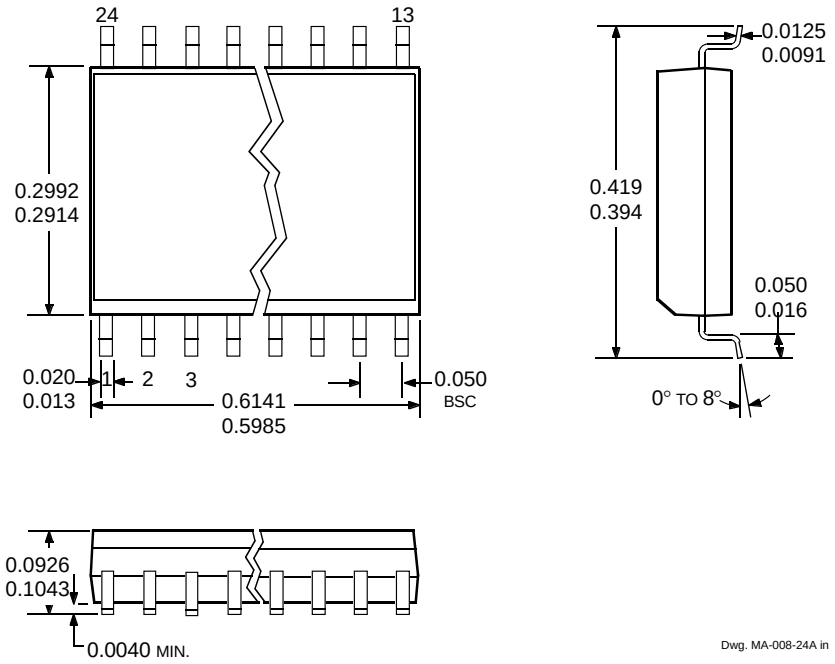


Dwg. MA-005-28A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

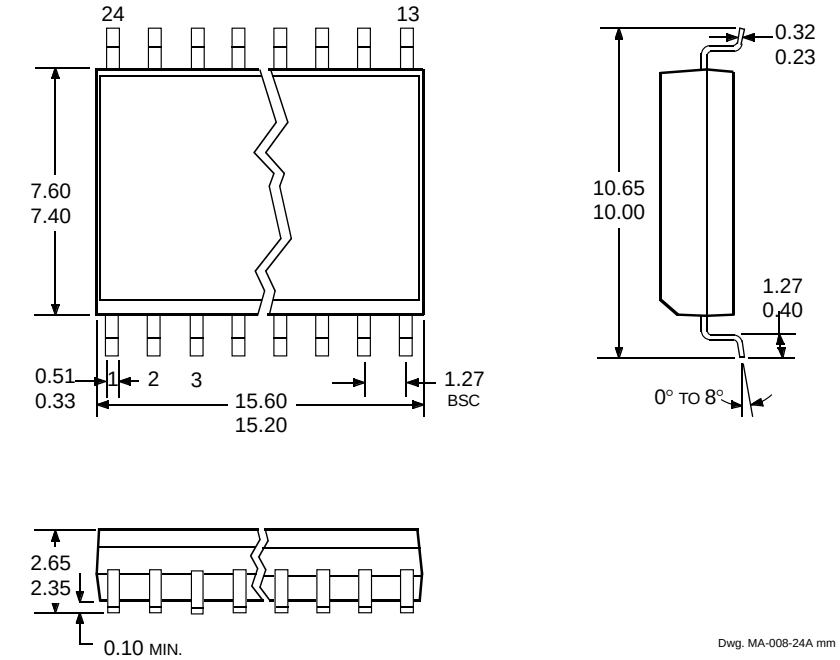
UCN5801LW

Dimensions in Inches
(for reference only)



Dwg. MA-008-24A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-24A mm

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.

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5800 AND 5801
BiMOS II
LATCHED DRIVERS

POWER INTERFACE DRIVERS

Function	Output Ratings*		Part Number†
SERIAL-INPUT LATCHED DRIVERS			
8-Bit (saturated drivers)	-120 mA	50 V‡	5895
8-Bit	350 mA	50 V	5821
8-Bit	350 mA	80 V	5822
8-Bit	350 mA	50 V‡	5841
8-Bit	350 mA	80 V‡	5842
8-Bit (constant-current LED driver)	75 mA	17 V	6275
8-Bit (constant-current LED driver)	120 mA	24 V	6277
8-Bit (DMOS drivers)	250 mA	50 V	6595
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595
8-Bit (DMOS drivers)	100 mA	50 V	6B595
10-Bit (active pull-downs)	-25 mA	60 V	6810
12-Bit (active pull-downs)	-25 mA	60 V	5811
16-Bit (constant-current LED driver)	75 mA	17 V	6276
20-Bit (active pull-downs)	-25 mA	60 V	6812
32-Bit (active pull-downs)	-25 mA	60 V	6818
32-Bit	100 mA	30 V	5833
32-Bit (saturated drivers)	100 mA	40 V	5832
PARALLEL-INPUT LATCHED DRIVERS			
4-Bit	350 mA	50 V‡	5800
8-Bit	-25 mA	60 V	5815
8-Bit	350 mA	50 V‡	5801
8-Bit (DMOS drivers)	100 mA	50 V	6B273
8-Bit (DMOS drivers)	250 mA	50 V	6273
SPECIAL-PURPOSE DEVICES			
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

‡ Internal transient-suppression diodes included for inductive-load protection.

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