A5821

BiMOS II 8-Bit Serial Input Latched Drivers

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 2, 2005

Deadline for receipt of LAST TIME BUY orders: October 28, 2005

Recommended Substitutions:

For new customers or new applications, refer to the A6821.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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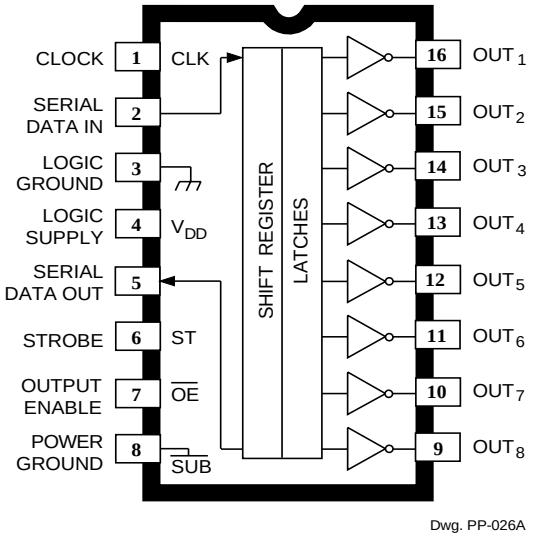
Data Sheet
26185.12F

BiMOS II 8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. PP-026A

Note the DIP package and the SOIC package are electrically identical and share common terminal number assignments.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... **50 V**
Logic Supply Voltage, V_{DD} ..... **15 V**
Input Voltage Range,
V_{IN} ..... **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} ..... **500 mA**
Package Power Dissipation, P_D
Package Code 'A' ..... **2.1 W**
Package Code 'LW' ..... **1.5 W**
Operating Temperature Range,
T_A ..... **-20°C to +85°C**
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

A merged combination of bipolar and MOS technology gives these devices an interface flexibility beyond the reach of standard logic buffers and power driver arrays. The UCN5821A and UCN5821LW each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers.

BiMOS II devices have much higher data-input rates than the original BiMOS circuits. With a 5 V logic supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS and NMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

The UCN5821A are furnished in a standard 16-pin plastic DIP; the UCN5821LW are in a 16-lead wide-body SOIC for surface-mount applications. The UCN5821A is also available for operation from -40°C to +85°C. To order, change the prefix from 'UCN' to 'UCQ'.

FEATURES

- To 3.3 MHz Data Input Rate
- CMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic & Latches
- High-Voltage Current-Sink Outputs
- Automotive Capable

Always order by complete part number, e.g., **UCN5821A**.

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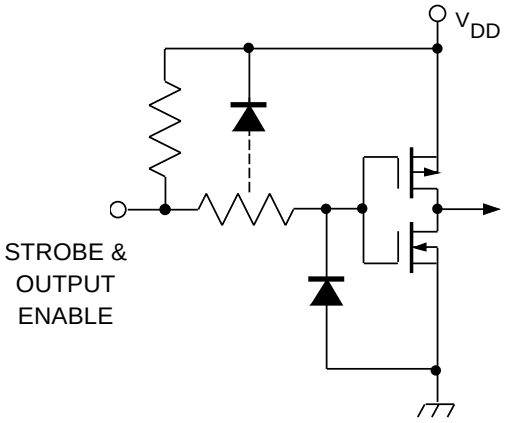
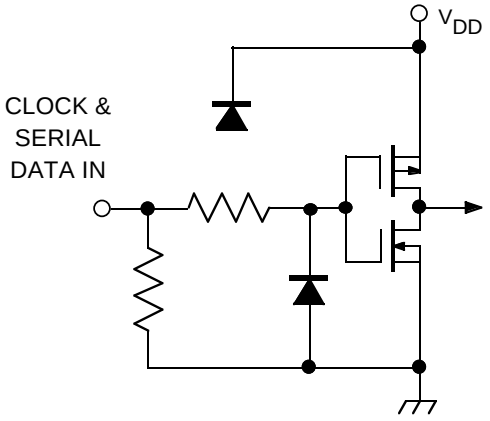
8-BIT SERIAL-INPUT, LATCHED DRIVERS

TYPICAL INPUT CIRCUITS

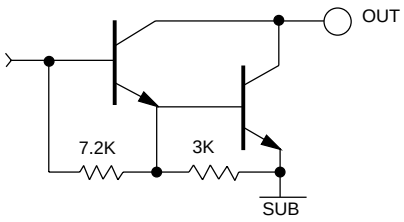


Dwg. EP-010-3



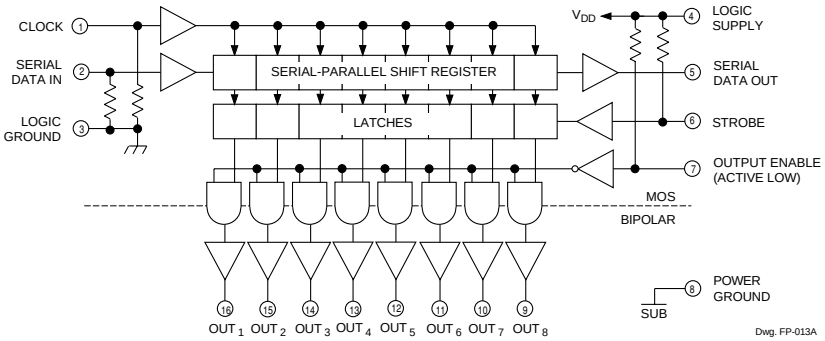
Dwg. EP-010-4A

TYPICAL OUTPUT DRIVER



Dwg. No. A-14,314

FUNCTIONAL BLOCK DIAGRAM



NOTE — There is an indeterminate resistance between logic ground and power ground. For proper operation, these terminals must be externally connected together.

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	UCN5821A Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	90%	79%	72%	65%	57%
7	100%	90%	82%	74%	65%
6	100%	100%	96%	86%	76%
5	100%	100%	100%	100%	91%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 12 V)	UCN5821LW Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	67%	59%	54%	49%	43%
7	77%	68%	62%	56%	49%
6	90%	79%	72%	65%	57%
5	100%	95%	86%	78%	68%
4	100%	100%	100%	98%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 50 V	—	50	µA
		V_{OUT} = 50 V, T_A = +70°C	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100 mA	—	1.1	V
		I_{OUT} = 200 mA	—	1.3	V
		I_{OUT} = 350 mA, V_{DD} = 7.0 V	—	1.6	V
Input Voltage	$V_{IN(0)}$		—	0.8	V
	$V_{IN(1)}$	V_{DD} = 12 V	10.5	—	V
		V_{DD} = 5.0 V	3.5	—	V
Input Resistance	r_{IN}	V_{DD} = 12 V	50	—	kΩ
		V_{DD} = 5.0 V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, V_{DD} = 12 V	—	4.5	mA
		One Driver ON, V_{DD} = 10 V	—	3.9	mA
		One Driver ON, V_{DD} = 5.0 V	—	2.4	mA
	$I_{DD(OFF)}$	V_{DD} = 5.0 V, All Drivers OFF, All Inputs = 0 V	—	1.6	mA
		V_{DD} = 12 V, All Drivers OFF, All Inputs = 0 V	—	2.9	mA

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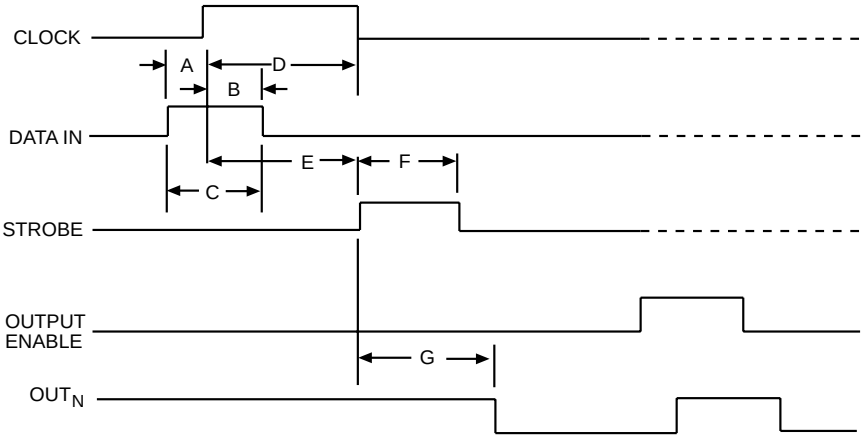
8-BIT SERIAL-INPUT, LATCHED DRIVERS



Dwg. No. A-12,627

TIMING CONDITIONS
(V_{DD} = 5.0 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **30 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

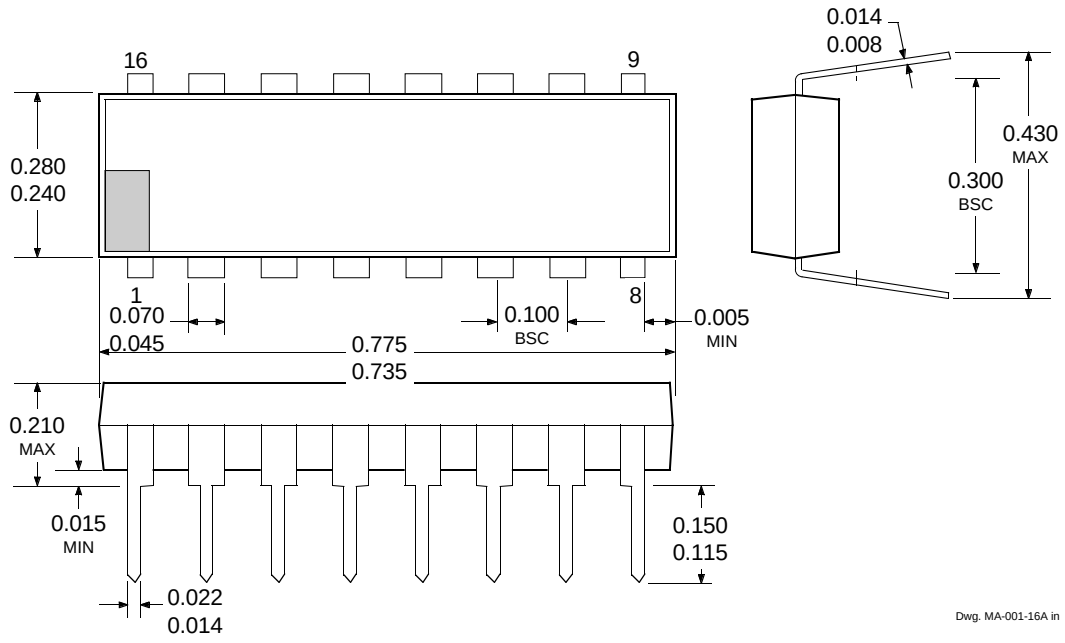
Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 ..... I_8	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 ..... I_8	Output Enable	Output Contents I_1 I_2 I_3 ..... I_8
H	⊓	H R_1 R_2 ..... R_7	R_7				
L	⊓	L R_1 R_2 ..... R_7	R_7				
X	⊔	R_1 R_2 R_3 ..... R_8	R_8				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

115 Northeast Cutoff, Box 15036

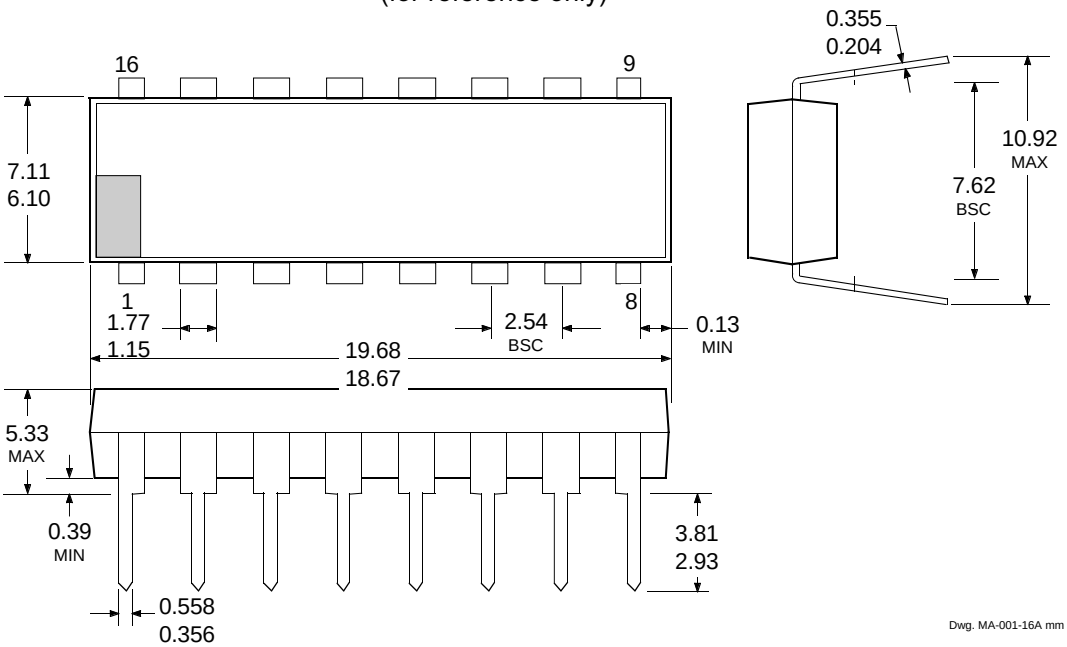
UCN5821A

Dimensions in Inches
(controlling dimensions)



Dwg. MA-001-16A in

Dimensions in Millimeters
(for reference only)



Dwg. MA-001-16A mm

NOTES: 1. Lead thickness is measured at seating plane or below.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

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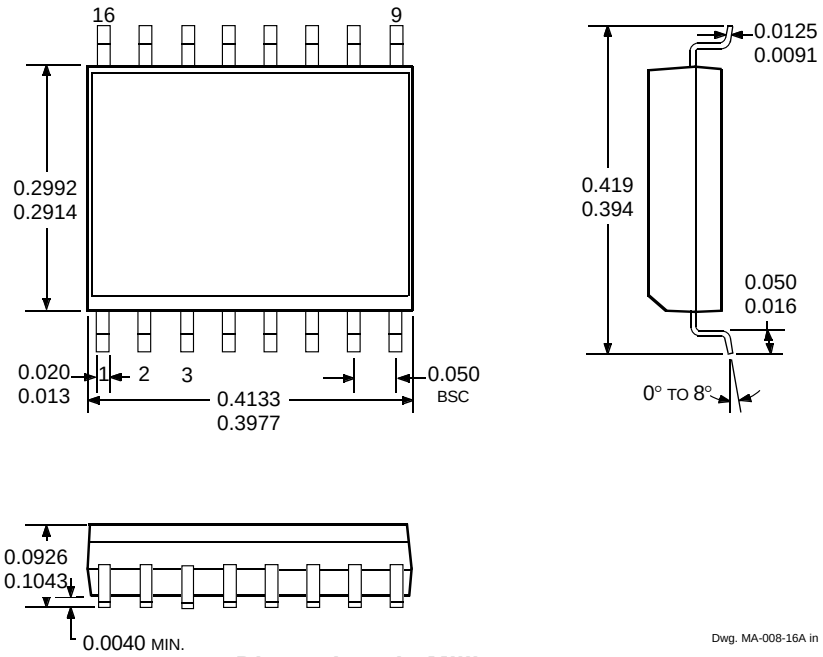
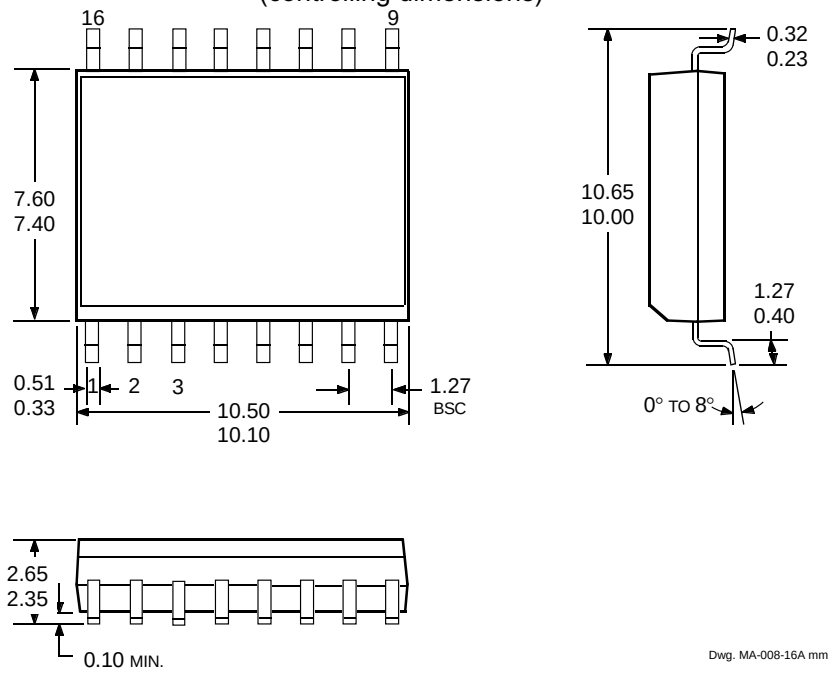
8-BIT SERIAL-INPUT, LATCHED DRIVERS

UCN5821LW
Dimensions in Inches
(for reference only)



Dwg. MA-008-16A in

Dimensions in Millimeters
(controlling dimensions)



Dwg. MA-008-16A mm

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.

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8-BIT SERIAL-INPUT, LATCHED DRIVERS