



Preliminary

A64S06161A

Document Title

16M(1M x 16bit) Normal mode & Page mode Static Random Access Memory

Revision history

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue	March 28, 2005	Preliminary



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MEMORY

16M(1M x 16bit) Normal mode & Page mode Static Random Access Memory

DESCRIPTION

The A64S06161A is a 16Mb high speed, low power Static Random Access Memory(SRAM) organized as 1,048,576 words by 16 bits and supports Page Mode.

The A64S06161A is a Pseudo SRAM based on successfully proven DRAM CELL SRAM which was specifically developed for cost sensitive, low power computing and communication applications such as mobile cellular phone handsets, personal digital assistants and other battery-operated consumer products.

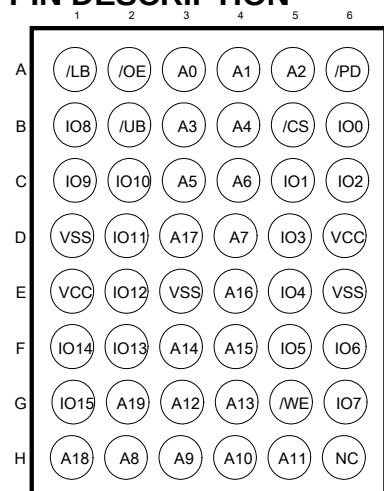
FEATURES

- Standard Asynchronous SRAM Interface and Page Mode
- Organization : 1M x 16Bit
- Power Supply Voltage : 2.7 ~ 3.3 V
- Page Size : 4 words
- Page Mode Access (tPAA) : 35ns
- Data Retention Voltage : 2.4V
- Tri-state Output and TTL Compatible

PRODUCT FAMILY

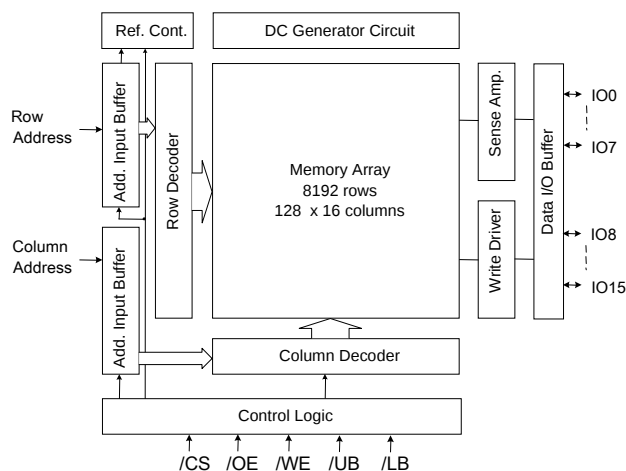
Product Family	Operating Temperature	Voltage	Speed	ISB1 (Max)	IccDR (Max)	ICC1 (Max)	Mode
A64S06161A	-40 ~ 85 °C	2.7 ~ 3.3 V	70	100uA	100uA	2.0mA	Page

PIN DESCRIPTION



Note : E3 pin (VSS) can be remain as a NC

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
/CS	Chip Select Input	VCC	Power
/OE	Output Enable Input	VSS	Ground
/WE	Write Enable Input	/UB	Upper Byte (IO8~15)
A0~A19	Address Input	/LB	Lower Byte (IO0~7)
IO0~IO15	Data Input / Output		



Preliminary

A64S06161A

PRODUCT LIST

Part Name	Function
A64S06161A-70U	16M, 48-FBGA , 70 ns, 3.0V, -40°C~85°C

ABSOLUTE MAXIMUM RATING

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to VCC+0.3 V	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-55 to 150	°C
Operating Temperature (Extended)	T _A	-40 ~ 85	°C

Note :

Stresses greater than those listed under “ABSOLUTE MAXIMUM RATINGS” may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied.

Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS	/PD	/OE	/WE	/LB	/UB	I/O 0~7	I/O 8~15	MODE	Power
H	H	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	H	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

RECOMMENDED DC OPERATING CONDITIONS ¹⁾

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage ⁽⁵⁾	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	0.8*V _{CC}	-	V _{CC} +0.2 ²⁾	V
Input Low Voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

Note :

1. T_A = -40°C to 85°C, otherwise specified.
2. Overshoot : V_{CC} + 1.0V in case of pulse width ≤ 20 ns.
3. Undershoot : -1.0V in case of pulse width ≤ 20 ns.
4. Overshoot and undershoot are sampled, not 100% tested.
5. Stable power supply required 100 us before device operation.

CAPACITANCE (T_A = 25 °C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance	V _{IO} = 0V	10	pF

Note : This parameter is sampled and not 100% tested

DC AND OPERATING CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	-1		1	uA
Output Leakage Current	I _{LO}	/CS = V _{IH} , /UB=/LB= V _{IH} or /OE=V _{IH} or /WE=V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1		1	uA
	I _{CC1}	Cycle Time = 1 us, 100%duty, I _{IO} =0mA, /CS ≤ 0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V			2.0	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty /CS = V _{IL} , V _{IN} =V _{IL} or V _{IH}			20	mA
	I _{CCP}	/CS1 = V _{IL} , CS2=V _{IH} , T _{pwc} = min Page address cycling			10	mA
Output Low Voltage	V _{OL}	I _{OL} = 2 mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.2			V
Standby Current(TTL)	I _{SB}	/CS=V _{IH} , /UB=/LB= V _{IH} , Other inputs = V _{IH} or V _{IL}			0.3	mA
Standby Current(CMOS)	I _{SB1}	/CS ≥ V _{CC} -0.2V, /UB=/LB ≥ V _{CC} -0.2V (/UB,/LB Controlled) Other inputs = 0 or V _{CC}			100	uA

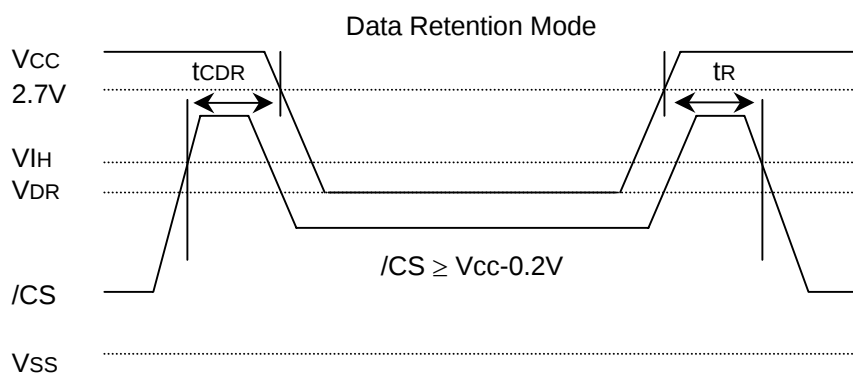
Data Retention Electric Characteristic

$T_A = -40^{\circ}\text{C}$ to 85°C (Normal), unless otherwise specified

Item	Symbol	Test Condition	Min	Typ. (1)	Max	Unit
Voltage for Data Retention	VDR	/CS=/PD= $V_{IH} > V_{CC}-0.2\text{V}$ or /UB,/LB $\geq V_{CC}-0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq V_{SS} + 0.2\text{V}$	2.4		3.3	V
Data Retention Current	IccDR	$V_{CC}=2.4\text{V}$, /CS=/PD= $V_{IH} > V_{CC}-0.2\text{V}$ or /UB,/LB $\geq V_{CC}-0.2\text{V}$, $V_{IN} \geq V_{CC}-0.2\text{V}$ or $V_{IN} \leq V_{SS} + 0.2\text{V}$			100	μA
Chip Deselect to Data Retention Time	tCDR	Refer to data retention wave form	0	-	-	ns
Operating Recovery Time	tR		tRC	-	-	ns

(1) $V_{CC} = 2.4\text{V}$, $T_A = 25^{\circ}\text{C}$

Data Retention Wave Form

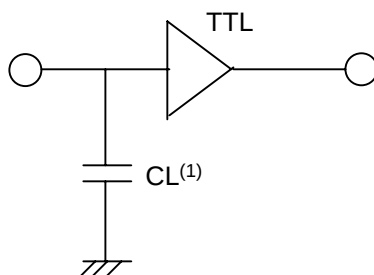


AC TEST CONDITIONS

$T_A = -40^{\circ}\text{C}$ to 85°C (Normal), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	$CL = 30\text{pF} + 1\text{TTL Load}$

AC TEST LOADS



Note : (1) Including jig and scope capacitance

POWER UP TIME

At starting, maintain stable power for a minimum 100us with /CS = /PD = high.



Preliminary

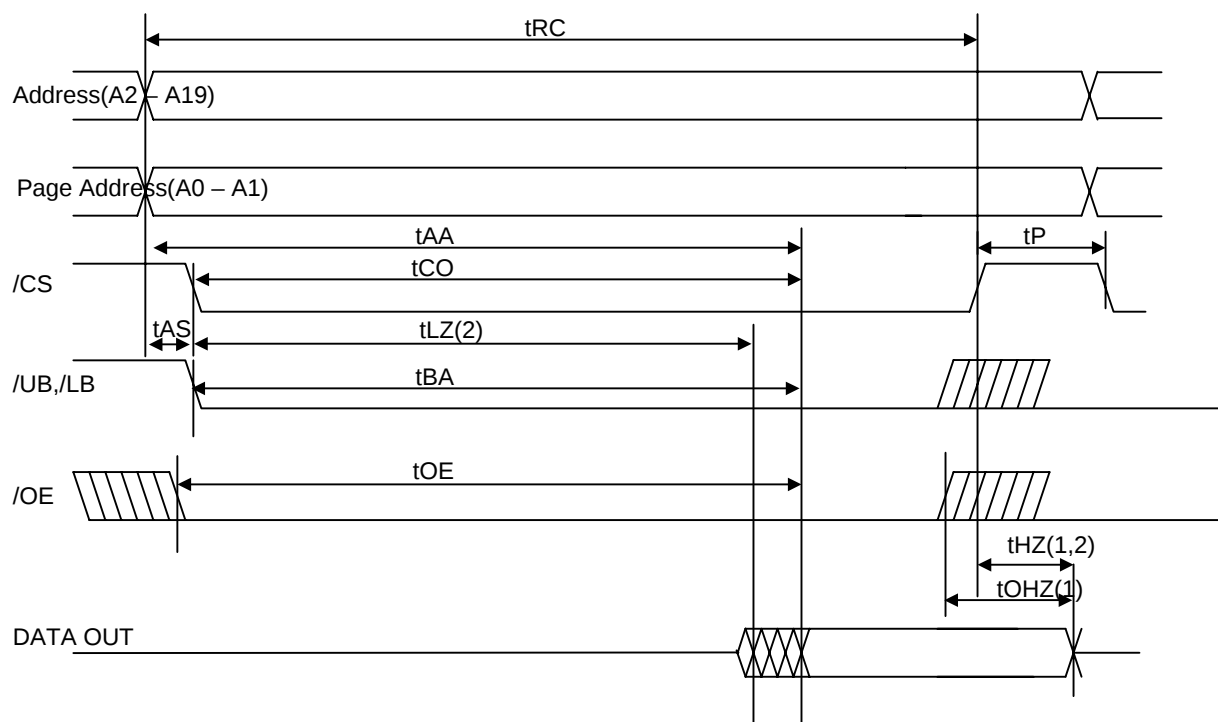
A64S06161A

AC CHARACTERISTICS (V_{CC} = 2.7 ~ 3.3V, T_A = -40 to 85°C)

Parameter List		Symbol	70ns		Unit
			Min	Max	
R E A D	Read Cycle Time	t _{RC}	70		ns
	Address Set-up Time	t _{AS}	0		ns
	Address Access Time	t _{AA}		70	ns
	Chip Select to Output	t _{CO}		70	ns
	Output Enable to Valid Output	t _{OE}		35	ns
	/UB, /LB Access Time	t _{BA}		70	ns
	Chip select to Low-Z Output	t _{LZ}	10		ns
	/UB, /LB Enable to Low-Z Output	t _{BLZ}	10		ns
	Output Enable to Low-Z Output	t _{OLZ}	5		ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	ns
	/UB, /LB Disable to High-Z Output	t _{BHZ}	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	ns
	Output Hold from Address Change	t _{OH}	10		ns
	Page Read Precharge Time	t _P	10		ns
	Page Read Cycle Time	t _{PRC}	35		ns
	Page Read Address Access Time	t _{PAA}		35	ns
W R I T E	Write Cycle Time	t _{WC}	70		ns
	Chip Select to End of Write	t _{CW}	60		ns
	Address Valid to End of Write	t _{AW}	60		ns
	/UB, /LB Valid to End of Write	t _{BW}	60		ns
	Write Pulse Width	t _{WP}	50		ns
	Write Recovery Time	t _{WR}	0		ns
	Write to Output High-Z	t _{WHZ}	0	20	ns
	Data to Write Time Overlap	t _{DW}	40		ns
	Data Hold from Write Time	t _{DH}	0		ns
	End of Write to Output Low-Z	t _{OW}	5		ns
	Page Write Precharge Time	t _P	10		ns
	Page Write Cycle Time	t _{PWC}	35		ns
	Page Write Data to Write Time overlap	t _{PDW}	20		ns
	Page Write Data Hold from Write Time	t _{PDH}	0		ns

TIMING DIAGRAMS

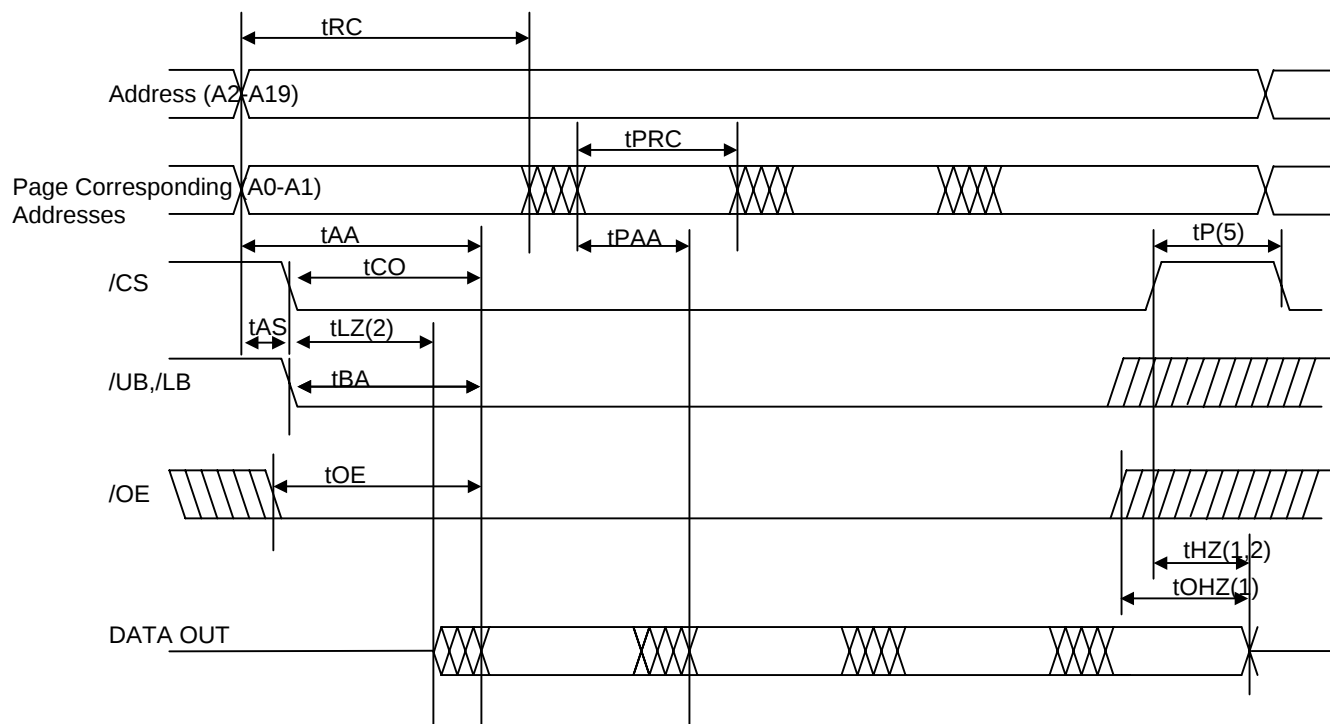
READ CYCLE (/PD = /WE = V_{IH})



Note (READ CYCLE) :

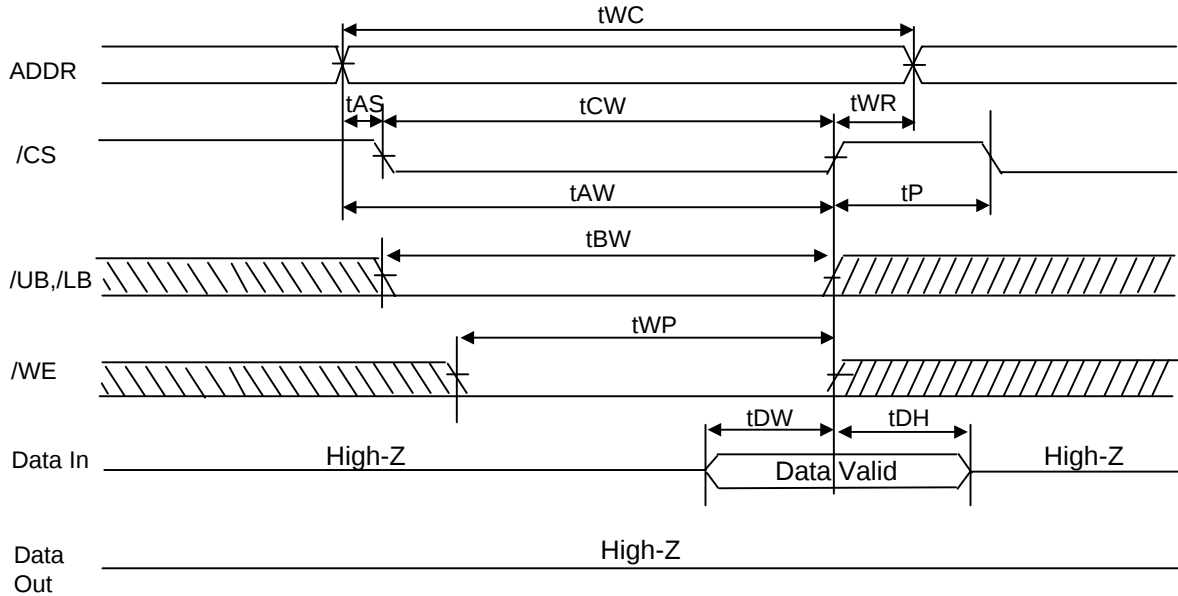
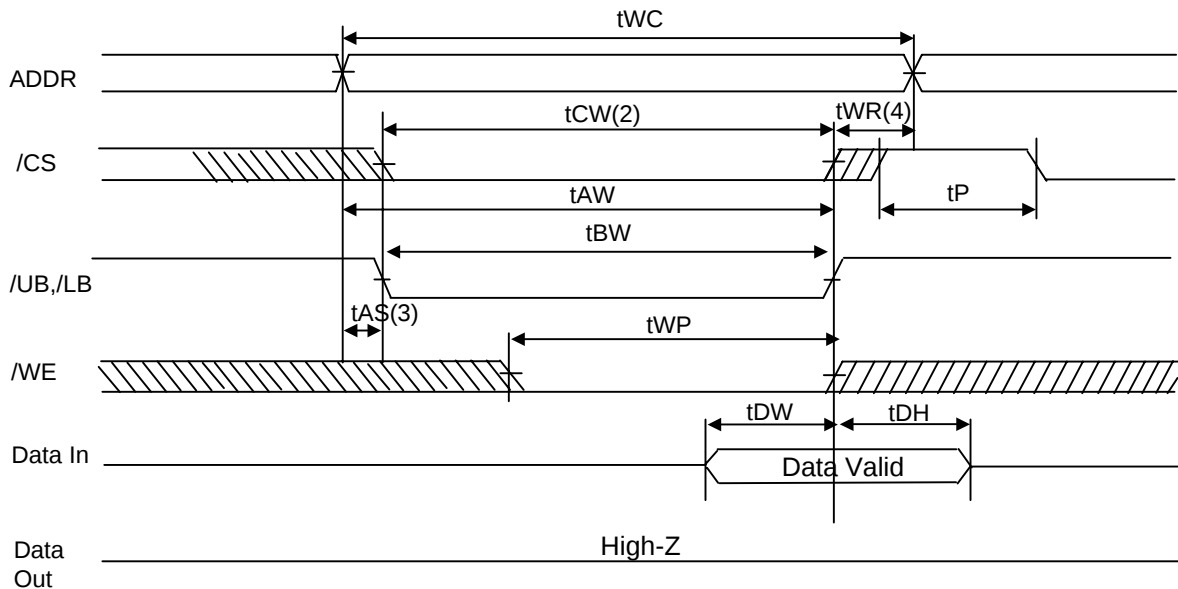
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, $t_{HZ}(\text{max.})$ is less than $t_{LZ}(\text{min.})$ both for a given device and from device to device.
3. /WE is high for the read cycle.
4. Do not access device with cycle timing shorter than t_{RC} for continuous periods > 16 μ s.

PAGE READ CYCLE (/PD = /WE = V_{IH})



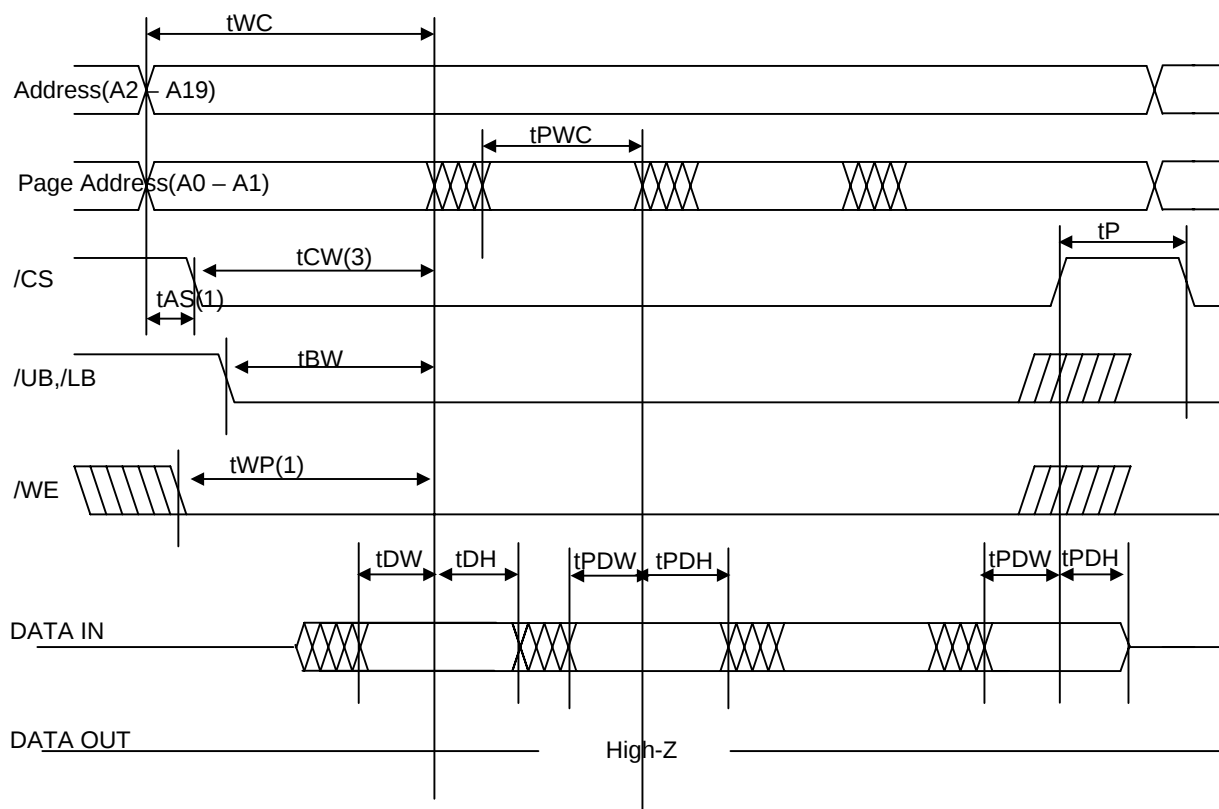
Note (PAGE MODE READ CYCLE) :

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tHZ(max.) is less than tLZ(min.) both for a given device and from device to device.
3. /WE is high for the read cycle.
4. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.
5. tP (precharge time) should be guaranteed for **new Address**.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page

WRITE CYCLE 1 (/CS Controlled, /PD = V_{IH})

WRITE CYCLE 2 (/UB /LB Controlled, /PD = V_{IH})

Notes (WRITE CYCLE) :

1. A write occurs during the overlap of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low: A write end at the earliest transition among /CS going high and /WE going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of /CS going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends as /CS.
5. Do not access device with cycle timing shorter than t_{RC} for continuous periods > 16us.

PAGE MODE WRITE CYCLE (/PD = V_{IH})



Notes (PAGE MODE WRITE CYCLE) :

1. A write occurs during the overlap of a low /CS and low /WE.
A write begins at the latest transition among /CS going low in initial page mode .
A write end at the earliest transition among /CS going high and **Page Address transition**.
tWP is measured from the beginning of write to the end of write in initial page access.
2. tPWC is measured from Page Address transition (After initial page access) to Page Address transition or /CS going high.
3. tCW is measured from the later of /CS going low to the end of write in initial page access.
3. tAS is measured from the address valid to the beginning of write.
4. Do not access device with cycle timing shorter than tRC for continuous periods > 16us.
5. tP (precharge time) should be guaranteed for new Page Address.
6. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page



Preliminary

A64S06161A

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Package
A64S06161AG-70	70	20	48B Mini BGA
A64S06161AG-70F	70	20	48B Pb-Free Mini BGA
A64S06161AG-70U	70	20	48B Mini BGA
A64S06161AG-70UF	70	20	48B Pb-Free Mini BGA

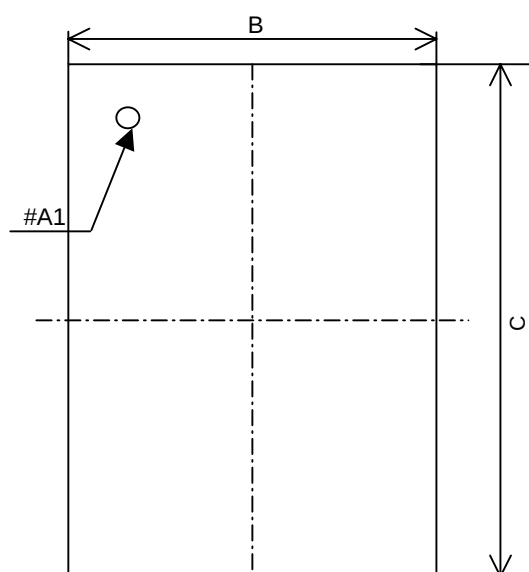
•Note : -U is for -40c ~ 85c temperature grade

PACKAGE DIMENSION FOR BGA TYPE

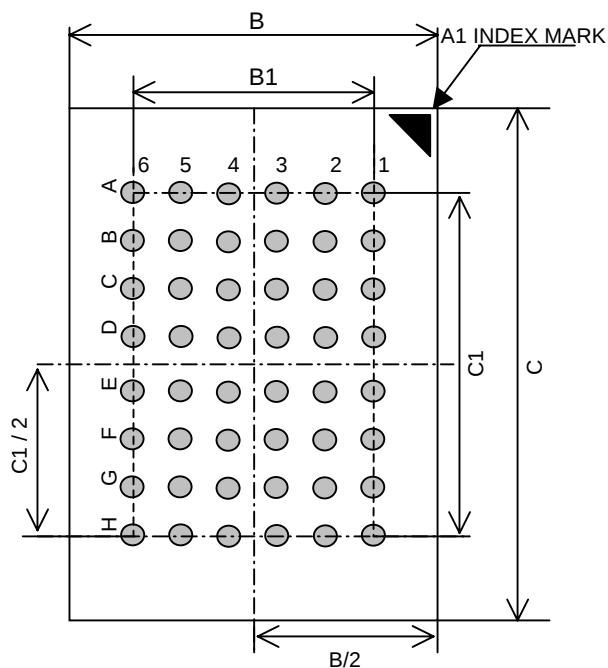
48 BALL FINE PITCH 6mm x 8mm BGA(0.75mm ball pitch)

Unit: millimeters

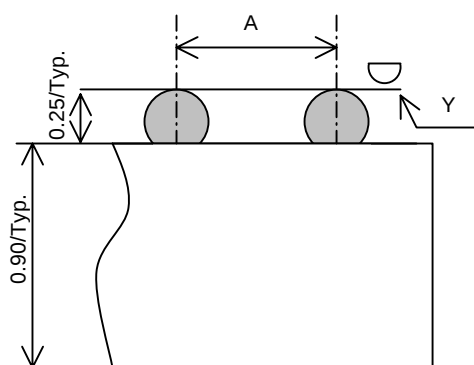
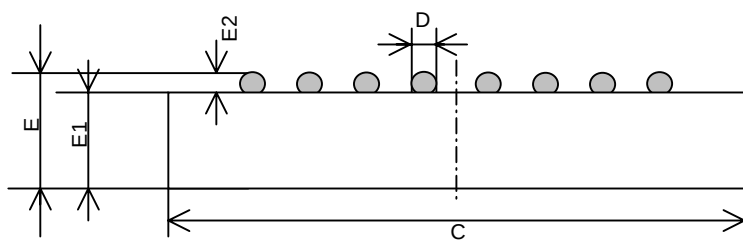
Top View



Bottom View



Side View



	Min	Typical	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	-	1.20
E1	-	-	0.90
E2	0.20	0.25	0.30
Y	-	-	0.10