

A8032 Series

Preliminary

8 Bit Microcontroller

Document Title

8 Bit Microcontroller

Revision History

Rev. No. History

0.0 Initial issue

Issue Date

Remark

November 27, 1998





Preliminary

8 Bit Microcontroller

Features

- 8-bit CMOS microcontroller
- Fully static design with power saving idle mode and power down mode
- Low standby current at full supply voltage
- Versions for 12/24/40MHz operating frequency
- On chip 256B RAM
- Four 8-bit bidirectional ports
- 64K bytes external data memory space

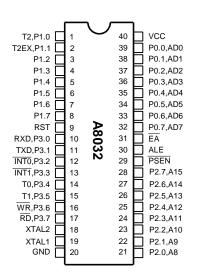
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General Description

The AMIC A8032 is a high-performance 8-bit microcontroller. It is compatible with the industry standard 80C52 microcontroller series.

Pin Configurations

■ P-DIP



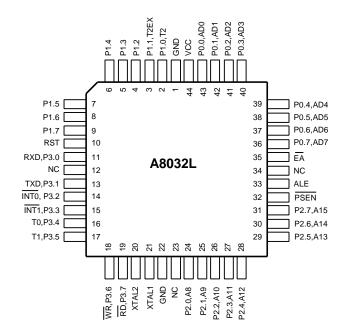
- Three 16-bit Timers/Counters (Timer 2 with up/down counter feature)
- One full duplex serial port
- Boolean processor
- Six interrupt sources, two priority levels
- Available in 40-pin P-DIP and 44-pin PLCC packages

The A8032 contains a 256B RAM, four 8-bit bidirectional parallel ports, three 16-bit timer/counters, a serial port and six interrupt sources with two priority levels.

The A8032 has supports 64KB external data memory.

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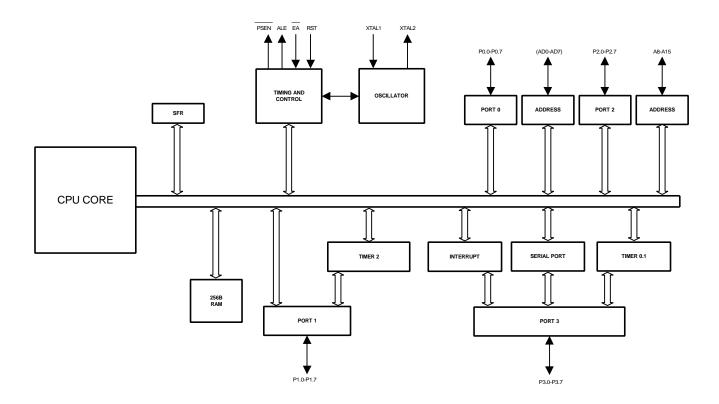
■ PLCC



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Block Diagram





Pin Description

Pin No.	Symbol	1/0	Description			
1 - 8	P1.0 - P1.7	I/O	Port1. Port1 is a bidirectional I/O port with internal pull-ups. Pin P1.0 and P1.1 also provide alternate functions as follows:			
		I/O	P1.0 T2 Timer/Counter2 external input/clock out			
		1	P1.1 T2EX Timer/Counter2 capture/reload input			
9	RST	I	Reset input, active high. It must be kept high for at least two machine cycles to be recognized by the processor			
10 - 17	P3.0 - P3.7	I/O	Port3. Port3 is a bidirectional I/O port with internal pull-ups. Port3 pins also serve alternate functions as follows:			
		I	P3.0 RXD Serial receive port			
		0	P3.1 TXD Serial transmit port			
		1	P3.2 INT0 External interrupt 0			
		1	P3.3 INT1 External interrupt 1			
		I	P3.4 T0 Timer/Counter 0 input			
		1	P3.5 T1 Timer/Counter 1 input			
		0	P3.6 WR External data memory write strobe			
		0	P3.7 RD External data memory read strobe			
18	XTAL2	0	Crystal2. This is the output of crystal oscillator. It is the inversion of XTAL1			
19	XTAL1	I	Crystal1. This is the input of crystal oscillator. It can be driven by an external clock			
20	GND	1	Ground			
21 - 28	P2.0 - P2.7	I/O	Port2. Port2 is a bidirectional I/O port with internal pull-ups. Port2 is also the multiplexed upper-order address bus during accesses to external data memory			
29	PSEN	0	Program Store Enable, active low. The read strobe to external program memory. PSEN is activated in each machine cycle when fetching external program memory			
30	ALE	0	Address latch enable, active high. ALE is used to enable the address latch that separates the data on Port 0			
31	ĒĀ	I	External Access enable, active low. It is held low to enable the device to fetch code from external program memory			
32 - 39	P0.7 - P0.0	I/O	Port0. Port0 is an open drain, bidirectional I/O port. Port0 is also the multiplexed low-order address bus during accesses to external data memory			
40	VCC	1	Power supply			



Functional Description

The A8032 is a high speed 8-bit microcontroller. The architecture consists of a core controller, four general purposes I/O ports, 256 bytes RAM internal register and a serial port.

This microcontroller supports 111 opcodes and executes instructions in a 6-clock bus cycle. It can reference both a 64K program address space and a 64K data storage space.

Timer/Counter 0, 1 and 2

Timer 0,1 and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0. TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TMOD and TCON registers support control function for Timer 0 and Timer 1. The T2CON register provides control function for Timer 2. When operating reload/capture mode, RCAP2H and RCAP2L will be used.

Interrupt

The A8032 provides 6 interrupt modes. These consist of 2 external interrupts, 3 internal interrupts and a serial port interrupt.

The enable/disable interrupt is controlled by IE register in SFR.

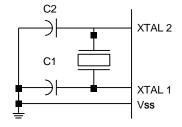
The priority of interrupts is controlled by IP register in SFR.

Serial Port Transfer

The A8032 provides a full duplex serial transfer function. This function is controlled by SCON register in SFR. And the data is storaged in SBUF register during transmitting and receiving.

Oscillator Characteristics

The oscillator connections are shown as Figure 1. And Figure 2. When quartz crystal is used, C1 and C2 are 30pF shown in Figure 1. When external clock is used, the internal clock will be gotten through a divide-by-two flip-flop. When starting up, the input loading for XTAL1 pin is 100pF. This is due to interaction between the amplifier and its feedback capacitance interaction. After the external signal meets the VIL and VIH specification the capacitance will not exceed 20pF.



C1,C2 = 30pF ± 10pF for Crystals

Figure 1. Oscillator Connections

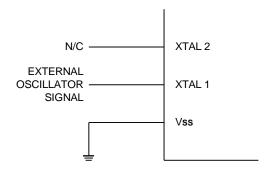


Figure 2. External Clock Drive configuration

RESET

The external reset signal must be held high for at least two machine cycles during the oscillator running. After reset, the ports are held high, SP register to 07H, all of the other SFR registers except SBUF to 00H, and SBUF is not reset.



Recommended DC Operating Conditions ($T_A = -25^{\circ}C$ to + $85^{\circ}C$)

Symbol	Parameter	Min.	Тур.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
Vıн*	Input High Voltage	2.4	-	VCC+0.2	V
VIL	Input Low Voltage	0	-	0.8	V

^{*} XTAL1 is a CMOS input. RESET is a Schmit trigger input. The min. of Viн is 3.5 Volts for these two pins.

Absolute Maximum Ratings*

VCC to GND
IN, IN/OUT Volt to GND0.5V to VCC + 0.5V
Operating Temperature, Topr25°C to + 85°C
Storage Temperature, Tstg55°C to + 125°C
Power Dissipation 1*, Pr
Soldering Temperature & Time 260°C, 10sec

1*: Operating frequency is 40MHz

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics ($T_A = -25^{\circ}C$ to + $85^{\circ}C$, $VCC = 5V \pm 10\%$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
	Input Leakage Current	-	10	μΑ	Vin = GND to VCC
110	Output Leakage Current	-	10	μΑ	Vvo = GND to VCC
lcc	Operating Current	-	50	mA	foper = 40MHz External oscillator is on XTAL1 pin No load
Vol1	Output Low Voltage (PORT1, PORT2 and PORT3)	-	0.45	V	loL = 2mA
Vol2	Output Low Voltage (ALE, PSEN and PORT0)	-	0.45	V	IoL = 4mA
Vон1	Output High Voltage (PORT1, PORT2 and PORT3)	2.4	-	V	Іон = -100μΑ
Voн2	Output High Voltage (ALE, PSEN and PORT0)	2.4	-	V	Іон = -400μА
C ₁	Input Pin Capacitance	-	10	pF	1MHz, 25°C

^{1.} For RESET pin, the | Lu | max. is 300 μA , since it has an internal pull-low of approx. 30K Ω resistor.



AC Characteristics (T_A = -25°C to + 85°C, VCC = 5V \pm 10%)

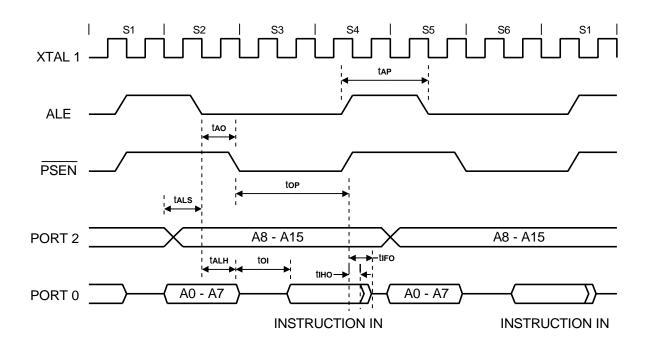
tcк3 Clock Period 25 - ns tcкн4 Clock High Time 10 - ns tcкt4 Clock Low Time 10 - ns Data Memory Cycle tpR RD Pulse Width 6tck - 20¹ - ns tpD RD Low to Valid Data in - 4tck ns tDHR Data Hold from RD High 0 2tck ns tDFR Data Float from RD High 0 2tck ns tAR ALE Low to RD Low 3tck 3tck + 20¹ ns tWP WR Pulse Width 6tck - 20¹ - ns tDHW Data Hold from WR Low 1tck - ns tDHW Data Hold from WR High 1tck - ns tAW ALE Low to WR Low 3tck 3tck + 20¹ ns Serial Port Cycle tsck Serial Port Clock 12tck - ns tki Clock Rising Edge to Valid Input Data - 11tck ns	Symbol	Parameter	Min.	Max.	Unit
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tıкн Input Data to Serial Clock Rising Clock Hold Time 0 - ns	tscĸ	Serial Port Clock	12tck	-	ns
	tкı	Clock Rising Edge to Valid Input Data	-	11tck	ns
toks Output Data to Serial Clock Rising Edge Setup Time 11tck - ns	tıкн	Input Data to Serial Clock Rising Clock Hold Time	0	-	ns
2 st.p. 2 st.s. 2 st.s. 1 st.s	toks	Output Data to Serial Clock Rising Edge Setup Time	11tck	-	ns
tокн Output Data to Serial Clock Rising Edge Hold Time 1tck - ns	tокн	Output Data to Serial Clock Rising Edge Hold Time	1tck	-	ns

- 1. This 20 ns is due to buffer driving delay and wire loading.
- 2. Instruction cycle time is 12 tck.
- 3. tck = 1/foper
- 4. There are no duty cycle requirements on the XTAL1 input.

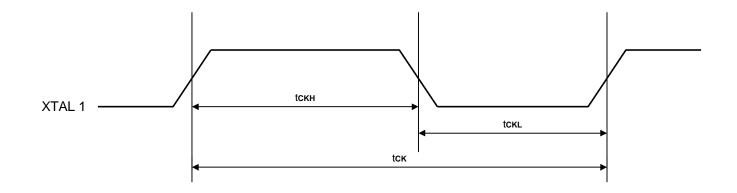


Timing Waveforms

Program Memory Cycle



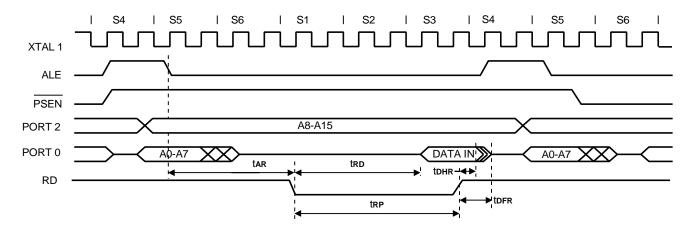
Clock Input Waveform



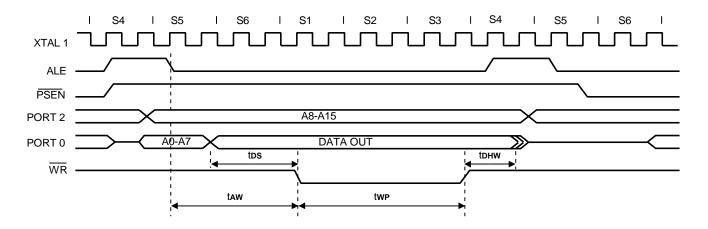


Timing Waveforms (continued)

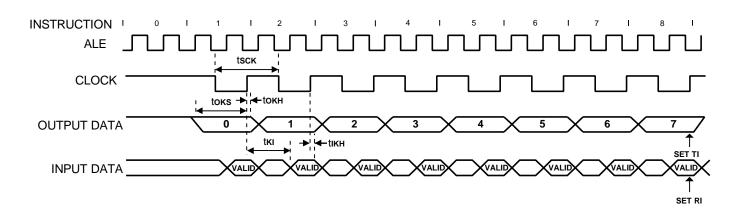
Data Memory Read Cycle



Data Memory Write Cycle



Serial Port Timing - Shift Register Mode





Ordering Information

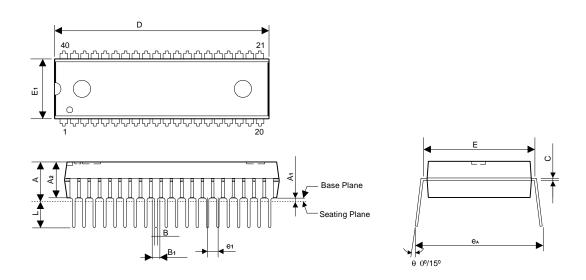
Part No.	RAM	FREQ (MHz)	Package
A8032-12	256 Byte	12	40L P-DIP
A8032L-12	256 Byte	12	44L PLCC
A8032-24	256 Byte	24	40L P-DIP
A8032L-24	256 Byte	24	44L PLCC
A8032-40	A8032-40 256 Byte		40L P-DIP
A8032L-40	256 Byte	40	44L PLCC

unit: inches/mm



Package Information

P-DIP 40L Outline Dimensions



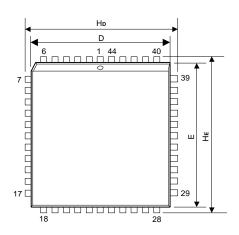
Symbol	Dimensions in inches			Dimensions in mm				
Symbol	Min	Nom	Max	Min	Nom	Max		
Α	-	-	0.210	-	-	5.344		
A1	0.015	-	-	0.381	-	-		
A2	0.150	0.155	0.160	3.810	3.937	4.064		
В	(0.018 TYP			0.457 TYP			
B1	0.050 TYP			1.270 TYP				
С	-	0.010	-	-	0.254	=		
D	2.049	2.054	2.059	52.045	52.172	52.299		
Е	0.590	0.600	0.610	14.986	15.240	15.494		
E1	0.542	0.547	0.552	13.767	13.894	14.021		
e 1	0.100 TYP			:	2.540 TYF	•		
L	0.120	0.130	0.140	3.048	3.302	3.556		
еа	0.622	0.642	0.662	15.799	16.307	16.815		

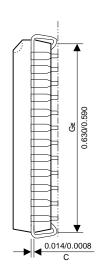
- The maximum value of dimension D includes end flash.
 Dimension E₁ does not include resin fins.



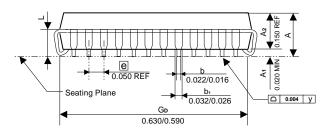
Package Information

PLCC 44L Outline Dimension





unit: inches/mm



	Dimensions in inches			Dimensions in mm		
Symbol	Min	Nom	Max	Min	Nom	Max
А	-	-	0.185	-	-	4.70
D	0.648	0.653	0.658	16.46	16.59	16.71
Е	0.648	0.653	0.658	16.46	16.59	16.71
Hd	0.680	0.690	0.700	17.27	17.53	17.78
HE	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
θ	0°	-	10°	0°	-	10°

Notes:

- 1. Dimensions D and E do not include resin fins.
- 2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.