查询AD208BY供应商 捷多邦，专业PCB打样工厂，24小时加急出货

ANALOG DEVICES

High Precision, Low Offset, mV Input Isolation Amplifier

AD208

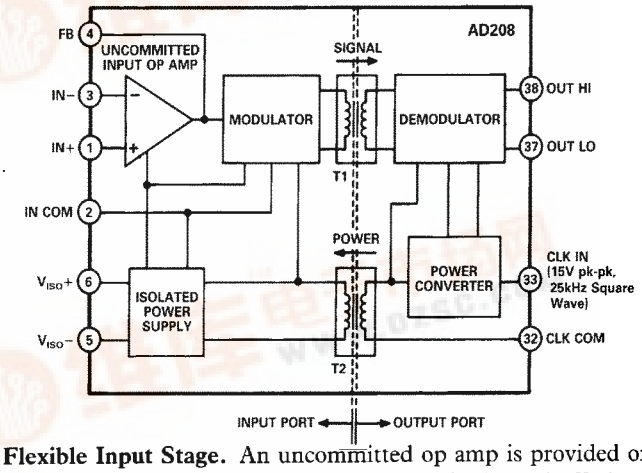
FEATURES

Wide Gain Range: 1 to 1000 V/V
Low Nonlinearity: ±0.0125%
Low Input Offset Voltage: ±0.27 mV, max (G = 1000 V/V)
Low Offset Drift: ±1.5 μV/°C , max (G = 1000 V/V)
High CMV Isolation: 1.5 kV RMS (B Grade)
Isolated Power: ±8.0 V DC with up to ±5 mA
Completely Compatible with the AD204 SIP
Small SIP: 2.08″ (52.8 mm) × 0.26″ (6.6 mm) × 0.625″ (15.9 mm)
Performance Rated over −40°C to +85°C

APPLICATIONS

Isolated RTD and Thermocouple Applications
mV Signal Amplification and Isolation
Process Instrumentation and Control
Multichannel Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD208 is a high precision, two-port, transformer-coupled isolation amplifier expressly designed for applications that require the amplification and isolation of extremely low level (i.e., ±mV) signals. The innovative front-end circuit design of the AD208 ensures the low offset characteristics and stable high gain properties of the AD208. The AD208 is fully compatible with the SIP style packaging of Analog Devices' low cost AD204 family of isolation amplifiers.

The AD208 provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD208, powered by an externally supplied 15 V pk–pk, 25 kHz clock or the recommended AD246 Clock Driver, eliminates the need for a user supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD208 emphasizes maximum flexibility and ease of use in a broad range of applications where low level signals must be measured and transmitted under high CMV conditions. The AD208 has a ±5 V output range, an adjustable gain range of from 1 to 1,000 V/V and a front-end power supply of ±8.0 V dc with up to ±5 mA of current drive capability.

PRODUCT HIGHLIGHTS

Wide Gain Range. The AD208 features a wide adjustable gain range of from 1 to 1,000 V/V. The stable high gain properties of the AD208 allow for the amplification and isolation of signals in the ±mV range.

Flexible Input Stage. An uncommitted op amp is provided on the input stage of the AD208. This allows for input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current inputs.

High Accuracy. Exhibiting a typical nonlinearity of ±0.0125% and a low gain temperature coefficient, averaging ±35 ppm/°C over the rated temperature range, the AD208 provides high isolation without loss of signal integrity and quality.

Low Offset Characteristics. With a maximum initial offset of ±(0.25 + 15 /G)mV and a maximum offset drift of ±(1.5 + 20 /G) μV/°C, the AD208 is the ideal isolation amplifier solution when low level, ±mV, signals must be measured and processed.

Excellent Common Mode Performance. The AD208BY provides 1.5 kV rms of common mode protection. Both grades of the AD208 feature a low common mode capacitance of 5.0 pF, inclusive of power isolation, that results in a typical common mode rejection specification of 100 dB (1 kΩ source impedance imbalance) as well as a low leakage current of 2.0 μA rms (max @ 240 V rms, 60 Hz).

Isolated Power. An isolated ±8.0 V dc power supply with the capability of delivering typically up to ±5 mA is available at the input port of the AD208. This permits the isolator to power floating signal conditioners, front-end amplifiers or remote transducers at the input.

Performance Rated Over the −40°C to +85°C Temperature Range. With its performance rated over the −40°C to +85°C temperature range the AD208 is an ideal isolation amplifier for use in industrial environments.

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
West Coast 714/641-9391 Central 214/231-5094 Atlantic 215/643-7790

AD208–SPECIFICATIONS

(typical @ +25°C, Output Load ≥ 1 MΩ, V_S = 15 V pk–pk, 25 kHz square wave unless noted otherwise)

	AD208AY	AD208BY
GAIN		
Range	1–1000 V/V	*
Error (G = 1 V/V)	−1.0% (±2.5%, max)	*
vs. Temperature[1]		
−40°C to 0°C	±60 ppm/°C, max	*
0°C to +85°C	±20 ppm/°C, max	*
vs. Supply Voltage	±100 ppm/V	*
Nonlinearity[2], ±5 V Output Swing, G = 1–1000 V/V	±0.0125%	*
G = 1 V/V	±0.03%, max	±0.015%, max
INPUT VOLTAGE RATINGS[3]		
Linear Differential Range	±5 V, min	*
Max Safe Differential Range	±6 V	*
Max CMV Input to Output		
AC, 60 Hz, Continuous	750 V rms	1500 V rms
Continuous (AC & DC)	±1000 V peak	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz		
R_S ≤100 Ω (HI & LO Inputs),		
G = 1 V/V	100 dB	*
G = 1,000 V/V	120 dB	*
Common Mode Rejection (CMR) @ 60 Hz		
R_S<1 kΩ (Input, HI, LO or Both)		
G = 1 V/V	100 dB	*
G = 1,000 V/V	100 dB	*
Leakage Current, Input to Output, @ 240 V rms, 60 Hz	2 μA rms, max	*
INPUT IMPEDANCE		
Differential (G = 1 V/V)	15 MΩ	*
Common Mode Across the Isolation Barrier	2 GΩ‖5 pF	*
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)		
Initial @ +25°C (Adjustable to Zero)	±(0.25+15 /G) mV, max	*
vs. Temperature (−40°C to +85°C)	±(1.5+20 /G) μV/°C, max	*
vs. Supply Voltage	±(50+150 /G) μV/Volt	*
Voltage Noise, 0.1 Hz to 100 Hz	1.0 μV pk–pk	*
INPUT BIAS CURRENT		
Initial @ +25°C	±10 nA, max	*
vs. Temperature (−40°C to +85°C)	±100 pA/°C, max	*
vs. Supply Voltage	±1 nA/Volt	*
Current Noise, 0.1 Hz to 100 Hz	50 pA pk–pk	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	±6 nA	*
vs. Temperature (−40°C to +85°C)	±60 pA/°C	*
FREQUENCY RESPONSE		
Bandwidth[4] (Full Signal, i.e., V_O≤10 V pk–pk)		
G = 1 V/V	4.0 kHz	*
G = 1000 V/V	0.4 kHz	*
Slew Rate	0.1 V/μs	*
Settling Time to ±0.10% on a 10 V Step, G = 1 V/V	2 ms	*
Overload Recovery Time[5], G = 1000 V/V	5 ms	*
RATED OUTPUT		
Voltage (OUT HI to OUT LO)	±5 V	*
Maximum Voltage Difference Between OUT HI and OUT LO or CLK COM (Pin 32)	±6.5 V	*
Output Resistance	3 kΩ	*
Output Ripple, 100 kHz Bandwidth	10 mV pk–pk	*
5 kHz Bandwidth	0.8 mV pk–pk	*
ISOLATED POWER OUTPUT		
Voltage, No Load	±8.0 V	*
vs. Temperature (−40°C to +85°C)	±0.025%/°C	*

	AD208AY	AD208BY
ISOLATED POWER SUPPLY (Continued)		
Accuracy	±10%	*
Rated Load Current[6]	±2.0 mA, min	*
Regulation, No Load to Rated Load	10%	*
Line Regulation	±10%/Volt	*
Ripple, Rated Load, 100 kHz Bandwidth	100 mV pk–pk	*
CLOCK DRIVE INPUT OF THE AD208[7]		
Input Voltage	15 V pk–pk ± 5%, Square Wave	*
Input Current (No Load on Isolated Supplies)	±10 mA pk	*
Frequency	25 kHz ±5%	*
Duty Cycle	47.5% to 52.5%	*
PACKAGE DIMENSIONS		
SIP Package	2.08″ × 0.260″ × 0.625″, max	*
	52.8 mm × 6.6 mm × 15.9 mm, max	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +85°C	*
Storage	−40°C to +85°C	*
PRICES		
1–24	$51	$58
100s	$32	$36

NOTES

*Specification is the same as that for the AD208AY.

[1]This specification represents the average gain drift over the indicated temperature range. Refer to Figure 2 for an illustration of the typical normalized gain drift for the AD208.

[2]Nonlinearity is specified as a % deviation from a best straight line. For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 4) to the input common (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 30 for a circuit schematic.

[3]To limit the input current to the AD208 during unpowered or saturated conditions it is recommended that a resistor (typically 2 kΩ) be placed in series with the signal and the input terminal of the AD208. A reasonable value for the current limit would be 2.5 mA.

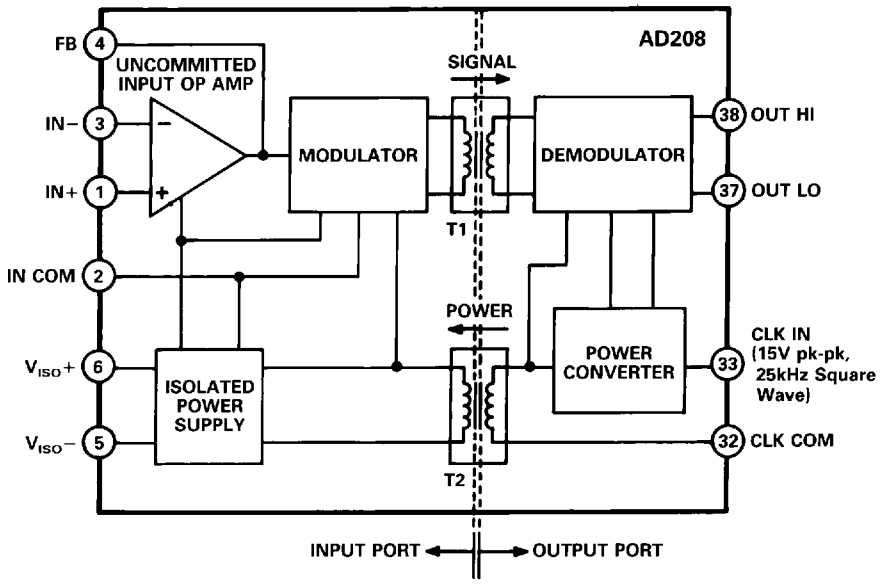
[4]Refer to Figure 16 for a graph of the AD208's 3 dB Bandwidth versus Gain Setting.

[5]Overload Recovery Time is the time it takes for the isolation amplifier to return to within ±0.10% of its correct value from a saturated condition once the initiating overrange signal has been removed. For the AD208, the overload recovery time is determined by applying a +5 V (−5 V) pulse at the input terminals, when the AD208 is configured for a gain of 1,000 V/V, and then measuring the time it takes for the output to return to zero from its positive (negative) full-scale saturated voltage condition. A 2 kΩ resistor placed in series with the signal and the input terminal will reduce the overload recovery time to approximately 2 ms.

[6]Refer to Figure 17 for a curve illustrating the load drive capabilities of the isolated power supply.

[7]It is recommended that the AD246 Clock Driver be used to drive the AD208. Refer to the "Powering the AD208 Section" of this data sheet for a detailed description of the AD208's clock driver input voltage and current requirements.

Specifications subject to change without notice.

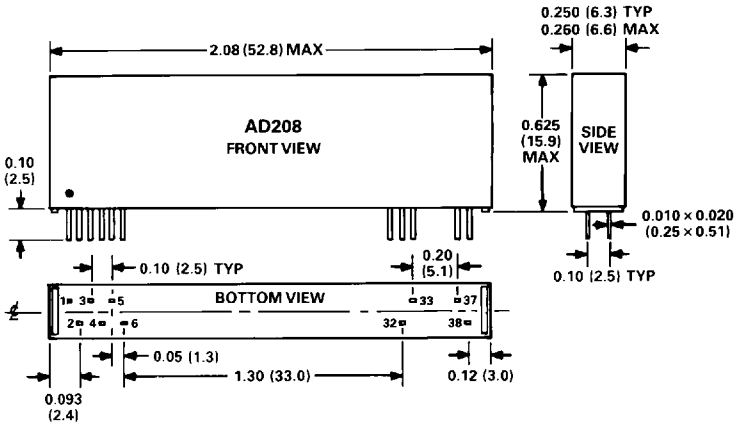


Functional Block Diagram

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

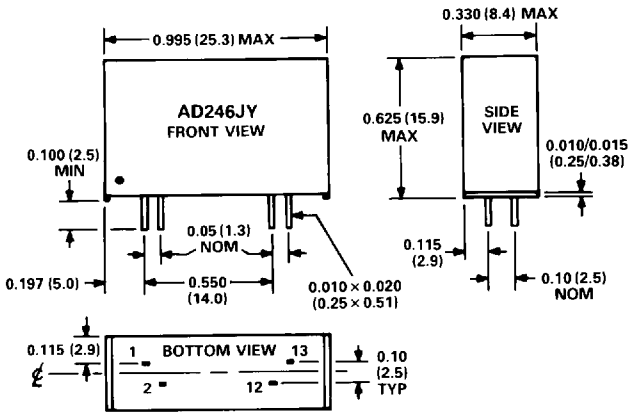
AD208 SIP Package



AD208 Pin Designations

PIN	DESIGNATION	FUNCTION
1	IN+	NONINVERTING INPUT
2	IN COM	INPUT COMMON
3	IN−	INVERTING INPUT
4	FB	INPUT OP AMP; OUTPUT/FEEDBACK
5	V_{ISO-}	ISOLATED POWER: −DC OUTPUT
6	V_{ISO+}	ISOLATED POWER: +DC OUTPUT
32	CLK COM	CLOCK COMMON
33	CLK IN	CLOCK INPUT
37	OUT LO	OUTPUT LO
38	OUT HI	OUTPUT HI

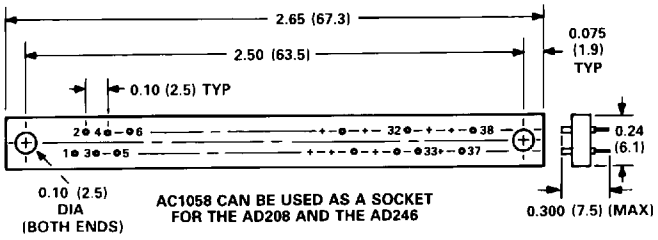
AD246 SIP Package



AD246 Pin Designations

PIN	DESIGNATION	FUNCTION
1	PWR IN	DC POWER SUPPLY INPUT
2	CLK OUT	CLOCK OUTPUT
12	PWR COM	POWER COMMON
13	PWR COM	POWER COMMON

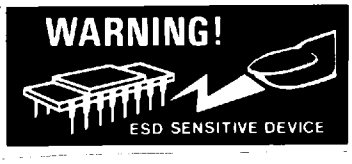
AC1058 Mating Socket



NOTES:
- AMP ZP SOCKET (P/N 2-382006-3) MAY BE USED IN PLACE OF THE AC1058.
- NUMBERS BESIDE THE PIN RECEPTACLES OF THE AC1058 CORRESPOND TO THE PIN NUMBERS OF THE AD208.

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



INSIDE THE AD208

The functional block diagram of the AD208 is shown previously. The AD208 employs amplitude modulation techniques to implement transformer coupling of signals down to dc. The primary side of the power transformer, T2, is driven by the externally supplied 15 V pk–pk, 25 kHz square wave generator or the AD246 Clock Driver.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The output signal is not internally buffered, therefore the user is free to interchange the output leads to get signal inversion.

The input port of the AD208 contains an uncommitted input op amp, a modulator and the isolated power supply. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

PERFORMANCE CHARACTERISTICS

Gain Error. Figure 1 shows the typical gain error for the AD208, expressed in % of full scale, as a function of the isolator's output load (Ω). For minimal gain errors, the AD208 is best operated with output loads greater than or equal to 1 MΩ.

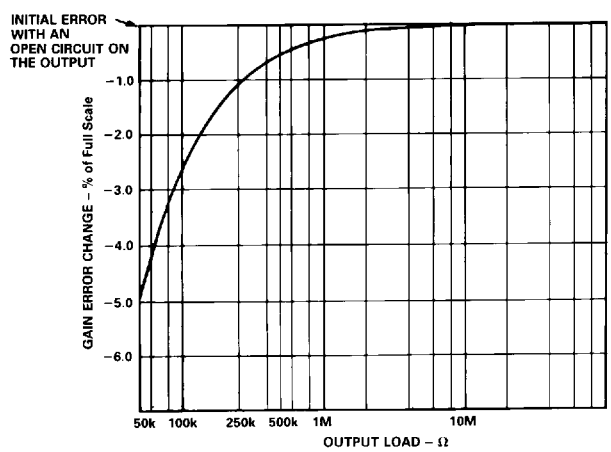


Figure 1. Gain Error Change (% of Full Scale) vs. Output Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Drift. Figure 2 presents the normalized gain drift, from the gain error measured at +25°C, of the AD208 over the −40°C to +85°C rated temperature range.

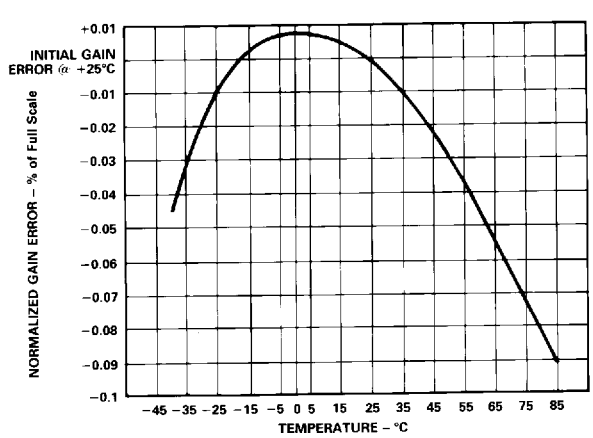


Figure 2. Normalized Gain Error (% of Full Scale) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The effect of the output load on the AD208's gain temperature coefficient is shown in Figure 3 for the −40°C to 0°C and 0°C to +85°C temperature ranges. To minimize the gain temperature coefficient, the AD208 performs best with output loads of greater than or equal to 1 MΩ.

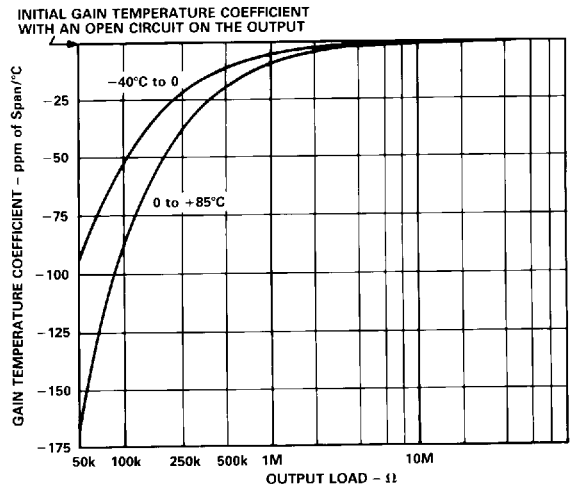


Figure 3. Gain Temperature Coefficient (ppm/°C) vs. Output Load (Ω) and Operating Temperature Range, with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Nonlinearity. The typical gain nonlinearity error of the AD208, at a gain of 1 V/V, is specified as ±0.0125% or ±1.25 mV. The nonlinearity performance of the AD208 is dependent on the output voltage swing and this dependency is illustrated in Figure 4. The vertical axis represents the nonlinearity error, expressed in % of output span (i.e., % of 10 V) on the left axis or in mV on the right axis. The horizontal axis displays the magnitude of the output voltage swing.

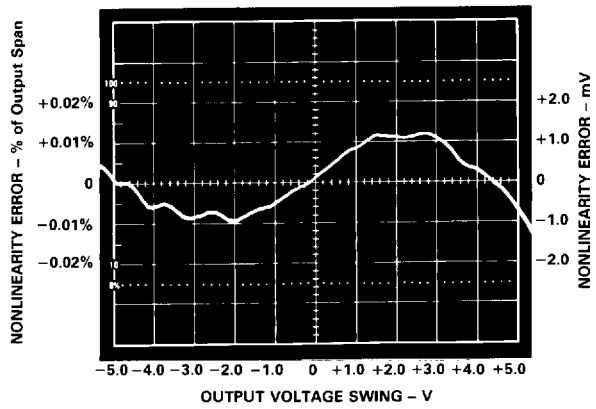


Figure 4. Typical Gain Nonlinearity Error (% of Output Span and mV) vs. Output Voltage Swing for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

The variation of the AD208's gain nonlinearity, from that measured at +25°C, over the entire −40°C to +85°C rated temperature range is demonstrated by the curve in Figure 5.

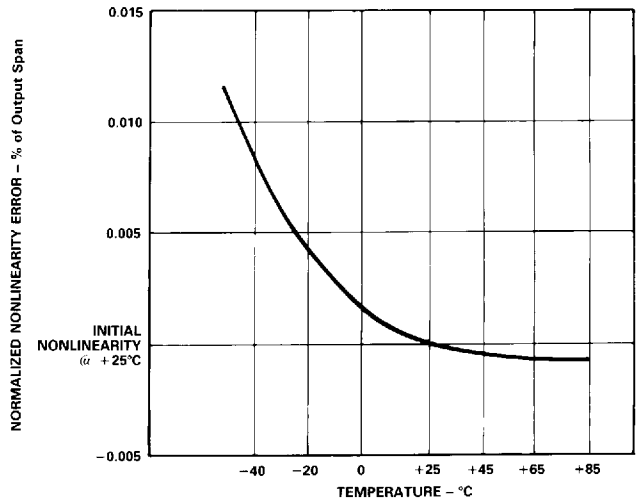


Figure 5. Normalized Gain Nonlinearity (% of Output Span) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The nonlinearity of the AD208 is minimized when its output load is greater than 1 MΩ, as shown in Figure 6.

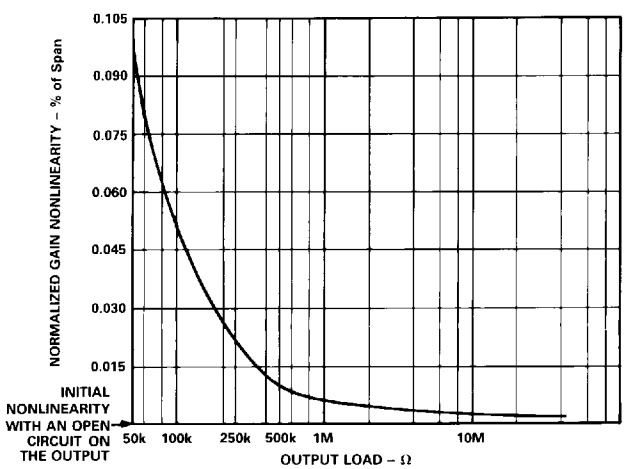


Figure 6. Normalized Gain Nonlinearity (% of Output Span) vs. Output Load (Ω) for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Voltage Rating. The linear input voltage range for the AD208 is specified as ±5 V. This rating applies when the AD208 is powered by a 15 V pk–pk ±5%, square wave (@ 25 kHz). The specified input voltage range is, however, affected by the clock driver voltage and the load placed on the AD208's front-end isolated power supplies. The variation of the input voltage range as a function of the isolated power supply load and the clock supply voltage are illustrated by the parametric curves in Figure 7.

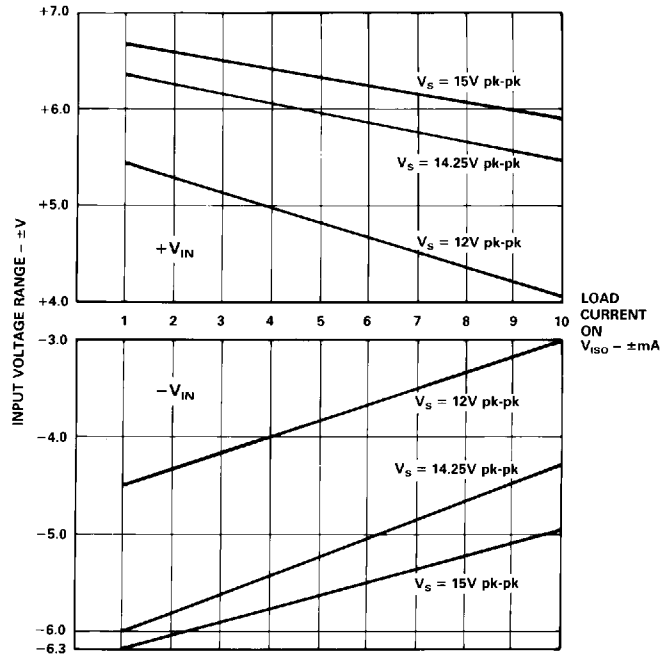


Figure 7. Input Voltage Range (±V) vs. Load Placed on the Isolated Power Supplies (mA) and Clock Driver Voltage (V pk–pk)

Common Mode Rejection. Figures 8 and 9 illustrate the typical common mode rejection, expressed in dB, of the AD208 as a function of the common mode signal frequency (kHz) and source impedance imbalance (kΩ) for gains of 1 V/V and 1,000 V/V, respectively.

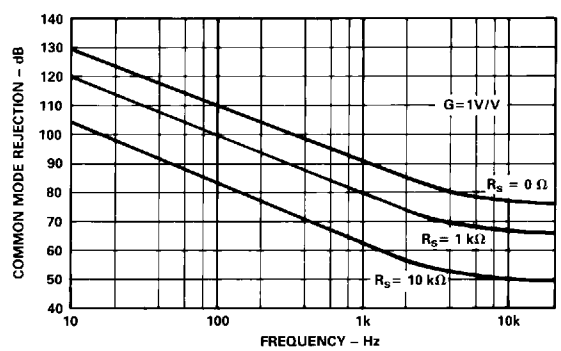


Figure 8. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance Imbalance (kΩ) for a Gain of 1 V/V

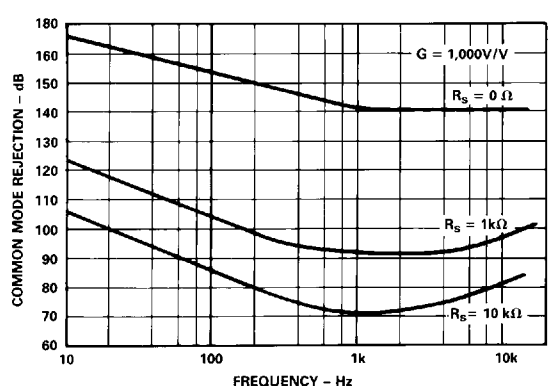


Figure 9. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance

To achieve the optimal common mode rejection of unwanted signals, it is strongly recommended that the source impedance imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

Output Offset Voltage. The normalized output offset voltage drift from the initial offset measured at +25°C is presented in Figure 10 over the rated −40°C to +85°C temperature range.

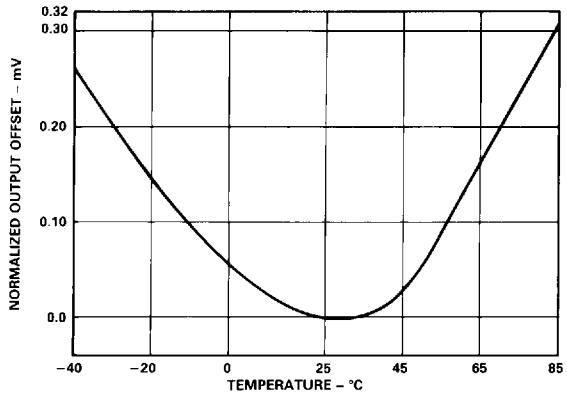


Figure 10. Normalized Output Offset Voltage (mV) vs. Temperature (°C) with an AD208 Gain of 1 V/V, with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Offset Voltage. The AD208 exhibits an extremely low input offset voltage temperature coefficient over the −40°C to +85°C temperature range as indicated in Figure 11.

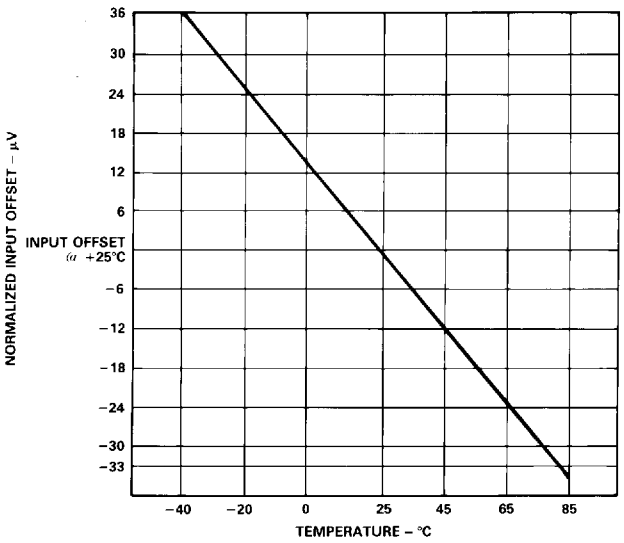


Figure 11. Normalized Input Offset Voltage (µV) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The typical noise characteristics for the AD208's uncommitted input op amp is summarized in Figure 12.

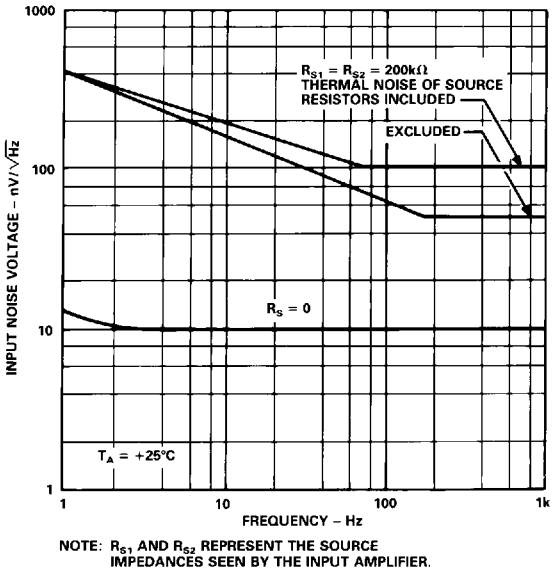


Figure 12. Typical Input Voltage Noise (nV/√Hz) vs. Frequency for the AD208's Uncommitted Input Op Amp

Input Bias Current. The typical input bias current variation from the initial bias current at +25°C as a function of temperature is presented in Figure 13.

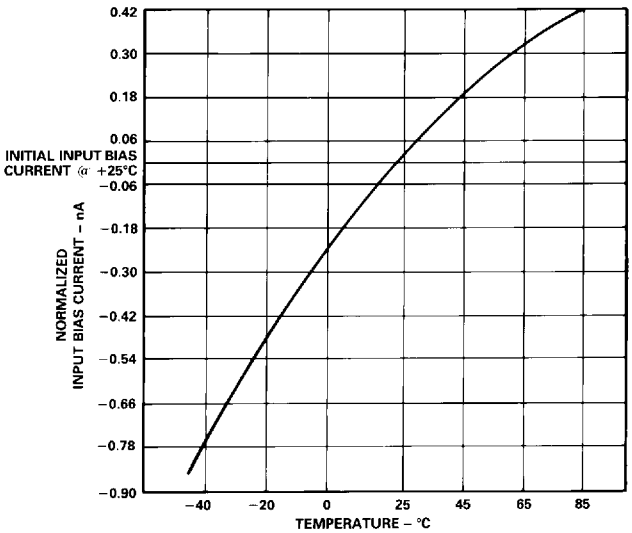


Figure 13. Normalized Input Bias Current (nA) vs. Temperature (°C)

Frequency Response: Gain and Phase Shift. Figure 14 characterizes the AD208's gain as a function of frequency, while Figure 15 illustrates the corresponding phase shift versus frequency.

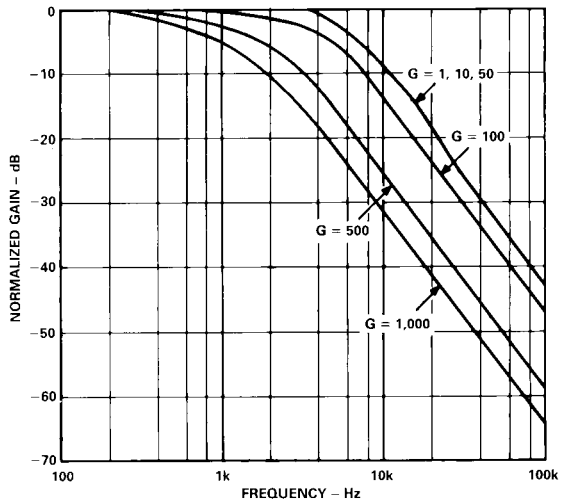


Figure 14. Normalized Gain (dB) as a Function of Input Signal Frequency (Hz)

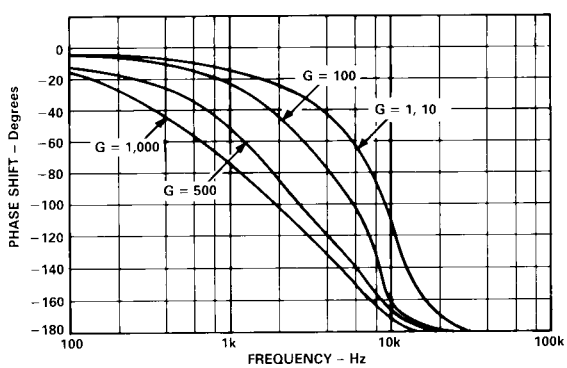


Figure 15. Phase Shift (Degrees) vs. Input Signal Frequency (Hz)

The frequency response performance of the AD208 can also be characterized in terms of its 3 dB bandwidth versus the desired gain setting as plotted in Figure 16.

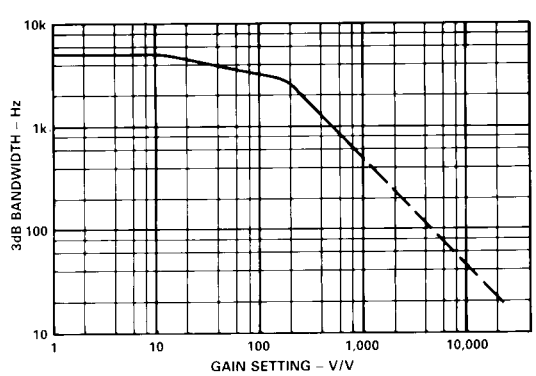


Figure 16. 3 dB Bandwidth (Hz) vs. AD208 Gain Setting (V/V)

Isolated Power Supply. The load characteristics of the AD208's isolated power supplies are plotted in Figure 17. It is recommended that the isolated power supply load not exceed 10 mA as permanent damage to the internal power circuitry of the AD208 may occur.

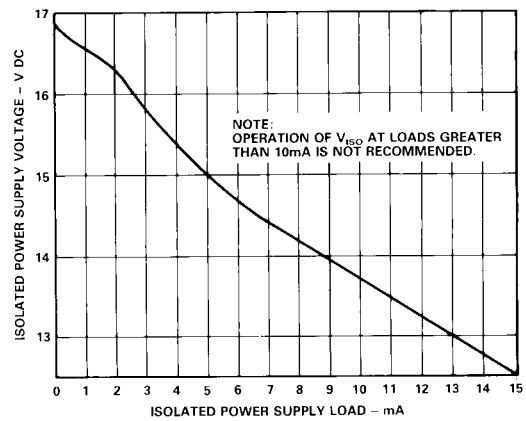


Figure 17. Isolated Power Supply Voltage (V DC) vs. Isolated Power Supply Load (mA), with V_S = 15 V pk–pk, 25 kHz Square Wave

The isolated power supply exhibits some ripple which varies as a function of the load placed on the supply terminals. Figure 18 illustrates the functional relationship between the isolated supply ripple (mV pk–pk) and the resistive load placed on the supplies.

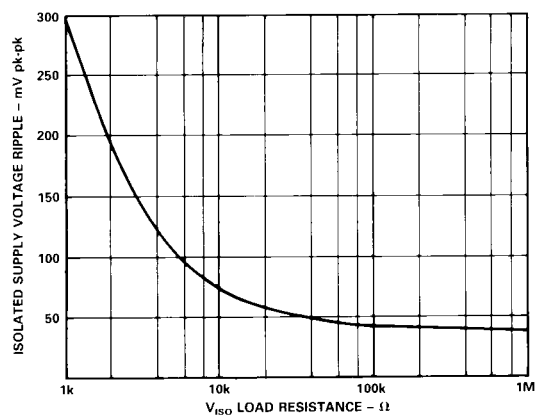


Figure 18. Isolated Power Supply Ripple (mV pk–pk) vs. Resistive Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

The AD208 has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load conditions. If a specific application requires more bypassing of the isolated power supplies, external capacitors may be added. Figure 19 plots the isolated power supply ripple as a function of the external bypass capacitance under rated load conditions (i.e., ±2 mA).

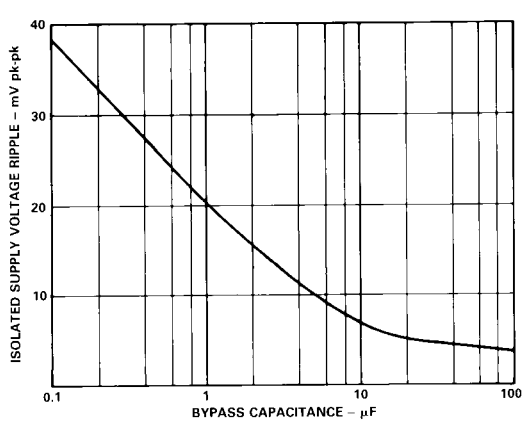


Figure 19. Isolated Power Supply Ripple (mV pk–pk) vs. Bypass Capacitance (μF) with a ±2 mA Load on the Isolated Supplies and a Noise Bandwidth of 100 kHz

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

As an assurance of high performance reliability, the CMV rating of each grade of the AD208 is factory tested for one minute to 120% of the appropriate CMV isolation rating (1800 V rms for the B grade and 900 V rms for the A Grade).

POWERING THE AD208

The AD208 is powered by an externally supplied 15 V pk–pk, 25 kHz square wave (50% duty cycle) clock signal connected as shown in Figure 20. An ac coupling capacitor is provided in the AD208 to level shift the clock signal which in turn generates the necessary internal dc supply voltages and carrier signal.

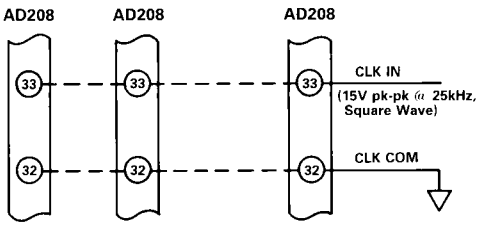


Figure 20. Powering the AD208

The rated performance of the AD208 is specified for a clock driver square wave signal that meets the following requirements:

- 15 V pk–pk ±5%
- 25 kHz ±5%
- 47.5% to 52.5% duty cycle.

Care must be exercised when using a square wave generator whose output does not meet the above requirements as the performance of the AD208 may be adversely affected.

Clock Driver Voltage Considerations. The rated performance of the AD208 will remain unaffected for clock driver voltages in the 14.25 V pk–pk to 15.75 V pk–pk range. Voltage swings below 14.25 V pk–pk will result primarily in the derating of the output voltage and isolated power supply voltage specifications as shown in Figures 21 and 22, respectively.

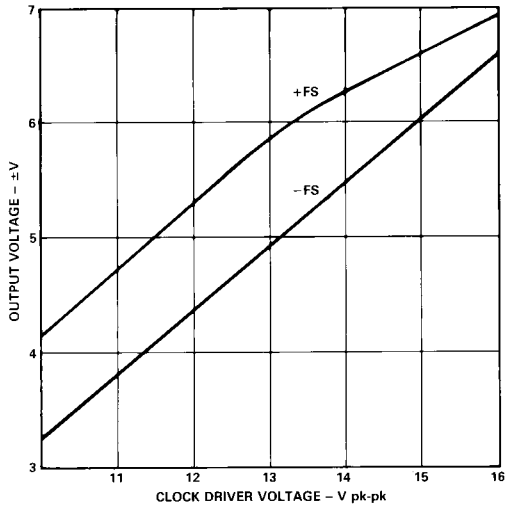


Figure 21. Output Voltage Swing (±V) vs. Clock Driver Voltage (V pk–pk)

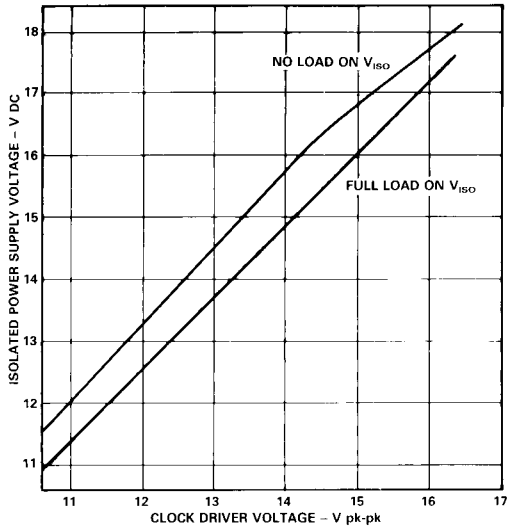


Figure 22. Isolated Power Supply Voltage (V DC) vs. Clock Driver Voltage (V pk–pk)

The reduction in the rated output voltage will increase the values for the nonlinearity and gain error parameters of the AD208 because of the headroom limits placed on the internal circuitry.

Note: Clock driver voltages greater than 16.5 V pk–pk may damage the internal components of the AD208 and consequently should not be used.

Clock Driver Frequency Considerations. The definition of the clock duty cycle for a two-state rectangular waveform is given by:

$$\text{Duty Cycle (\%)} = T_{HI}/(T_{HI} + T_{LO}) \times 100\%$$

where:

T_{HI} = The period of time that the waveform is in the HI state.

T_{LO} = The period of time that the waveform is in the LO state.

The performance of the AD208 will not be adversely affected by off-nominal clock signals so long as these clock signals are in the 47.5% to 52.5% duty cycle range and the 23.75 kHz to 26.25 kHz frequency range. To prevent a significant deterioration of the AD208 performance, it is strongly recommended that the clock driver duty cycle and frequency values ultimately chosen to operate the AD208 do not fall outside of the 40% to 60% and 20 kHz to 30 kHz ranges.

Clock Driver Power Considerations. In selecting and/or designing a clock driver for the AD208 isolation amplifier, it should be noted that the AD208 presents a reactive load to the clock driver. Consequently, both the average and peak drive currents to the AD208 clock input must be considered. Figures 23 and 24 illustrate the typical clock driver input voltage and current waveforms for a single AD208 with its isolated power supplies unloaded and fully loaded.

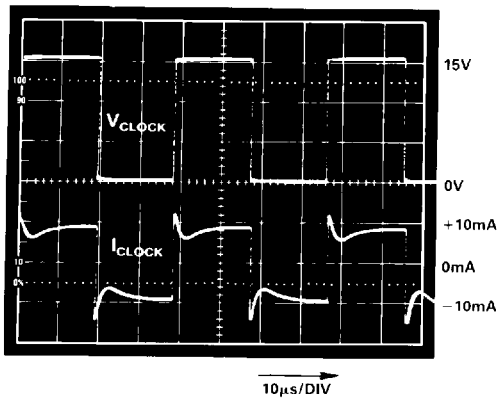


Figure 23. Typical Clock Voltage and Current Waveforms for a Single AD208 with No Load on its Isolated Power Supply

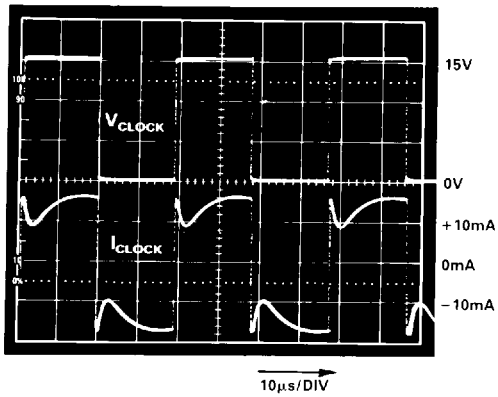


Figure 24. Typical Clock Voltage and Current Waveforms for a Single AD208 with a ±2 mA Load on its Isolated Power Supply

USING THE AD246 CLOCK DRIVER TO POWER THE AD208

To ensure that the power requirements of the AD208 are satisfied, Analog Devices suggests the use of the AD246 Clock Driver. The AD246 is an inexpensive, compact square wave oscillator that can be used to generate the necessary AD208 clock signal from a single +15 V dc supply. Table I lists the key specifications for the AD246.

	AD246JY
OUTPUT	
Frequency	25 kHz
Voltage	15 V pk–pk
Duty Cycle	50%
Maximum Safe Current Drive Capability[1]	120 mA
Fan Out	16
Resistance	15 Ω
POWER SUPPLY REQUIREMENTS	
Input Voltage	+15 V dc ± 5%
Supply Current	
Unloaded	3.5 mA
Each AD208 Adds	4.0 mA
Each 1 mA Load on AD208	
$+V_{ISO}$ or $-V_{ISO}$ Adds	1.12 mA

NOTE
[1]The high current drive output of the AD246 will not withstand a short to ground.

Table I. Key Specifications for the AD246 Clock Driver (Specifications typical @ +25°C and V_S = +15 V DC unless otherwise noted)

The AD246JY is connected to the AD208 oscillator input(s) as shown in Figure 25. The AC1058 mating socket can be used with the AD246JY as demonstrated in Figure 27.

A supply bypass capacitor is included in the AD246, however it is recommended that an externally supplied bypass capacitor, as indicated by the dotted circuitry in Figure 26, be used if many AD208s are to be driven by a single AD246. The suggested capacitance value is 1 μF for every five AD208s driven. The placement of the bypass capacitor should be as close as possible to the AD246 Clock Driver.

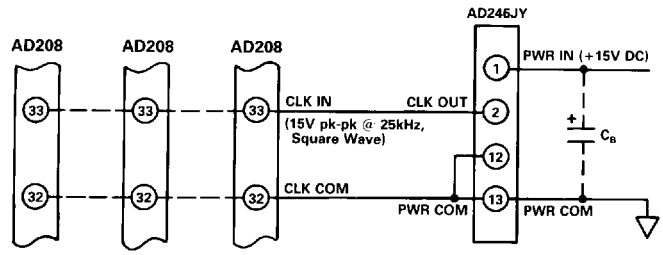


Figure 25. Using the AD246 to Power the AD208

USING THE AD208

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±5 V is shown in Figure 26.

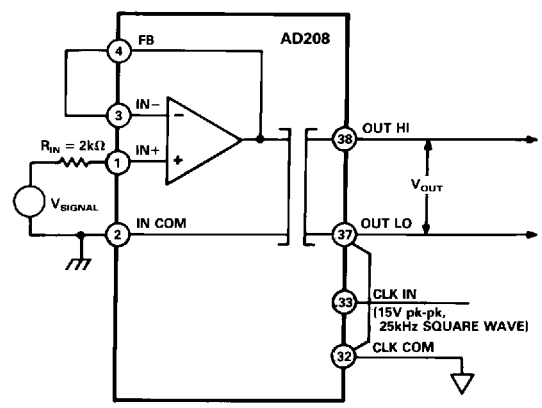


Figure 26. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 27 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

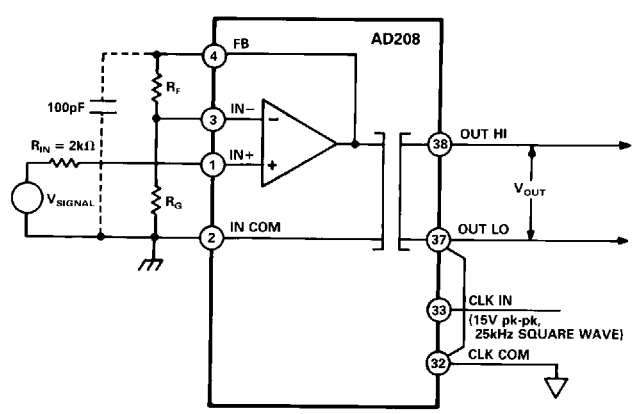


Figure 27. Input Configuration for a Gain Greater Than 1

In this circuit, the gain equation may be written as:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where:

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

The values for the resistors R_F and R_G should be chosen subject to the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA. Note that for each mA drawn by the feedback resistor, the isolated power supply drive capability will decrease by 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

Note on the 100 pF Capacitor: Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 27, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

Note on the 2 kΩ Resistor: The 2 kΩ resistor placed in series with the input signal source and the IN+ terminal, designated as R_{IN} in Figures 26 and 27, is suggested so as to limit the current seen at the input terminals to 2.5 mA when the AD208 is OFF. The 2 kΩ resistor will also reduce the overload recovery time to 2 ms.

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp is given in Figure 28. These curves can be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when reactive or nonlinear components are used in conjunction with the uncommitted input op amp.

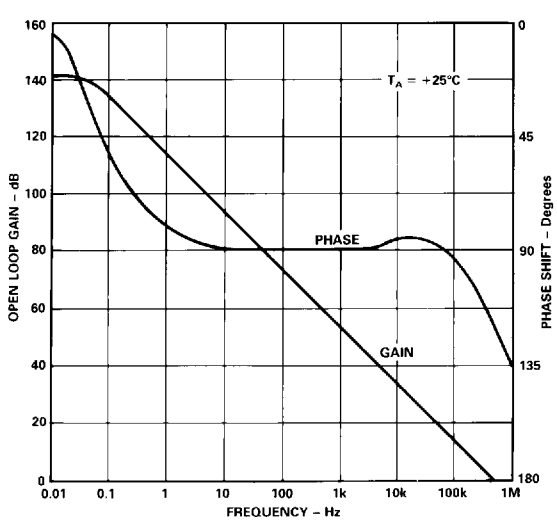


Figure 28. Open Loop Gain and Phase Response for the Uncommitted Input Op Amp of the AD208

A capacitor placed in the feedback loop of the input op amp may increase the nonlinearity of the AD208, particularly for large gains. A resistor (1 kΩ) placed in series with this capacitor should minimize the capacitor's effect on nonlinearity.

Signal Inversion. The circuits illustrated in Figures 26 and 29 are "noninverting." If signal inversion is desired simply interchange the output leads of the circuits shown in Figures 26 or 27 to get inversion. This approach allows for the retention of the high input impedance characteristics of the "noninverting" circuit.

Summing or Current Input Configuration. Figure 29 shows how the AD208 can accommodate current inputs or sum currents or voltages.

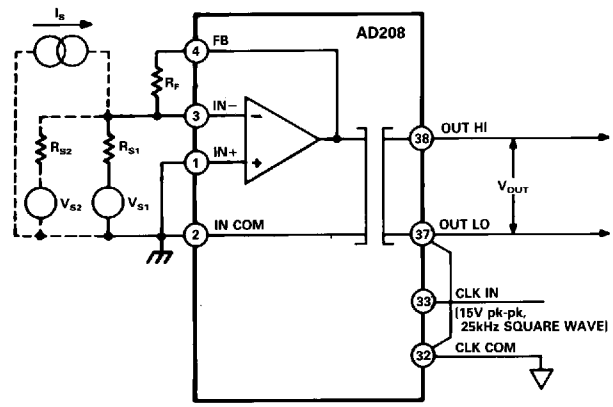


Figure 29. Summing or Current Input Configuration

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where:

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor (Ω)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω)
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 29 can also be used when the input signal is larger than the ±5 V input range of the isolator. For example, suppose that in Figure 29 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 29. Now, a V_{S1} with a ±50 V span can be accommodated with R_F = 20 kΩ and R_{S1} = 200 kΩ.

Output Filter Circuit. Except at the highest useful gains, the noise seen at the output of the AD208 will be almost entirely comprised of the carrier ripple at multiples of 25 kHz. The ripple, when measured over a 100 kHz noise bandwidth, is typically 2 mV pk–pk near zero output and increases to approximately 7 mV pk–pk for outputs of ±5 V. The simple two-pole, 5 kHz low-pass Butterworth filter of Figure 30 can be used to reduce the output ripple of the AD208 to approximately 0.1 mV pk–pk and serve as an output buffer for the AD208.

An output buffer or filter may sometimes exhibit voltage spikes on the output even though none were present on the input signal to the buffer/filter. These spikes are usually due to clock

An output buffer or filter may sometimes exhibit voltage spikes on the output even though none were present on the input signal to the buffer/filter. These spikes are usually due to clock noise appearing at the op amp's power supply pins, since most op amps have little or no supply rejection at high frequencies. Another common source of clock-related noise is from the sharing of the ground track by both the output circuit and the power input. The circuit of Figure 30, shows how to avoid these clock noise related problems.

Ideally, the output signal LO lead and the supply common should be tied together at the final signal measurement point as indicated in Figure 30. It may be useful to bypass the output LO to the output common with a 0.1 μF capacitor should the measurement point be more than a few feet from the isolator.

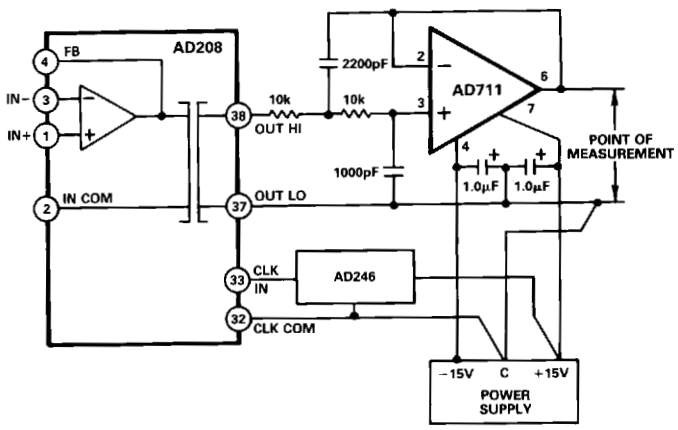


Figure 30. Output Filter Circuit Showing Proper Grounding

In multichannel applications where more than a few AD208s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal output lead returns to a low impedance point (usually OUT LO). Consequently, both of these tracks should be made as large and as short as possible to minimize the track inductance and resistance. For best results, OUT LO should be connected directly to a ground plane that serves as the measurement common.

Current spikes can be greatly reduced by connecting a small inductance, 68 μHy to 100 μHy, in series with the clock drive input pin of each AD208. Molded chokes, such as the Dale IM-2 series, with a dc resistance of about 5 Ω should be suitable for most applications.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset Adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain Adjustments are most easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- To ensure the highest degree of stability in the gain and offset adjustments, the adjusting potentiometers should be located as close as possible to the isolator's front end. Adjustment ranges should be kept to a minimum and high quality multiturn trimming potentiometers should be used.
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.
- It is recommended that the offset adjustment precedes the gain adjustment.

Input Adjustments for the Noninverting Mode of Operation

Offset Adjustment. Figure 31 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P_2 is responsible for nulling out the offset voltage. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV. Since the offset is zeroed out ahead of the gain, the values given above for P_2, R_{OA} and R_C should work for any gain on the isolator.

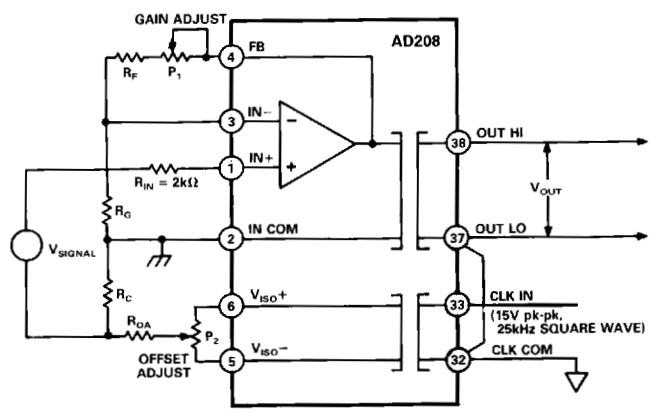


Figure 31. Input Adjustment Circuit for the Noninverting Mode of Operation

Notes:

- To minimize CMR degradation it is recommended that the resistor R_C (shown in Figure 31) be below a few hundred ohms.
- The offset adjustment circuit of Figure 31 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 31 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P_1 is incorporated into the gain-setting resistor network at the isolator's input.

To maintain gain trim ranges that are independent of the gain setting, the potentiometer P_1 should be proportioned to R_F such that

$$\frac{P_1 \times 100\%}{R_F} = \textit{Desired Gain Adjustment Range (in \% of Output Span)}$$

and

$$(R_F + P_1/2)/R_G + 1 = \textit{Desired Gain Setting}$$

Input Adjustments for the Inverting Mode of Operation
Offset Adjustment. Figure 32 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P_2 nulls the voltage at the summing node. This method may be preferred over current injection since it is less affected by any subsequent gain adjustments. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV.

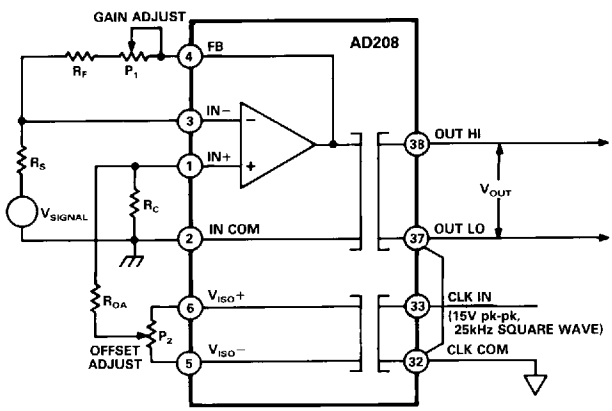


Figure 32. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 32 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P_1. The adjustments will be effective for all gains in the 1 to 1,000 V/V range.

Output Adjustments
Offset Adjustment. Figure 33 shows the recommended technique for offset adjustment at the output. In this circuit, a ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 33, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_C \times V_S}{R_C + R_O}$$

where, V_S is the power supply voltage. A 100 kΩ P_0, 100 Ω R_C and a 50 kΩ R_O should provide an offset adjustment range of about ±30 mV on the output.

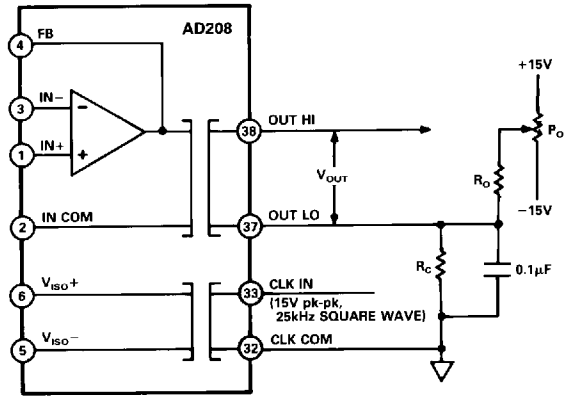


Figure 33. Output Side Offset Adjustment Circuit

Gain Adjustment. Since the output stage of the AD208 is unbuffered, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD208 provides ±8.0 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power output has a current capacity of up to 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners or remote transducers.

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATION EXAMPLES

Isolated RTD Signal Processing. The stable high gain properties and low offset drift characteristics make the AD208 an ideal component for use in isolated RTD signal processing applications. RTD applications typically require the following three major elements: a stable current excitation source, a lead compensation network and a zero suppression network. The circuit schematic of Figure 34 illustrates how to use the AD208 with a handful of low power external components to condition, amplify and isolate low level RTD signals.

In the RTD application shown in Figure 34, the stable current excitation source needed to drive the RTD consists of a:

- Dual, single supply op amp (LM358)
- Pair of low V_{GSOFF} JFETS (ex. J201)
- Low power 2.5 V reference source
- Several precision 10 kΩ, 1%, 10 ppm/°C resistors.

The dual current sources generate a 250 μA excitation signal for the RTD and they also provide about 5 V of compliance with a ±5% gain adjustment range.

Zero suppression is accomplished in Figure 34 by using a simple ground servo amplifier in combination with the resistor labelled R_Z, while lead wire compensation is realized by remote sensing the RTD with the ground servo. The current, I_{S1} develops a voltage V_1 that is equal to:

$$V_1 = V_{OS_{A1}} + V_Z + V_{LEAD}$$

where the voltages V_1, $V_{OS_{A1}}$, V_Z and V_{LEAD} are as indicated in Figure 34.

The current I_{S2}, in turn, develops the voltage seen by the input amplifier of the AD208 and, with reference to the voltages labelled in Figure 34, V_{IN} is given by:

$$\begin{aligned} V_{IN} &= V_1 - V_{RTD} - V_{LEAD} \\ &= (V_{OS_{A1}} + V_Z + V_{LEAD}) - V_{RTD} - V_{LEAD} \\ &= V_{OS_{A1}} + V_Z - V_{RTD}. \end{aligned}$$

The offset trim circuit can then be used to null out all of the offset terms. Note that a high quality low power, low offset drift amplifier should be used for the ground servo amplifier.

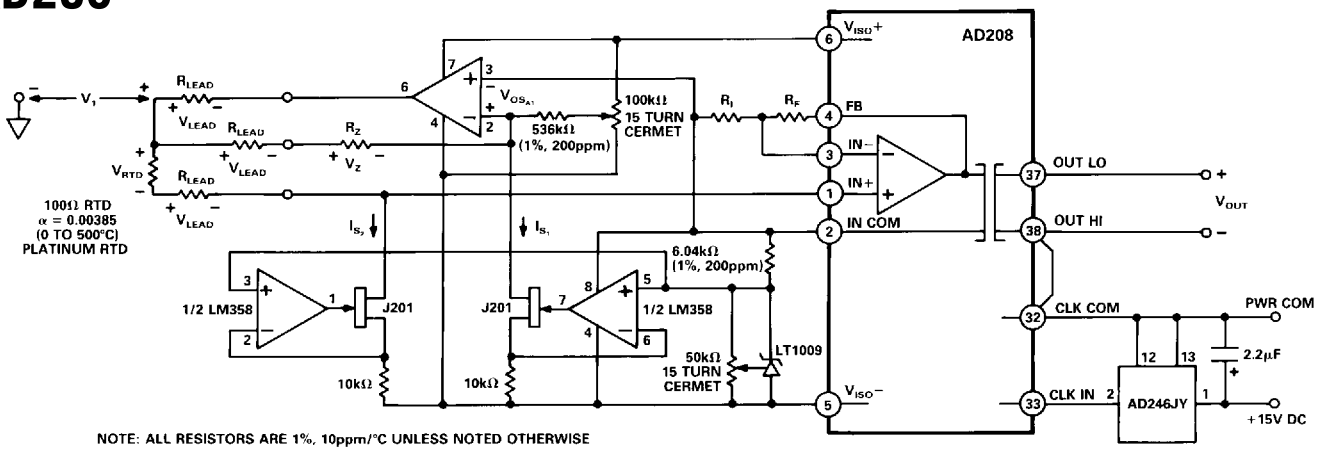


Figure 34. Using the AD208 in an Isolated RTD Application

The typical sensitivity of a 100 Ω platinum RTD with a 0.25 mA current excitation is in the 95 μV/°C range. Therefore, using the AD208 isolation amplifier with a gain of 105 V/V will result in an approximate output sensitivity of 10 mV/°C which corresponds to a 0 to 500°C RTD range for a 0 to −5 V output span. If a 0 to +5 V output span is desired, simply reverse the OUT LO (Pin 37) and OUT HI (Pin 38) terminals of the AD208 taking care to ensure that the OUT LO pin is now connected to the CLK COM terminal.

The gain equation for the circuit of Figure 34 is determined by the formula given below.

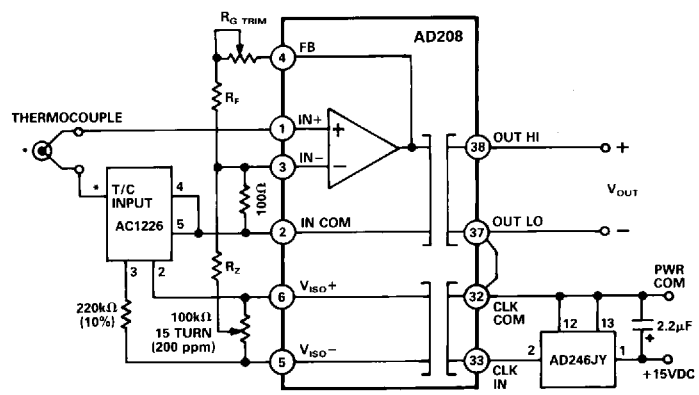
$$\frac{V_O\,(HI) - V_O\,(LO)}{I_S \cdot (\Omega_{RTD}\,(HI) - \Omega_{RTD}\,(LO))} = R_F/R_I + 1$$

where:

V_O (HI)	=	AD208 output voltage at the maximum expected temperature seen by the RTD application
V_O (LO)	=	AD208 output voltage at the minimum expected temperature seen by the RTD application
Ω_{RTD} (HI)	=	Resistance of the RTD at the maximum expected temperature
Ω_{RTD} (LO)	=	Resistance of the RTD at the minimum expected temperature
R_Z	=	RTD resistance at 0°C (100 Ω, typ)
I_S	=	Current of the stable excitation source (0.25 mA)
R_F	=	Feedback resistor (10.5 kΩ)
R_I	=	Input resistor (100 Ω, 1%, 10 ppm/°C).

The circuit of Figure 34 accommodates a 10 mV/°C, unlinearized output for a 100 Ω platinum RTD. The circuit allows for a maximum measured temperature range of 500°C. The initial input offset is ±1.3 mV (max) which is roughly equivalent to 5.2 Ω. The offset adjustment circuit, which has a ±1.5 mV (RTI) adjustment range, can be used to easily trim out this initial offset. The offset drift of the RTD application shown in Figure 34 is ±4 μV/°C (max) or 0.016 Ω/°C.

Thermocouple Applications. Thermocouples provide an inexpensive and reliable way to measure temperature over a wide range. Thermocouples require high gain amplification and in some cases cold junction compensation. The circuit of Figure 35 shows how the stable high gain capability of the AD208 can be effectively utilized to amplify and isolate the low level voltage signals from a thermocouple. The AC1226 Monolithic Cold Junction Compensator is recommended for use in this application. The AC1226 acts to eliminate the cold junction voltage that is formed between the thermocouple wire and the actual measurement circuit. The AC1226 outputs 0 V at 0°C and it provides the correct compensation slope for many thermocouple types through user selected taps off of the internal AC1226 resistor string.



PIN	T/C TYPE
1	E
6	R, S
7	K, T
8	J

Figure 35. Input Adjustments for the Inverting Mode of Operation

The gain and offset adjustment for the circuit shown in Figure 35 is easily accomplished by first shorting the AD208 inputs to ground (IN COM) and adjusting the offset potentiometer until 0 V is measured at the output. Once the offset has been nulled out, the gain adjustment can then be initiated by applying an appropriate full-scale voltage, for the thermocouple type being used, at the input. Then adjust the gain trim until measuring +5 V out. The offset and gain trim do interact slightly with each other consequently, it would be advisable to recheck the offset error and readjust it if necessary. The residual error that may be introduced by the AC1226 at 25°C will be no more

than ±2°C off nominal for all temperature ranges specified in Table II.

Table II lists the most commonly used thermocouple types along with their typical temperature ranges and a suggested AD208 gain setting. The table also includes recommended values for the feedback resistor (R_F), the gain trim resistor ($R_{G_{TRIM}}$) and the offset adjustment resistor (R_Z) all three of which are shown in Figure 35.

Thermo-couple Type	Maximum Temperature Range @ 5 V Out (°C)	Maximum V_{IN} (mV)	AD208 Gain Setting (V/V)	SUGGESTED RESISTOR VALUES (With Reference to Figure 38) R_F (kΩ)	$R_{G_{TRIM}}$ (kΩ)	R_Z (MΩ)
E	900	68.783	72.69	6.98	0.5	2.0
J	750	42.283	118.25	11.5	1.0	2.0
K	1,250	50.633	98.75	9.53	1.0	2.0
R	1,450	16.741	298.6	28.7	2.0	2.0
S	1,450	14.973	333.9	32.4	2.0	2.0
T	350	17.816	280.6	27.4	2.0	2.0

Table II. Commonly Used Thermocouple Types, Temperature Ranges, AD208 Gain Settings and Circuit Resistor Values