

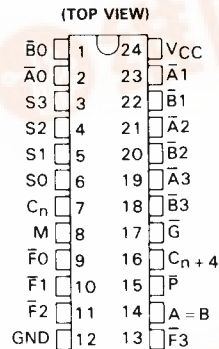
查询SN54AS181AJT供应商

# SN54AS181, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNIT/FUNCTION GENERATORS

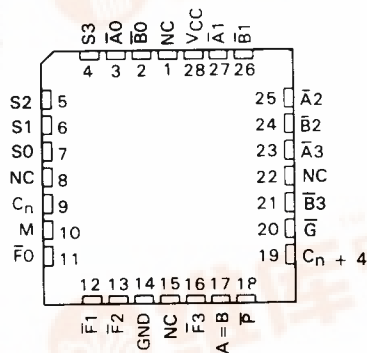
D2661, DECEMBER 1982—REVISED MAY 1986

- Package Options Include the 'AS181A in Compact 300-mil or Standard 600-mil Packages. The 'AS881A is Offered in 300-mil Packages. Both Devices are Available in Both Plastic and Ceramic Chip Carriers.
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - 'AS881A Provides Status Register Checks
  - Plus Ten Other Logic Operations
- Dependable Texas Instruments Quality and Reliability

SN54AS181A . . . JT OR JW PACKAGE  
SN54AS881A . . . JT PACKAGE  
SN74AS181A . . . DW, NT OR NW PACKAGE  
SN74AS881A . . . DW OR NT PACKAGE

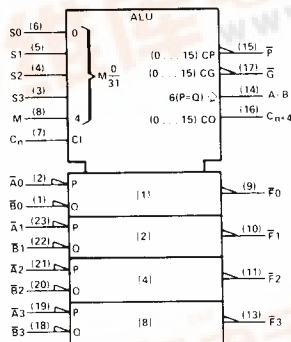


SN54AS181A, SN54AS881A . . . FK PACKAGE  
SN74AS181A, SN74AS881A . . . FN PACKAGE



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, JW, NT, and NW packages.

TYPICAL ADDITION TIMES ( $C_L = 15 \text{ pF}$ ,  $R_L = 280 \Omega$ ,  $T_A = 25^\circ\text{C}$ )

| NUMBER OF BITS | ADDITION TIMES           |                          |                       |                        | PACKAGE COUNT               |  | CARRY METHOD BETWEEN ALUs |
|----------------|--------------------------|--------------------------|-----------------------|------------------------|-----------------------------|--|---------------------------|
|                | USING 'AS881A AND 'AS882 | USING 'AS181A AND 'AS882 | USING 'S181 AND 'S182 | ARITHMETIC LOGIC UNITS | LOOK-AHEAD CARRY GENERATORS |  |                           |
| 1 to 4         | 5 ns                     | 5 ns                     | 11 ns                 | 1                      |                             |  | NONE                      |
| 5 to 8         | 10 ns                    | 10 ns                    | 18 ns                 | 2                      |                             |  | RIPPLE                    |
| 9 to 16        | 14 ns                    | 14 ns                    | 19 ns                 | 3 or 4                 | 1                           |  | FULL LOOK-AHEAD           |
| 17 to 64       | 19 ns                    | 19 ns                    | 28 ns                 | 5 to 16                | 2 to 5                      |  | FULL LOOK-AHEAD           |

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## SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

### description

The 'AS181A and 'AS881A are arithmetic logic units (ALU)/function generators that have a complexity of 75 and 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input ( $C_n$ ) and a ripple-carry output ( $C_n + 4$ ) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181A and 'AS881A will accommodate active-high or active-low data if the pin designations are interpreted as follows:

| PIN NUMBER                 | 2          | 1          | 23         | 22         | 21         | 20         | 19         | 18         | 9          | 10         | 11         | 13         | 7           | 16              | 15        | 17        |
|----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|-----------------|-----------|-----------|
| Active-low data (Table 1)  | $\bar{A}0$ | $\bar{B}0$ | $\bar{A}1$ | $\bar{B}1$ | $\bar{A}2$ | $\bar{B}2$ | $\bar{A}3$ | $\bar{B}3$ | $\bar{F}0$ | $\bar{F}1$ | $\bar{F}2$ | $\bar{F}3$ | $\bar{C}_n$ | $\bar{C}_{n+4}$ | $\bar{P}$ | $\bar{G}$ |
| Active-high data (Table 2) | A0         | B0         | A1         | B1         | A2         | B2         | A3         | B3         | F0         | F1         | F2         | F3         | $\bar{C}_n$ | $\bar{C}_{n+4}$ | X         | Y         |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is  $A - B - 1$ , which requires an end-around or forced carry to provide  $A - B$ .

The 'AS181A and 'AS881A can also be utilized as a comparator. The  $A = B$  output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ( $A = B$ ). The ALU must be in the subtract mode with  $C_n = H$  when performing this comparison. The  $A = B$  output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( $C_n + 4$ ) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

| INPUT $C_n$ | OUTPUT $C_{n+4}$ | ACTIVE-LOW DATA<br>(FIGURE 1) | ACTIVE-HIGH DATA<br>(FIGURE 2) |
|-------------|------------------|-------------------------------|--------------------------------|
| H           | H                | $A \geq B$                    | $A \leq B$                     |
| H           | L                | $A < B$                       | $A > B$                        |
| L           | H                | $A > B$                       | $A < B$                        |
| L           | L                | $A \leq B$                    | $A \geq B$                     |

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

# SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## description (continued)

The 'AS881A has the same pinout and same functionality as the 'AS181A except for the  $\bar{P}$ ,  $\bar{G}$ , and  $C_n + 4$  outputs when the device is in the logic mode ( $M = H$ ).

In the logic mode the 'AS881A provides the user with a status check on the input words A and B, and the output word F. While in the logic mode the  $\bar{P}$ ,  $\bar{G}$ , and  $C_n + 4$  outputs supply status information based upon the following logical combinations:

$$\bar{P} = F_0 + F_1 + F_2 + F_3$$

$$\bar{G} = H$$

$$C_n + 4 = PC_n$$

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL

S0 = S3 = H, S1 = S2 = L, and M = H

| C <sub>n</sub> | DATA INPUTS                |                            |                            |                            | OUTPUTS   |           |                    |
|----------------|----------------------------|----------------------------|----------------------------|----------------------------|-----------|-----------|--------------------|
|                | $\bar{A}_0 = \bar{B}_0$    | $\bar{A}_1 = \bar{B}_1$    | $\bar{A}_2 = \bar{B}_2$    | $\bar{A}_3 = \bar{B}_3$    | $\bar{G}$ | $\bar{P}$ | C <sub>n</sub> + 4 |
| H              | $\bar{A}_0 = \bar{B}_0$    | $\bar{A}_1 = \bar{B}_1$    | $\bar{A}_2 = \bar{B}_2$    | $\bar{A}_3 = \bar{B}_3$    | H         | L         | H                  |
| L              | $\bar{A}_0 = \bar{B}_0$    | $\bar{A}_1 = \bar{B}_1$    | $\bar{A}_2 = \bar{B}_2$    | $\bar{A}_3 = \bar{B}_3$    | H         | L         | L                  |
| X              | $\bar{A}_0 \neq \bar{B}_0$ | X                          | X                          | X                          | H         | H         | L                  |
| X              | X                          | $\bar{A}_1 \neq \bar{B}_1$ | X                          | X                          | H         | H         | L                  |
| X              | X                          | X                          | $\bar{A}_2 \neq \bar{B}_2$ | X                          | H         | H         | L                  |
| X              | X                          | X                          | X                          | $\bar{A}_3 \neq \bar{B}_3$ | H         | H         | L                  |

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH

S0 = S1 = S3 = L, S2 = H, and M = H

| C <sub>n</sub> | DATA INPUTS                    |                                |                                |                                | OUTPUTS   |           |                    |
|----------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-----------|-----------|--------------------|
|                | $\bar{A}_0$ or $\bar{B}_0 = L$ | $\bar{A}_1$ or $\bar{B}_1 = L$ | $\bar{A}_2$ or $\bar{B}_2 = L$ | $\bar{A}_3$ or $\bar{B}_3 = L$ | $\bar{G}$ | $\bar{P}$ | C <sub>n</sub> + 4 |
| H              | $\bar{A}_0$ or $\bar{B}_0 = L$ | $\bar{A}_1$ or $\bar{B}_1 = L$ | $\bar{A}_2$ or $\bar{B}_2 = L$ | $\bar{A}_3$ or $\bar{B}_3 = L$ | H         | L         | H                  |
| L              | $\bar{A}_0$ or $\bar{B}_0 = L$ | $\bar{A}_1$ or $\bar{B}_1 = L$ | $\bar{A}_2$ or $\bar{B}_2 = L$ | $\bar{A}_3$ or $\bar{B}_3 = L$ | H         | L         | L                  |
| X              | $\bar{A}_0 = \bar{B}_0 = H$    | X                              | X                              | X                              | H         | H         | L                  |
| X              | X                              | $\bar{A}_1 = \bar{B}_1 = H$    | X                              | X                              | H         | H         | L                  |
| X              | X                              | X                              | $\bar{A}_2 = \bar{B}_2 = H$    | X                              | H         | H         | L                  |
| X              | X                              | X                              | X                              | $\bar{A}_3 = \bar{B}_3 = H$    | H         | H         | L                  |

The combination of signals on the S3 through S0 control lines determine the operation performed on the data words to generate the output bits  $\bar{F}_i$ . By monitoring the  $\bar{P}$  and  $C_n + 4$  outputs, the user can determine if all pairs of input bits are equal (see table above) or if any pair of inputs are both high (see table above). The 'AS881A has the unique feature of providing an  $A = B$  status while the exclusive-OR ( $\oplus$ ) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H; a status check is generated to determine whether all pairs ( $\bar{A}_i$ ,  $\bar{B}_i$ ) are equal in the following manner:  $\bar{P} = (\bar{A}_0 \oplus \bar{B}_0) + (\bar{A}_1 \oplus \bar{B}_1) + (\bar{A}_2 \oplus \bar{B}_2) + (\bar{A}_3 \oplus \bar{B}_3)$ . This unique bit-by-bit comparison of the data words, which is available on the totem-pole  $\bar{P}$  output, is particularly useful when cascading 'AS881s. As the  $A = B$  condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ( $\bar{P}$  and  $\bar{G}$ ). Thus the  $A = B$  status is transmitted to the second stage more quickly without the need for external multiplexing logic. The  $A = B$  open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ( $\bar{A}_i$ ,  $\bar{B}_i$ ) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner:  $\bar{P} = \bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$ .

| S3 | S2 | S1 | S0 | M | $\bar{P} = F_0 + F_1 + F_2 + F_3$                                                                                           |
|----|----|----|----|---|-----------------------------------------------------------------------------------------------------------------------------|
| L  | H  | L  | L  | H | $\bar{A}_0\bar{B}_0 + \bar{A}_1\bar{B}_1 + \bar{A}_2\bar{B}_2 + \bar{A}_3\bar{B}_3$                                         |
| H  | L  | L  | H  | H | $(\bar{A}_0 \oplus \bar{B}_0) + (\bar{A}_1 \oplus \bar{B}_1) + (\bar{A}_2 \oplus \bar{B}_2) + (\bar{A}_3 \oplus \bar{B}_3)$ |

## signal designations

In both Figures 1 and 2, the polarity indicators ( $\nabla$ ) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181A and 'AS881A together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

# SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

2

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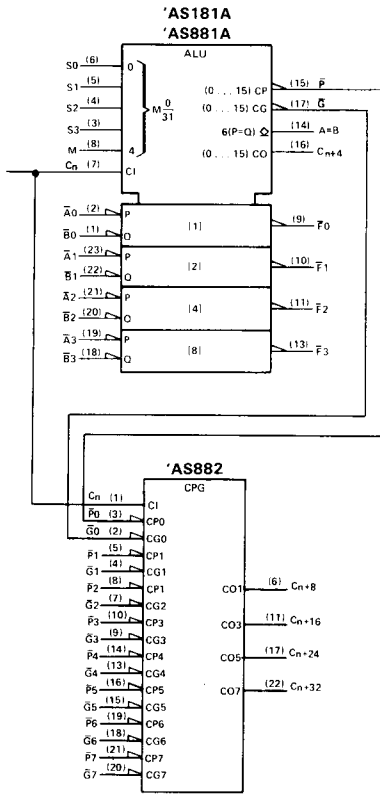


FIGURE 1  
(USE WITH TABLE 1)

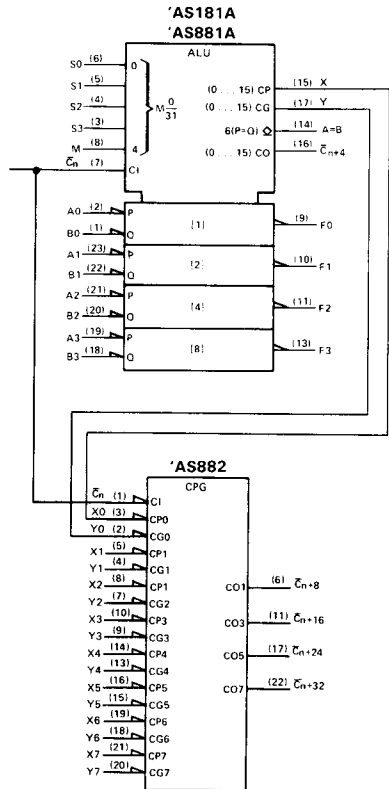


FIGURE 2  
(USE WITH TABLE 2)

TABLE 1

| SELECTION |    |    |    |    | ACTIVE-LOW DATA              |                                                |                                                                |
|-----------|----|----|----|----|------------------------------|------------------------------------------------|----------------------------------------------------------------|
|           | S3 | S2 | S1 | S0 | M = L; ARITHMETIC OPERATIONS |                                                |                                                                |
|           |    |    |    |    | LOGIC FUNCTIONS              | $C_n = L$<br>(no carry)                        | $C_n = H$<br>(with carry)                                      |
| L L L L   | L  | L  | L  | L  | $F = \bar{A}$                | $F = A \text{ MINUS } 1$                       | $F = A$                                                        |
| L L L L   | L  | L  | L  | H  | $F = \bar{A}\bar{B}$         | $F = AB \text{ MINUS } 1$                      | $F = AB$                                                       |
| L L L L   | L  | L  | H  | L  | $F = \bar{A} + B$            | $F = AB \text{ MINUS } 1$                      | $F = A\bar{B}$                                                 |
| L L L L   | L  | L  | H  | H  | $F = 1$                      | $F = \text{MINUS } 1 (2's \text{ COMP})$       | $F = \text{ZERO}$                                              |
| L L L L   | L  | H  | L  | L  | $F = A \oplus \bar{B}$       | $F = A \text{ PLUS } (A \cdot \bar{B})$        | $F = A \text{ PLUS } (A \cdot \bar{B}) \text{ PLUS } 1$        |
| L L L L   | L  | H  | L  | H  | $F = \bar{B}$                | $F = AB \text{ PLUS } (A \cdot \bar{B})$       | $F = AB \text{ PLUS } (A \cdot \bar{B}) \text{ PLUS } 1$       |
| L L L L   | L  | H  | H  | L  | $F = A \ominus B$            | $F = A \text{ MINUS } B \text{ MINUS } 1$      | $F = A \text{ MINUS } B$                                       |
| L L L L   | L  | H  | H  | H  | $F = A + \bar{B}$            | $F = A + \bar{B}$                              | $F = (A + \bar{B}) \text{ PLUS } 1$                            |
| H L L L   | L  | L  | L  | L  | $F = \bar{A}B$               | $F = A \text{ PLUS } (A \cdot B)$              | $F = A \text{ PLUS } (A \cdot B) \text{ PLUS } 1$              |
| H L L L   | L  | L  | L  | H  | $F = A \oplus B$             | $F = A \text{ PLUS } B$                        | $F = A \text{ PLUS } B \text{ PLUS } 1$                        |
| H L L L   | L  | L  | H  | L  | $F = B$                      | $F = \bar{A}\bar{B} \text{ PLUS } (A \cdot B)$ | $F = \bar{A}\bar{B} \text{ PLUS } (A \cdot B) \text{ PLUS } 1$ |
| H L L L   | L  | L  | H  | H  | $F = A + B$                  | $F = (A + B)$                                  | $F = (A + B) \text{ PLUS } 1$                                  |
| H L L L   | L  | H  | L  | L  | $F = 0$                      | $F = A \text{ PLUS } A^1$                      | $F = A \text{ PLUS } A \text{ PLUS } 1$                        |
| H L L L   | L  | H  | L  | H  | $F = \bar{A}\bar{B}$         | $F = AB \text{ PLUS } A$                       | $F = AB \text{ PLUS } A \text{ PLUS } 1$                       |
| H L L L   | L  | H  | H  | L  | $F = AB$                     | $F = \bar{A}\bar{B} \text{ PLUS } A$           | $F = \bar{A}\bar{B} \text{ PLUS } A \text{ PLUS } 1$           |
| H L L L   | L  | H  | H  | H  | $F = A$                      | $F = A$                                        | $F = A \text{ PLUS } 1$                                        |

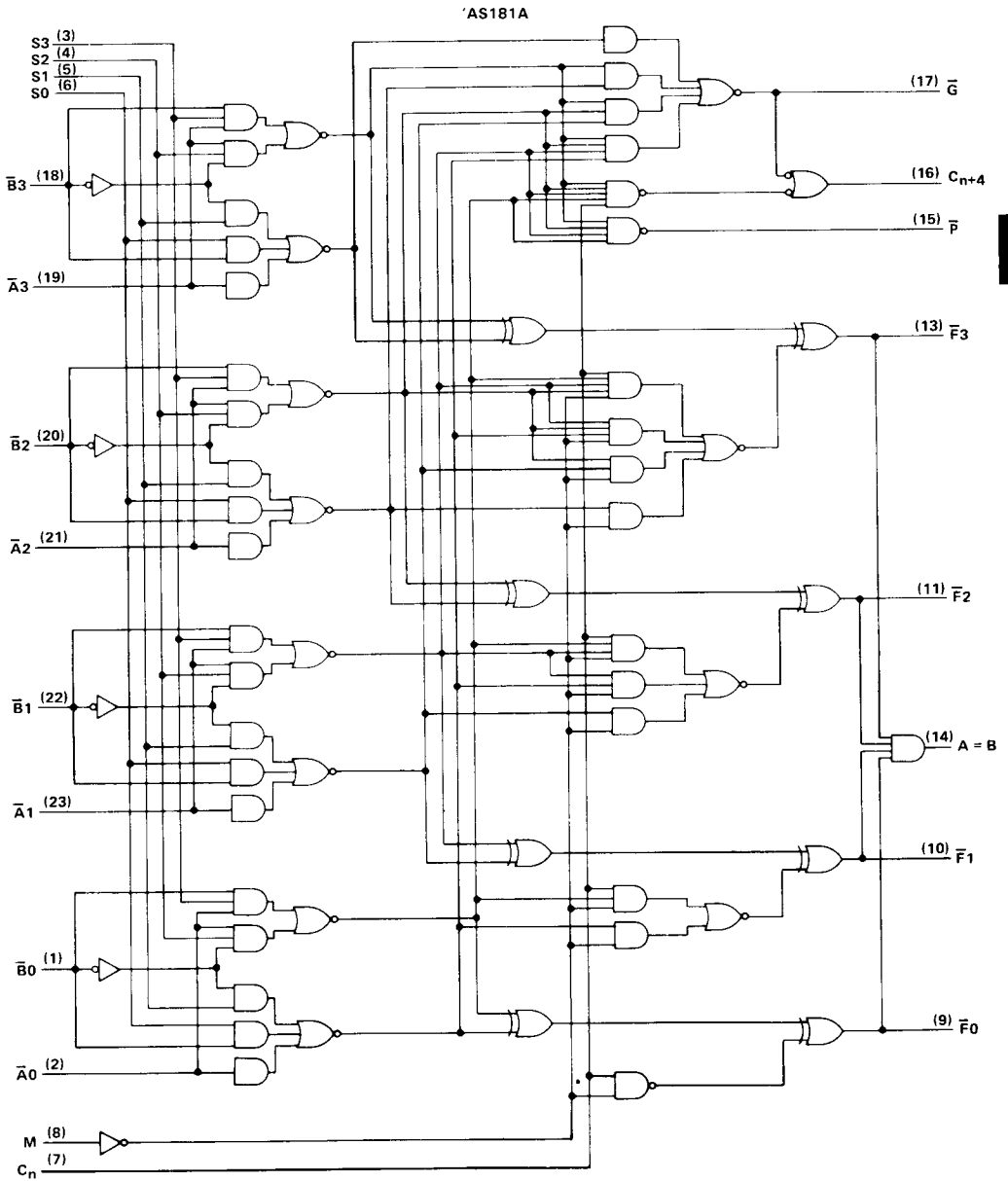
TABLE 2

| SELECTION |    |    |    |    | ACTIVE-HIGH DATA             |                                            |                                                            |
|-----------|----|----|----|----|------------------------------|--------------------------------------------|------------------------------------------------------------|
|           | S3 | S2 | S1 | S0 | M = L; ARITHMETIC OPERATIONS |                                            |                                                            |
|           |    |    |    |    | LOGIC FUNCTIONS              | $C_n = H$<br>(no carry)                    | $C_n = L$<br>(with carry)                                  |
| L L L L   | L  | L  | L  | L  | $F = \bar{A}$                | $F = A$                                    | $F = A \text{ PLUS } 1$                                    |
| L L L L   | L  | L  | L  | H  | $F = \bar{A} + B$            | $F = A + B$                                | $F = (A + B) \text{ PLUS } 1$                              |
| L L L L   | L  | L  | H  | L  | $F = \bar{A}\bar{B}$         | $F = A + \bar{B}$                          | $F = (A + \bar{B}) \text{ PLUS } 1$                        |
| L L L L   | L  | L  | H  | H  | $F = 0$                      | $F = \text{MINUS } 1 (2's \text{ COMPL})$  | $F = \text{ZERO}$                                          |
| L L L L   | L  | H  | L  | L  | $F = \bar{A}\bar{B}$         | $F = A \text{ PLUS } \bar{A}\bar{B}$       | $F = A \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$       |
| L L L L   | L  | H  | L  | H  | $F = \bar{B}$                | $F = (A + B) \text{ PLUS } \bar{A}\bar{B}$ | $F = (A + B) \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$ |
| L L L L   | L  | H  | H  | L  | $F = A \ominus B$            | $F = A \text{ MINUS } B \text{ MINUS } 1$  | $F = A \text{ MINUS } B$                                   |
| L L L L   | L  | H  | H  | H  | $F = \bar{A}\bar{B}$         | $F = \bar{A}\bar{B} \text{ MINUS } 1$      | $F = \bar{A}\bar{B}$                                       |
| H L L L   | L  | L  | L  | L  | $F = \bar{A}B$               | $F = A \text{ PLUS } \bar{A}B$             | $F = A \text{ PLUS } \bar{A}B \text{ PLUS } 1$             |
| H L L L   | L  | L  | L  | H  | $F = \bar{A} + B$            | $F = A + \bar{B}$                          | $F = (A + \bar{B}) \text{ PLUS } 1$                        |
| H L L L   | L  | L  | H  | L  | $F = B$                      | $F = (A + B) \text{ PLUS } \bar{A}B$       | $F = (A + \bar{B}) \text{ PLUS } \bar{A}B \text{ PLUS } 1$ |
| H L L L   | L  | L  | H  | H  | $F = A + B$                  | $F = AB \text{ MINUS } 1$                  | $F = AB$                                                   |
| H L L L   | L  | H  | L  | L  | $F = 1$                      | $F = A \text{ PLUS } A^1$                  | $F = A \text{ PLUS } A \text{ PLUS } 1$                    |
| H L L L   | L  | H  | L  | H  | $F = \bar{A} + \bar{B}$      | $F = (A + B) \text{ PLUS } A$              | $F = (A + B) \text{ PLUS } A \text{ PLUS } 1$              |
| H L L L   | L  | H  | H  | L  | $F = A + B$                  | $F = (A + \bar{B}) \text{ PLUS } A$        | $F = (A + \bar{B}) \text{ PLUS } A \text{ PLUS } 1$        |
| H L L L   | L  | H  | H  | H  | $F = A$                      | $F = A \text{ MINUS } 1$                   | $F = A$                                                    |

<sup>1</sup>Each bit is shifted to the next more significant position.

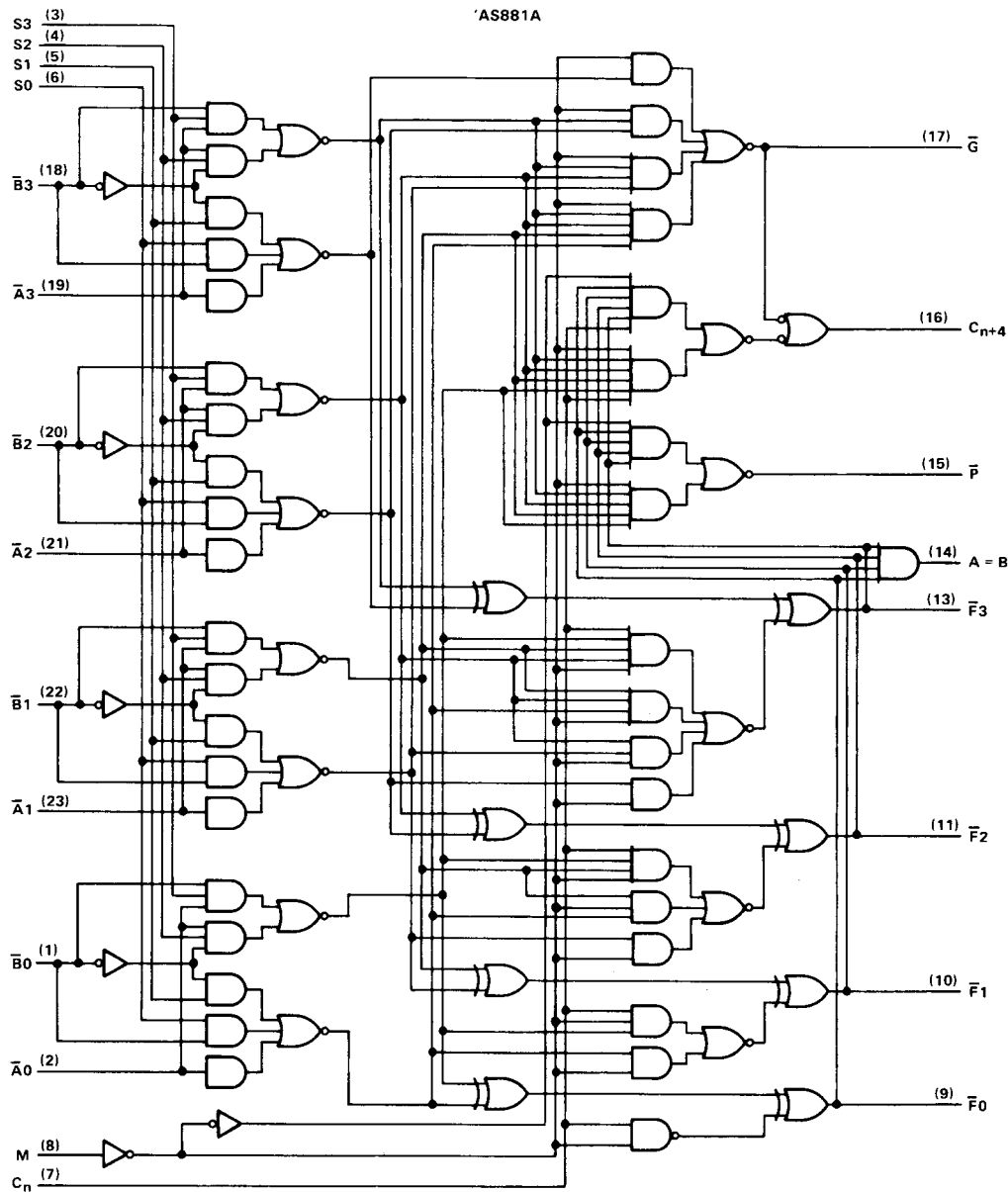
# SN54AS181A, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)



# **SN54AS881A, SN74AS881A** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

logic diagram (positive logic)



Pin numbers shown are for DW, JT, JW, NT, and NW packages.

2

ALS and AS Circuits

# SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                              |                |
|--------------------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$                                     | 7 V            |
| Input voltage                                                | 7 V            |
| Off-state output voltage (A=B output only)                   | 7 V            |
| Operating free-air temperature range: SN54AS181A, SN54AS881A | -55°C to 125°C |
| SN74AS181A, SN74AS881A                                       | 0°C to 70°C    |
| Storage temperature range                                    | -65°C to 150°C |

recommended operating conditions

|          |                                |                                           | SN54AS' |     |     | SN74AS' |     |     | UNIT |
|----------|--------------------------------|-------------------------------------------|---------|-----|-----|---------|-----|-----|------|
|          |                                |                                           | MIN     | NOM | MAX | MIN     | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 |                                           | 4.5     | 5   | 5.5 | 4.5     | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       |                                           | 2       |     |     | 2       |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |                                           |         |     | 0.8 |         |     | 0.8 | V    |
| $V_{OH}$ | High-level output voltage      | A = B output only                         |         |     | 5.5 |         |     | 5.5 | V    |
| $I_{OH}$ | High-level output current      | All outputs except<br>A = B and $\bar{G}$ |         |     | -2  |         |     | -2  | mA   |
|          |                                | $\bar{G}$                                 |         |     | -3  |         |     | -3  | mA   |
| $I_{OL}$ | Low-level output current       | All outputs<br>except $\bar{G}$           |         |     | 20  |         |     | 20  | mA   |
|          |                                | $\bar{G}$                                 |         |     | 48  |         |     | 48  | mA   |
| $T_A$    | Operating free-air temperature |                                           | -55     |     | 125 | 0       |     | 70  | °C   |

2

ALS and AS Circuits

# **SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                                             | TEST CONDITIONS                                           |         | SN54AS'             |                  |      | SN74AS'             |                  |      | UNIT |
|-----------------------------|---------------------------------------------|-----------------------------------------------------------|---------|---------------------|------------------|------|---------------------|------------------|------|------|
|                             |                                             |                                                           |         | MIN                 | TYP <sup>†</sup> | MAX  | MIN                 | TYP <sup>†</sup> | MAX  |      |
| V <sub>IK</sub>             |                                             | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA          |         | -1.2                |                  |      | -1.2                |                  |      | V    |
| V <sub>OH</sub>             | Any output except A = B                     | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA |         | V <sub>CC</sub> - 2 |                  |      | V <sub>CC</sub> - 2 |                  |      | V    |
|                             | $\overline{G}$                              | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA          |         | 2.4                 | 3.4              |      | 2.4                 | 3.4              |      | V    |
| I <sub>OH</sub>             | A = B                                       | V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V          |         | 0.1                 |                  |      | 0.1                 |                  |      | mA   |
| V <sub>OL</sub>             | Any output except $\overline{G}$            | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA          |         | 0.3                 | 0.5              |      | 0.3                 | 0.5              |      | V    |
|                             | $\overline{G}$                              | V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA          |         | 0.4                 | 0.5              |      | 0.4                 | 0.5              |      | V    |
| I <sub>I</sub>              | M input                                     | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V             |         | 0.1                 |                  |      | 0.1                 |                  |      | mA   |
|                             | 0.3                                         |                                                           |         | 0.3                 |                  |      |                     |                  |      |      |
|                             | 0.4                                         |                                                           |         | 0.4                 |                  |      |                     |                  |      |      |
|                             | 0.6                                         |                                                           |         | 0.6                 |                  |      |                     |                  |      |      |
| I <sub>IH</sub>             | M input                                     | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V           |         | 20                  |                  |      | 20                  |                  |      | μA   |
|                             | 60                                          |                                                           |         | 60                  |                  |      |                     |                  |      |      |
|                             | 80                                          |                                                           |         | 80                  |                  |      |                     |                  |      |      |
|                             | 120                                         |                                                           |         | 120                 |                  |      |                     |                  |      |      |
| I <sub>IL</sub>             | M input                                     | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V           |         | -2                  |                  |      | -2                  |                  |      | mA   |
|                             | -6                                          |                                                           |         | -6                  |                  |      |                     |                  |      |      |
|                             | -8                                          |                                                           |         | -8                  |                  |      |                     |                  |      |      |
|                             | -12                                         |                                                           |         | -12                 |                  |      |                     |                  |      |      |
| I <sub>O</sub> <sup>‡</sup> | All outputs except A = B and $\overline{G}$ | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V          |         | -30                 | -45              | -112 | -30                 | -45              | -112 | mA   |
|                             | -165                                        |                                                           |         | -165                |                  |      |                     |                  |      |      |
| I <sub>CC</sub>             |                                             | V <sub>CC</sub> = 5.5 V                                   | 'AS181A | 135                 | 200              |      | 135                 | 200              |      | mA   |
|                             |                                             |                                                           | 'AS881A | 135                 | 210              |      | 135                 | 210              |      |      |

<sup>†</sup>All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

<sup>†</sup>The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current,  $I_{OS}$ .



# SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

switching characteristics (see Note 1)

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT)     | TEST<br>CONDITIONS                                     | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 500 Ω<br>(280 Ω for A = B),<br>T <sub>A</sub> = 25 °C | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF (15 pF for A = B),<br>R <sub>L</sub> = 500 Ω (280 Ω for A = B),<br>T <sub>A</sub> = MIN to MAX |                          |    | UNIT |
|-----------------|-----------------|--------------------|--------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|----|------|
|                 |                 |                    |                                                        | 'AS181A<br>'AS881A                                                                                                          | SN54AS181A<br>SN54AS881A                                                                                                                                   | SN74AS181A<br>SN74AS881A |    |      |
|                 |                 |                    |                                                        | MIN TYP <sup>†</sup> MAX                                                                                                    | MIN TYP <sup>†</sup> MAX                                                                                                                                   | MIN TYP <sup>†</sup> MAX |    |      |
|                 |                 |                    |                                                        |                                                                                                                             |                                                                                                                                                            |                          |    |      |
| t <sub>pd</sub> | C <sub>n</sub>  | C <sub>n</sub> + 4 |                                                        | 5                                                                                                                           | 2 7 11                                                                                                                                                     | 2 7 9                    | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | C <sub>n</sub> + 4 | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 6                                                                                                                           | 2 8 14                                                                                                                                                     | 2 8 12                   | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | C <sub>n</sub> + 4 | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 7                                                                                                                           | 2 8 20                                                                                                                                                     | 2 8 16                   | ns |      |
| t <sub>pd</sub> | C <sub>n</sub>  | Any F̅             | M = 0 V (SUM or DIFF mode)                             | 5                                                                                                                           | 3 6 11                                                                                                                                                     | 3 6 9                    | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | G̅                 | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 4                                                                                                                           | 2 5 9                                                                                                                                                      | 2 5 7                    | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | G̅                 | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 5                                                                                                                           | 2 6 12                                                                                                                                                     | 2 6 9                    | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | P̅                 | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 5                                                                                                                           | 2 6 11                                                                                                                                                     | 2 6 8                    | ns |      |
| t <sub>pd</sub> | Any<br>A̅ or B̅ | P̅                 | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 5                                                                                                                           | 2 6 13                                                                                                                                                     | 2 6 10                   | ns |      |
| t <sub>pd</sub> | A̅i or<br>B̅i   | F̅i                | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 5                                                                                                                           | 2 5 11                                                                                                                                                     | 2 5 8                    | ns |      |
| t <sub>pd</sub> | A̅i or<br>B̅i   | F̅i                | M = 0 V, S0 = S1 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 5                                                                                                                           | 2 6 12                                                                                                                                                     | 2 6 10                   | ns |      |
| t <sub>pd</sub> | A̅i or<br>B̅i   | F̅i                | M = 4.5 V (LOGIC mode)                                 | 6                                                                                                                           | 2 6 16                                                                                                                                                     | 2 6 11                   | ns |      |
| t <sub>pd</sub> | Any A̅<br>or B̅ | A = B              | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 12                                                                                                                          | 4 14 26                                                                                                                                                    | 4 14 21                  | ns |      |

additional 'AS881A switching characteristics involving status checks (see Note 1)

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT)     | TEST<br>CONDITIONS                                                                                                                                                                                      | V <sub>CC</sub> = 5 V,<br>C <sub>L</sub> = 15 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = 25 °C | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX |              |    | UNIT |
|-----------------|-----------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|--------------|----|------|
|                 |                 |                    |                                                                                                                                                                                                         | AS881A                                                                                                 | SN54AS881A                                                                                                             | SN74AS881A   |    |      |
|                 |                 |                    |                                                                                                                                                                                                         | MIN TYP† MAX                                                                                           | MIN TYP† MAX                                                                                                           | MIN TYP† MAX |    |      |
| t <sub>pd</sub> | Any<br>A or B   | P                  | C <sub>n</sub> = 4.5 V, M = 4.5 V,<br>S <sub>0</sub> = S <sub>3</sub> = 4.5 V, S <sub>1</sub> = S <sub>2</sub> = 0 V,<br>Equality (A <sub>i</sub> = B <sub>i</sub> or A <sub>i</sub> ≠ B <sub>i</sub> ) | 8                                                                                                      | 2 10 19                                                                                                                | 2 10 15      | ns |      |
| t <sub>pd</sub> | Any<br>A or B   | C <sub>n</sub> + 4 | C <sub>n</sub> = 4.5 V, M = 4.5 V,<br>S <sub>0</sub> = S <sub>3</sub> = 4.5 V, S <sub>1</sub> = S <sub>2</sub> = 0 V,<br>Equality (A <sub>i</sub> = B <sub>i</sub> or A <sub>i</sub> ≠ B <sub>i</sub> ) | 10                                                                                                     | 2 12 24                                                                                                                | 2 12 18      | ns |      |
| t <sub>pd</sub> | Any<br>A or B   | P                  | C <sub>n</sub> = 4.5 V, M = 4.5 V,<br>S <sub>2</sub> = 4.5 V, S <sub>0</sub> = S <sub>1</sub> = S <sub>3</sub> = 0 V,<br>(A <sub>i</sub> = B <sub>i</sub> = H or A <sub>i</sub> or B <sub>i</sub> = L)  | 8                                                                                                      | 2 10 19                                                                                                                | 2 10 15      | ns |      |
| t <sub>pd</sub> | Any<br>A or B   | C <sub>n</sub> + 4 | C <sub>n</sub> = 4.5 V, M = 4.5 V,<br>S <sub>2</sub> = 4.5 V, S <sub>0</sub> = S <sub>1</sub> = S <sub>3</sub> = 0 V,<br>(A <sub>i</sub> = B <sub>i</sub> = H or A <sub>i</sub> or B <sub>i</sub> = L)  | †1                                                                                                     | 2 13 25                                                                                                                | 2 13 19      | ns |      |

t<sub>pd</sub> = t<sub>PHL</sub> or t<sub>PLH</sub>

<sup>†</sup>All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25 °C.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

# **SN54AS181A, SN54AS881A, SN74AS181A, SN74AS881A** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

## **PARAMETER MEASUREMENT INFORMATION**

**SUM MODE TEST TABLE**

FUNCTION INPUTS:  $S_0 = S_3 = 4.5 \text{ V}$ ,  $S_1 = S_2 = M = 0 \text{ V}$

| PARAMETER              | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS                 |                                           | OUTPUT UNDER TEST          | OUTPUT WAVEFORM (SEE NOTE 1) |
|------------------------|------------------|----------------------|-------------|-----------------------------------|-------------------------------------------|----------------------------|------------------------------|
|                        |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                       | APPLY GND                                 |                            |                              |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $C_n$            | None                 | None        | All $\bar{A}$                     | All $\bar{B}$                             | Any $\bar{F}$ or $C_n + 4$ | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_n + 4$                  | Out-of-Phase                 |

**DIFF MODE TEST TABLE**

FUNCTION INPUTS:  $S_1 = S_2 = 4.5 \text{ V}$ ,  $S_0 = S_3 = M = 0 \text{ V}$

| PARAMETER              | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS           |                                           | OUTPUT UNDER TEST          | OUTPUT WAVEFORM (SEE NOTE 1) |
|------------------------|------------------|----------------------|-------------|-----------------------------|-------------------------------------------|----------------------------|------------------------------|
|                        |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                 | APPLY GND                                 |                            |                              |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | remaining $\bar{B}$ , $C_n$               | $A = B$                    | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$                    | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $C_n$            | None                 | None        | All $\bar{A}$ and $\bar{B}$ | None                                      | $C_n + 4$ or any $\bar{F}$ | In-Phase                     |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PLH}$<br>$t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | In-Phase                     |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

# PRODUCT PREVIEW

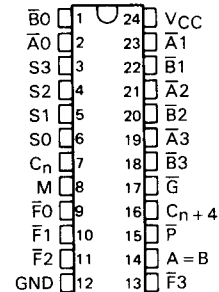
# SN54AS181B, SN74AS181B ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

D2661, DECEMBER 1985—REVISED MAY 1986

- Package Options Include Compact 300-mil or Standard 600-mil DIPs and Both Plastic and Ceramic Chip Carriers
- Full Look-Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
- Dependable Texas Instruments Quality and Reliability

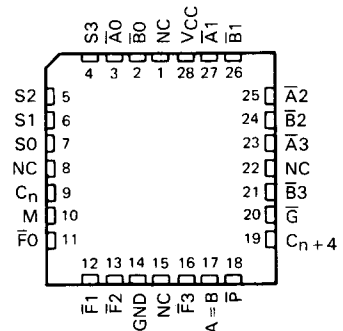
SN54AS181B ... JT OR JW PACKAGE  
SN74AS181B ... N OR NT PACKAGE

(TOP VIEW)



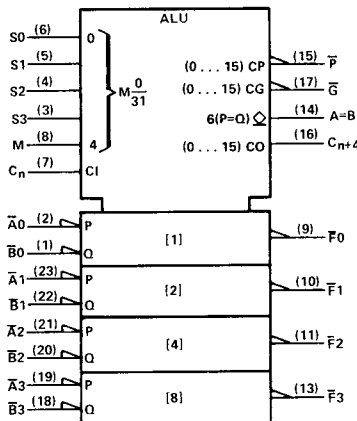
SN54AS181B ... FK PACKAGE  
SN74AS181B ... FN PACKAGE

(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J, JT, N, and NT packages.

TYPICAL ADDITION TIMES ( $C_L = 15 \text{ pF}$ ,  $R_L = 280 \Omega$ ,  $T_A = 25^\circ\text{C}$ )

| NUMBER<br>OF<br>BITS | ADDITION TIMES              |                             |                          | PACKAGE COUNT             |                                | CARRY METHOD<br>BETWEEN<br>ALUs |
|----------------------|-----------------------------|-----------------------------|--------------------------|---------------------------|--------------------------------|---------------------------------|
|                      | USING 'AS181B<br>AND 'AS882 | USING 'AS881B<br>AND 'AS882 | USING 'S181<br>AND 'S182 | ARITHMETIC<br>LOGIC UNITS | LOOK-AHEAD<br>CARRY GENERATORS |                                 |
| 1 to 4               | 5 ns                        | 5 ns                        | 11 ns                    | 1                         |                                | NONE                            |
| 5 to 8               | 10 ns                       | 10 ns                       | 18 ns                    | 2                         |                                | RIPPLE                          |
| 9 to 16              | 14 ns                       | 14 ns                       | 19 ns                    | 3 or 4                    | 1                              | FULL LOOK-AHEAD                 |
| 17 to 64             | 19 ns                       | 19 ns                       | 28 ns                    | 5 to 16                   | 2 to 5                         | FULL LOOK-AHEAD                 |

## SN54AS181B, SN74AS181B ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

### description

The 'AS181B arithmetic logic units (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs,  $\bar{G}$  and  $\bar{P}$ , for the four bits in the package. When used in conjunction with the SN54AS882 or SN74AS882 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multilevel full carry look-ahead is illustrated under signal designations.

If high speed is not of importance, a ripple-carry input ( $C_n$ ) and a ripple-carry output ( $C_n + 4$ ) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 'AS181B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

| PIN NUMBER                 | 2          | 1          | 23         | 22         | 21         | 20         | 19         | 18         | 9          | 10         | 11         | 13         | 7     | 16        | 15        | 17        |
|----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------|-----------|-----------|-----------|
| Active-low data (Table 1)  | $\bar{A}0$ | $\bar{B}0$ | $\bar{A}1$ | $\bar{B}1$ | $\bar{A}2$ | $\bar{B}2$ | $\bar{A}3$ | $\bar{B}3$ | $\bar{F}0$ | $\bar{F}1$ | $\bar{F}2$ | $\bar{F}3$ | $C_n$ | $C_n + 4$ | $\bar{P}$ | $\bar{G}$ |
| Active-high data (Table 2) | A0         | B0         | A1         | B1         | A2         | B2         | A3         | B3         | F0         | F1         | F2         | F3         | $C_n$ | $C_n + 4$ | X         | Y         |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is  $A - B - 1$ , which requires an end-around or forced carry to provide  $A - B$ .

The 'AS181B can also be utilized as a comparator. The  $A = B$  output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ( $A = B$ ). The ALU must be in the subtract mode with  $C_n = H$  when performing this comparison. The  $A = B$  output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output ( $C_n + 4$ ) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

| INPUT $C_n$ | OUTPUT $C_n + 4$ | ACTIVE-LOW DATA<br>(FIGURE 1) | ACTIVE-HIGH DATA<br>(FIGURE 2) |
|-------------|------------------|-------------------------------|--------------------------------|
| H           | H                | $A \geq B$                    | $A \leq B$                     |
| H           | L                | $A < B$                       | $A > B$                        |
| L           | H                | $A > B$                       | $A < B$                        |
| L           | L                | $A \leq B$                    | $A \geq B$                     |

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

# SN54AS181B, SN74AS181B ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

## signal designations

In both Figures 1 and 2, the polarity indicators ( $\triangle$ ) indicate that the associated input or output is active-low with respect to the function shown inside the symbol and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'AS181B together with 'AS882 and 'S182 can be used with the signal designation of either Figure 1 or Figure 2.

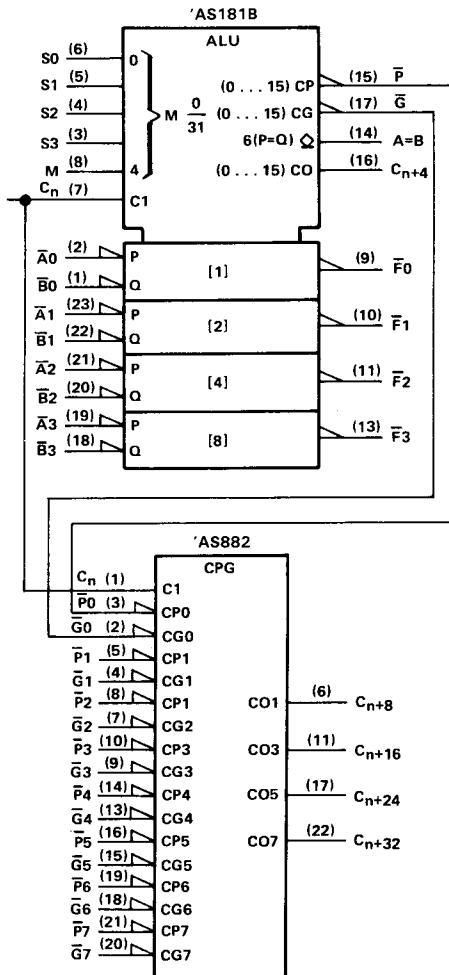


FIGURE 1  
(USE WITH TABLE I)

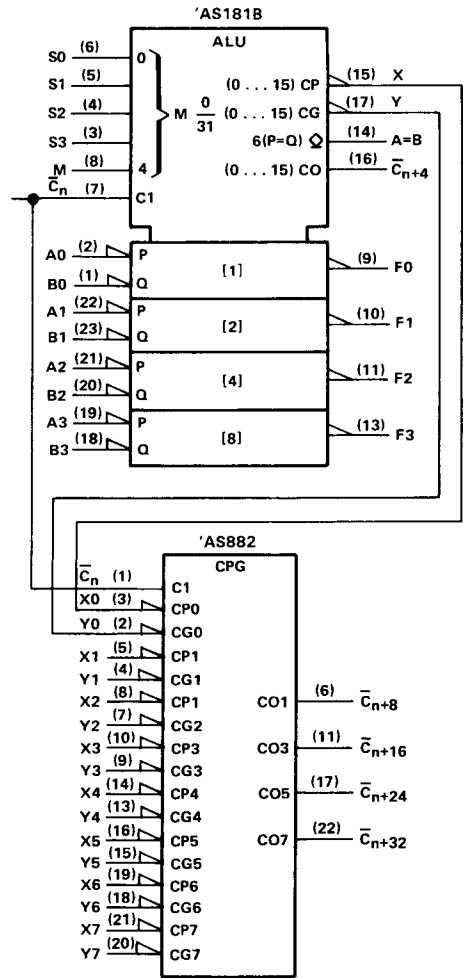


FIGURE 2  
(USE WITH TABLE II)

**SN54AS181B, SN74AS181B**  
**ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

**TABLE I**

| SELECTION |    |    |    |  | ACTIVE-LOW DATA              |                                           |                                                      |
|-----------|----|----|----|--|------------------------------|-------------------------------------------|------------------------------------------------------|
|           |    |    |    |  | M = H<br>LOGIC<br>FUNCTIONS  | M = L: ARITHMETIC OPERATIONS              |                                                      |
| S3        | S2 | S1 | S0 |  |                              | C <sub>n</sub> = L<br>(no carry)          | C <sub>n</sub> = H<br>(with carry)                   |
| L         | L  | L  | L  |  | $F = \bar{A}$                | $F = A \text{ MINUS } 1$                  | $F = A$                                              |
| L         | L  | L  | H  |  | $F = \bar{A}\bar{B}$         | $F = AB \text{ MINUS } 1$                 | $F = AB$                                             |
| L         | L  | H  | L  |  | $F = \bar{A} + B$            | $F = A\bar{B} \text{ MINUS } 1$           | $F = A\bar{B}$                                       |
| L         | L  | H  | H  |  | $F = 1$                      | $F = \text{MINUS } 1 \text{ (2's COMP)}$  | $F = \text{ZERO}$                                    |
| L         | H  | L  | L  |  | $F = \bar{A} + \bar{B}$      | $F = A \text{ PLUS } (A + \bar{B})$       | $F = A \text{ PLUS } (A + \bar{B}) \text{ PLUS } 1$  |
| L         | H  | L  | H  |  | $F = \bar{B}$                | $F = AB \text{ PLUS } (A + \bar{B})$      | $F = AB \text{ PLUS } (A + \bar{B}) \text{ PLUS } 1$ |
| L         | H  | H  | L  |  | $F = \bar{A} \oplus \bar{B}$ | $F = A \text{ MINUS } B \text{ MINUS } 1$ | $F = A \text{ MINUS } B$                             |
| L         | H  | H  | H  |  | $F = A + \bar{B}$            | $F = A + \bar{B}$                         | $F = (A + \bar{B}) \text{ PLUS } 1$                  |
| H         | L  | L  | L  |  | $F = \bar{A}B$               | $F = A \text{ PLUS } (A + B)$             | $F = A \text{ PLUS } (A + B) \text{ PLUS } 1$        |
| H         | L  | L  | H  |  | $F = A \oplus B$             | $F = A \text{ PLUS } B$                   | $F = A \text{ PLUS } B \text{ PLUS } 1$              |
| H         | L  | H  | L  |  | $F = B$                      | $F = A\bar{B} \text{ PLUS } (A + B)$      | $F = A\bar{B} \text{ PLUS } (A + B) \text{ PLUS } 1$ |
| H         | L  | H  | H  |  | $F = A + B$                  | $F = (A + B)$                             | $F = (A + B) \text{ PLUS } 1$                        |
| H         | H  | L  | L  |  | $F = 0$                      | $F = A \text{ PLUS } A^*$                 | $F = A \text{ PLUS } A \text{ PLUS } 1$              |
| H         | H  | L  | H  |  | $F = A\bar{B}$               | $F = AB \text{ PLUS } A$                  | $F = AB \text{ PLUS } A \text{ PLUS } 1$             |
| H         | H  | H  | L  |  | $F = AB$                     | $F = A\bar{B} \text{ PLUS } A$            | $F = A\bar{B} \text{ PLUS } A \text{ PLUS } 1$       |
| H         | H  | H  | H  |  | $F = A$                      | $F = A$                                   | $F = A \text{ PLUS } 1$                              |

**TABLE II**

| SELECTION |    |    |    |  | ACTIVE-HIGH DATA            |                                           |                                                      |
|-----------|----|----|----|--|-----------------------------|-------------------------------------------|------------------------------------------------------|
|           |    |    |    |  | M = H<br>LOGIC<br>FUNCTIONS | M = L: ARITHMETIC OPERATIONS              |                                                      |
| S3        | S2 | S1 | S0 |  |                             | C <sub>n</sub> = H<br>(no carry)          | C <sub>n</sub> = L<br>(with carry)                   |
| L         | L  | L  | L  |  | $F = \bar{A}$               | $F = A$                                   | $F = A \text{ PLUS } 1$                              |
| L         | L  | L  | H  |  | $F = \bar{A} + B$           | $F = A + B$                               | $F = (A + B) \text{ PLUS } 1$                        |
| L         | L  | H  | L  |  | $F = \bar{A}B$              | $F = A + \bar{B}$                         | $F = (A + \bar{B}) \text{ PLUS } 1$                  |
| L         | L  | H  | H  |  | $F = 0$                     | $F = \text{MINUS } 1 \text{ (2's COMP)}$  | $F = \text{ZERO}$                                    |
| L         | H  | L  | L  |  | $F = \bar{A}\bar{B}$        | $F = A \text{ PLUS } A\bar{B}$            | $F = A \text{ PLUS } A\bar{B} \text{ PLUS } 1$       |
| L         | H  | L  | H  |  | $F = \bar{B}$               | $F = (A + B) \text{ PLUS } A\bar{B}$      | $F = (A + B) \text{ PLUS } A\bar{B} \text{ PLUS } 1$ |
| L         | H  | H  | L  |  | $F = A \oplus B$            | $F = A \text{ MINUS } B \text{ MINUS } 1$ | $F = A \text{ MINUS } B$                             |
| L         | H  | H  | H  |  | $F = A\bar{B}$              | $F = A\bar{B} \text{ MINUS } 1$           | $F = A\bar{B}$                                       |
| H         | L  | L  | L  |  | $F = \bar{A} + B$           | $F = A \text{ PLUS } AB$                  | $F = A \text{ PLUS } AB \text{ PLUS } 1$             |
| H         | L  | L  | H  |  | $F = \bar{A} \oplus B$      | $F = A \text{ PLUS } B$                   | $F = A \text{ PLUS } B \text{ PLUS } 1$              |
| H         | L  | H  | L  |  | $F = B$                     | $F = (A + \bar{B}) \text{ PLUS } AB$      | $F = (A + \bar{B}) \text{ PLUS } AB \text{ PLUS } 1$ |
| H         | L  | H  | H  |  | $F = AB$                    | $F = AB \text{ MINUS } 1$                 | $F = AB$                                             |
| H         | H  | L  | L  |  | $F = 1$                     | $F = A \text{ PLUS } A^*$                 | $F = A \text{ PLUS } A \text{ PLUS } 1$              |
| H         | H  | L  | H  |  | $F = A + \bar{B}$           | $F = (A + B) \text{ PLUS } A$             | $A = (A + B) \text{ PLUS } A \text{ PLUS } 1$        |
| H         | H  | H  | L  |  | $F = A + B$                 | $F = (A + \bar{B}) \text{ PLUS } A$       | $F = (A + \bar{B}) \text{ PLUS } A \text{ PLUS } 1$  |
| H         | H  | H  | H  |  | $F = A$                     | $F = A \text{ MINUS } 1$                  | $F = A$                                              |

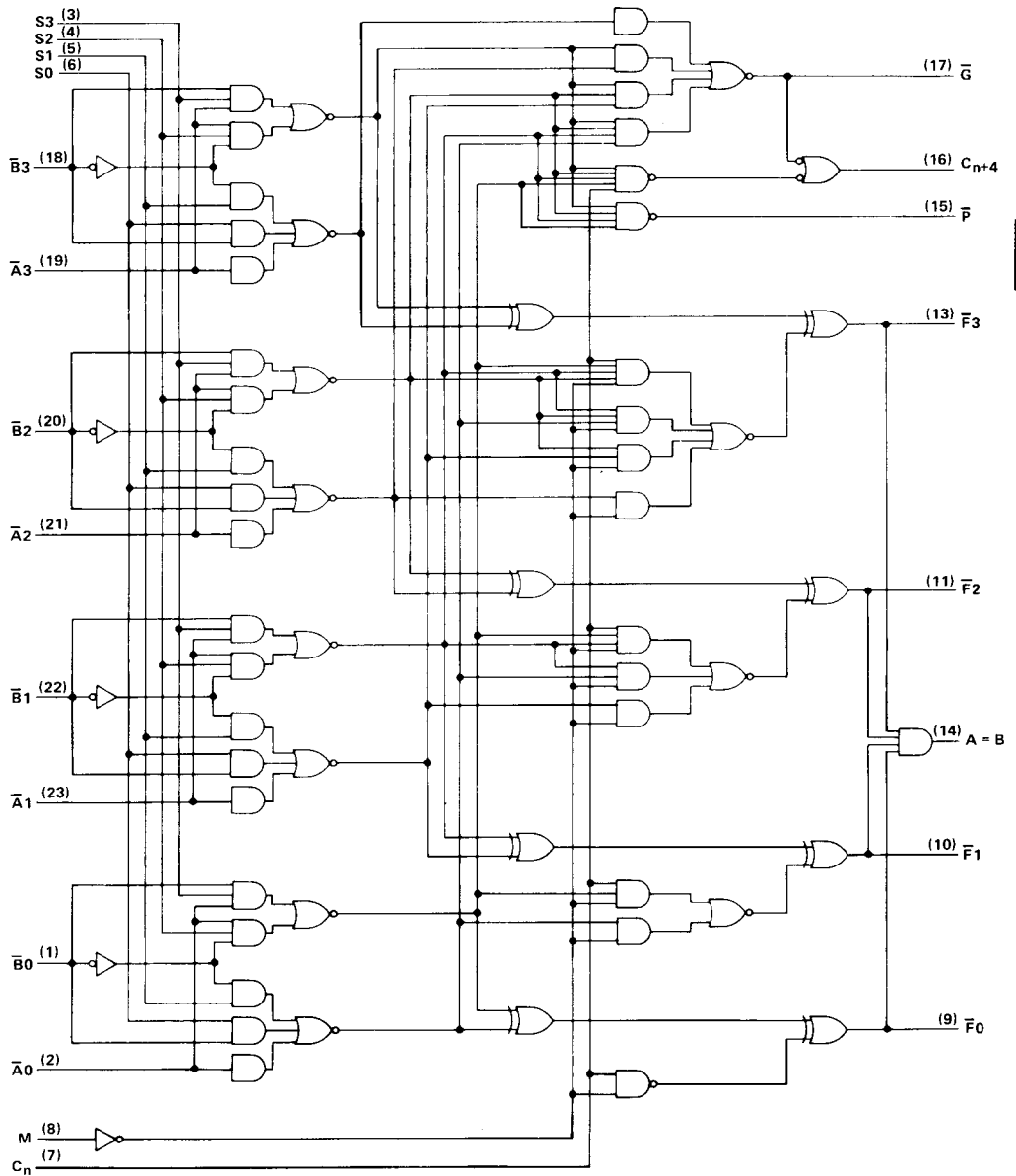
\*Each bit is shifted to the next more significant position.

2

ALS and AS Circuits

# SN54AS181B, SN74AS181B ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

logic diagram (positive logic)



Pin numbers shown are for J, JT, N, and NT packages.

# **SN54AS181B, SN74AS181B** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

|                                                        |                  |
|--------------------------------------------------------|------------------|
| Supply voltage, $V_{CC}$ .....                         | 7 V              |
| Input voltage .....                                    | 7 V              |
| Off-state output voltage (A=B output only) .....       | 7 V              |
| Operating free-air temperature range: SN54AS181B ..... | –55 °C to 125 °C |
| SN74AS181B .....                                       | 0 °C to 70 °C    |
| Storage temperature range .....                        | –65 °C to 150 °C |

## **recommended operating conditions**

|          |                                |                                                | SN54AS181B |     |     | SN74AS181B |     |     | UNIT |
|----------|--------------------------------|------------------------------------------------|------------|-----|-----|------------|-----|-----|------|
|          |                                |                                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 |                                                | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       |                                                | 2          |     |     | 2          |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |                                                |            |     | 0.8 |            |     | 0.8 | V    |
| $V_{OH}$ | High-level output voltage      | A = B output only                              |            |     | 5.5 |            |     | 5.5 | V    |
| $I_{OH}$ | High-level output current      | All outputs except<br>A = B and $\overline{G}$ |            |     | –2  |            |     | –2  | mA   |
|          |                                | $\overline{G}$                                 |            |     | –3  |            |     | –3  | mA   |
|          |                                |                                                |            |     |     |            |     |     |      |
| $I_{OL}$ | Low-level output current       | All outputs<br>except $\overline{G}$           |            |     | 20  |            |     | 20  | mA   |
|          |                                | $\overline{G}$                                 |            |     | 48  |            |     | 48  | mA   |
| $T_A$    | Operating free-air temperature |                                                | –55        |     | 125 | 0          |     | 70  | °C   |

2

ALS and AS Circuits



# SN54AS181B, SN74AS181B ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER      |                                          | TEST CONDITIONS                                                       | SN54AS181B   |      |      | SN74AS181B   |      |      | UNIT          |
|----------------|------------------------------------------|-----------------------------------------------------------------------|--------------|------|------|--------------|------|------|---------------|
|                |                                          |                                                                       | MIN          | TYP† | MAX  | MIN          | TYP† | MAX  |               |
| $V_{IK}$       |                                          | $V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$                     |              |      | -1.2 |              |      | -1.2 | V             |
| $V_{OH}$       | Any output except $A = B$                | $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -2 \text{ mA}$ | $V_{CC} - 2$ |      |      | $V_{CC} - 2$ |      |      | V             |
|                | $\bar{G}$                                | $V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -3 \text{ mA}$                   | 2.4          | 3.4  |      | 2.4          | 3.4  |      | V             |
| $I_{OH}$       | $A = B$                                  | $V_{CC} = 4.5 \text{ V}$ , $V_{OH} = 5.5 \text{ V}$                   |              |      | 0.1  |              |      | 0.1  | mA            |
| $V_{OL}$       | Any output except $\bar{G}$              | $V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 20 \text{ mA}$                   |              | 0.3  | 0.5  |              | 0.3  | 0.5  | V             |
|                | $\bar{G}$                                | $V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 48 \text{ mA}$                   |              | 0.4  | 0.5  |              | 0.4  | 0.5  | V             |
| $I_I$          | M input                                  | $V_{CC} = 5.5 \text{ V}$ , $V_I = 7 \text{ V}$                        |              |      | 0.1  |              |      | 0.1  | mA            |
|                | Any A or B input                         |                                                                       |              |      | 0.3  |              |      | 0.3  |               |
|                | Any S input                              |                                                                       |              |      | 0.4  |              |      | 0.4  |               |
|                | Carry input                              |                                                                       |              |      | 0.6  |              |      | 0.6  |               |
| $I_{IH}$       | M input                                  | $V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$                      |              |      | 20   |              |      | 20   | $\mu\text{A}$ |
|                | Any A or B input                         |                                                                       |              |      | 60   |              |      | 60   |               |
|                | Any S input                              |                                                                       |              |      | 80   |              |      | 80   |               |
|                | Carry input                              |                                                                       |              |      | 120  |              |      | 120  |               |
| $I_{IL}$       | M input                                  | $V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$                      |              |      | -0.5 |              |      | -0.5 | mA            |
|                | Any A or B input                         |                                                                       |              |      | -1.5 |              |      | -1.5 |               |
|                | Any S input                              |                                                                       |              |      | -2   |              |      | -2   |               |
|                | Carry input                              |                                                                       |              |      | -3   |              |      | -3   |               |
| $I_O^\ddagger$ | All outputs except $A = B$ and $\bar{G}$ | $V_{CC} = 5.5 \text{ V}$ , $V_O = 2.25 \text{ V}$                     | -30          | -45  | -112 | -30          | -45  | -112 | mA            |
|                | $\bar{G}$                                |                                                                       | -30          |      | -125 | -30          |      | -125 |               |
| $I_{CC}$       |                                          | $V_{CC} = 5.5 \text{ V}$                                              |              | 74   | 117  |              | 74   | 117  | mA            |

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current,  $I_{OS}$ .

# **SN54AS181B, SN74AS181B** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

switching characteristics (see Note 1)

| PARAMETER        | FROM<br>(INPUT)                    | TO<br>(OUTPUT)   | TEST CONDITIONS                                        | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX |      |            |      | UNIT |
|------------------|------------------------------------|------------------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------|------------|------|------|
|                  |                                    |                  |                                                        | SN54AS181B                                                                                                             |      | SN74AS181B |      |      |
|                  |                                    |                  |                                                        | MIN                                                                                                                    | MAX  | MIN        | MAX  |      |
| t <sub>PLH</sub> | C <sub>n</sub>                     | C <sub>n+4</sub> |                                                        | 3                                                                                                                      | 9    | 3          | 8.5  | ns   |
| t <sub>PHL</sub> |                                    |                  |                                                        | 2                                                                                                                      | 7    | 2          | 6.5  |      |
| t <sub>PLH</sub> | Any                                | C <sub>n+4</sub> | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 3.5                                                                                                                    | 13   | 5          | 12   | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 3.5                                                                                                                    | 12.5 | 5          | 12   |      |
| t <sub>PLH</sub> | Any                                | C <sub>n+4</sub> | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 5                                                                                                                      | 14.5 | 5          | 13   | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 5                                                                                                                      | 13.5 | 5          | 12.5 |      |
| t <sub>PLH</sub> | C <sub>n</sub>                     | Any F̅           | M = 0 V (SUM or DIFF mode)                             | 3                                                                                                                      | 10.5 | 3          | 9    | ns   |
| t <sub>PHL</sub> |                                    |                  |                                                        | 3                                                                                                                      | 8    | 3          | 7.5  |      |
| t <sub>PLH</sub> | Any                                | G̅               | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 3                                                                                                                      | 8.5  | 3          | 8    | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 2                                                                                                                      | 7    | 2          | 6    |      |
| t <sub>PLH</sub> | Any                                | G̅               | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 3                                                                                                                      | 10.5 | 3          | 9.5  | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 2                                                                                                                      | 9    | 2          | 7    |      |
| t <sub>PLH</sub> | Any                                | P̅               | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 3                                                                                                                      | 8.5  | 3          | 7.5  | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 2                                                                                                                      | 7.5  | 2          | 6    |      |
| t <sub>PLH</sub> | Any                                | P̅               | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 3                                                                                                                      | 10.5 | 3          | 9    | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 3                                                                                                                      | 8.5  | 3          | 8    |      |
| t <sub>PLH</sub> | A̅ <sub>i</sub> or                 | F̅ <sub>i</sub>  | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 3                                                                                                                      | 11   | 3          | 9.5  | ns   |
| t <sub>PHL</sub> | B̅ <sub>i</sub>                    |                  |                                                        | 3                                                                                                                      | 9    | 3          | 7.5  |      |
| t <sub>PLH</sub> | A̅ <sub>i</sub> or                 | F̅ <sub>i</sub>  | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 3                                                                                                                      | 12   | 3          | 10.5 | ns   |
| t <sub>PHL</sub> | B̅ <sub>i</sub>                    |                  |                                                        | 3                                                                                                                      | 11   | 3          | 9.5  |      |
| t <sub>PLH</sub> | Any                                | Any F̅           | M = 0 V, S1 = S2 = 0 V,<br>S0 = S3 = 4.5 V (SUM mode)  | 3                                                                                                                      | 13.5 | 3          | 12   | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 3                                                                                                                      | 13   | 3          | 11.5 |      |
| t <sub>PLH</sub> | Any                                | Any F̅           | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 3                                                                                                                      | 16   | 3          | 14.5 | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 3                                                                                                                      | 13   | 3          | 12.5 |      |
| t <sub>PLH</sub> | A̅ <sub>i</sub> or B̅ <sub>i</sub> | F̅ <sub>i</sub>  | M = 4.5 V (LOGIC mode)                                 | 3                                                                                                                      | 12.5 | 3          | 11   | ns   |
| t <sub>PHL</sub> |                                    |                  |                                                        | 3                                                                                                                      | 10   | 3          | 9.5  |      |
| t <sub>PLH</sub> | Any                                | A = B            | M = 0 V, S0 = S3 = 0 V,<br>S1 = S2 = 4.5 V (DIFF mode) | 4                                                                                                                      | 19   | 4          | 17   | ns   |
| t <sub>PHL</sub> | A̅ or B̅                           |                  |                                                        | 5                                                                                                                      | 18.5 | 5          | 15   |      |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

ALS and AS Circuits

**SN54AS181B, SN74AS181B**  
**ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

**PARAMETER MEASUREMENT INFORMATION**

SUM MODE TEST TABLE  
 FUNCTION INPUTS:  $S_0 = S_3 = 4.5\text{ V}$ ,  $S_1 = S_2 = M = 0\text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS                 |                                           | OUTPUT UNDER TEST          | OUTPUT WAVEFORM (SEE NOTE 1) |
|-----------|------------------|----------------------|-------------|-----------------------------------|-------------------------------------------|----------------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                       | APPLY GND                                 |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $C_n$            | None                 | None        | All $\bar{A}$                     | All $\bar{B}$                             | Any $\bar{F}$ or $C_n + 4$ | In-Phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PHL}$ |                  |                      |             |                                   |                                           |                            |                              |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

# **SN54AS181B, SN74AS181B** **ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

## **PARAMETER MEASUREMENT INFORMATION**

DIFF MODE TEST TABLE  
 FUNCTION INPUTS:  $S_1 = S_2 = 4.5 \text{ V}$ ,  $S_0 = S_3 = M = 0 \text{ V}$

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS           |                                           | OUTPUT UNDER TEST          | OUTPUT WAVEFORM (SEE NOTE 1) |
|-----------|------------------|----------------------|-------------|-----------------------------|-------------------------------------------|----------------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                 | APPLY GND                                 |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | In-Phase                     |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $\bar{F}_i$                | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In-Phase                     |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | In-Phase                     |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{G}$                  | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$                    | In-Phase                     |
| $t_{PHL}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$                    | In-Phase                     |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$                    | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}$ , $C_n$               | $A = B$                    | Out-of-Phase                 |
| $t_{PLH}$ | $C_n$            | None                 | None        | All $\bar{A}$ and $\bar{B}$ | None                                      | $C_n + 4$ or any $\bar{F}$ | In-Phase                     |
| $t_{PHL}$ | $C_n$            | None                 | None        | All $\bar{A}$ and $\bar{B}$ | None                                      | $C_n + 4$ or any $\bar{F}$ | In-Phase                     |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PHL}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | Out-of-Phase                 |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | In-Phase                     |
| $t_{PHL}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ , $\bar{B}$ , $C_n$   | $C_n + 4$                  | In-Phase                     |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

ALS and AS Circuits

**SN54AS181B, SN74AS181B**  
**ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

**PARAMETER MEASUREMENT INFORMATION**

**LOGIC MODE TEST TABLE**

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

| PARAMETER        | INPUT UNDER TEST | OTHER INPUT SAME BIT |           | OTHER DATA INPUTS |                                           | OUTPUT UNDER TEST | OUTPUT WAVEFORM (SEE NOTE 1) |
|------------------|------------------|----------------------|-----------|-------------------|-------------------------------------------|-------------------|------------------------------|
|                  |                  | APPLY 4.5 V          | APPLY GND | APPLY 4.5 V       | APPLY GND                                 |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{F}_i$       | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |           |                   |                                           |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{F}_i$       | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |           |                   |                                           |                   |                              |

**INPUT BITS EQUAL/NOT EQUAL TEST TABLE**

FUNCTION INPUTS: S0 = S3 = M = 4.5 V, S1 = S2 = 0 V

| PARAMETER        | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS                         |           | OUTPUT UNDER TEST | OUTPUT WAVEFORM (SEE NOTE 1) |
|------------------|------------------|----------------------|-------------|-------------------------------------------|-----------|-------------------|------------------------------|
|                  |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                               | APPLY GND |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $\bar{P}$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $\bar{P}$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $\bar{P}$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $\bar{P}$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $C_n + 4$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $C_n + 4$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $C_n + 4$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | None      | $C_n + 4$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |             |                                           |           |                   |                              |

**INPUT PAIRS HIGH/NOT HIGH TEST TABLE**

FUNCTION INPUTS: S2 = M = 4.5 V, S0 = S1 = S3 = 0 V

| PARAMETER        | INPUT UNDER TEST | OTHER INPUT SAME BIT |           | OTHER DATA INPUTS           |                     | OUTPUT UNDER TEST | OUTPUT WAVEFORM (SEE NOTE 1) |
|------------------|------------------|----------------------|-----------|-----------------------------|---------------------|-------------------|------------------------------|
|                  |                  | APPLY 4.5 V          | APPLY GND | APPLY 4.5 V                 | APPLY GND           |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None      | Remaining $\bar{A}$ , $C_n$ | Remaining $\bar{B}$ | $\bar{P}$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |           |                             |                     |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None      | Remaining $\bar{B}$ , $C_n$ | Remaining $\bar{A}$ | $\bar{P}$         | In-Phase                     |
| t <sub>PHL</sub> |                  |                      |           |                             |                     |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None      | Remaining $\bar{A}$ , $C_n$ | Remaining $\bar{B}$ | $C_n + 4$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |           |                             |                     |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None      | Remaining $\bar{B}$ , $C_n$ | Remaining $\bar{A}$ | $C_n + 4$         | Out-of-Phase                 |
| t <sub>PHL</sub> |                  |                      |           |                             |                     |                   |                              |

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.