Am1508/1408 • SSS1508A/1408A

8-Bit Multiplying D/A Converter

Distinctive Characteristics

- Improved direct replacement for MC1508/1408
- ±0.19% nonlinearity guaranteed over temperature range
- Improved settling time (SSS1508A/1408A) 250ns, typ.
- Improved power consumption (SSS1508A/1408A) 157mW, typ.
- Compatible with TTL, CMOS logic
- Standard supply voltage: +5.0V and −5.0V to −15V
- Output voltage swing: +0.5V to −5.0V
- High speed multiplying input: 4.0mA/μs

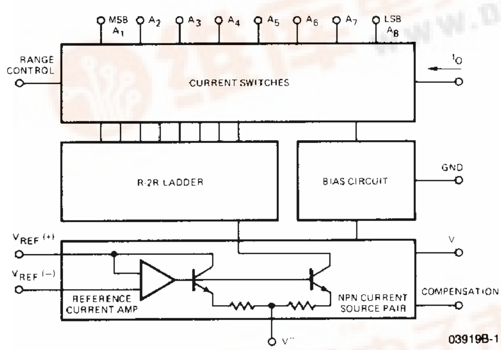
FUNCTIONAL DESCRIPTION

The SSS1508A/1408A, Am1508/1408 are 8-bit monolithic multiplying Digital-to-Analog Converters consisting of a reference current amplifier, an R-2R ladder, and eight high speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

The R-2R ladder divides the reference current into eight binarily-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full scale output current of 1.992mA would result from a reference input current of 2.0mA.

The SSS1508A/1408A, Am1508/1408 is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building Tracking and Successive Approximation Analog-to-Digital Converters.

BLOCK DIAGRAM



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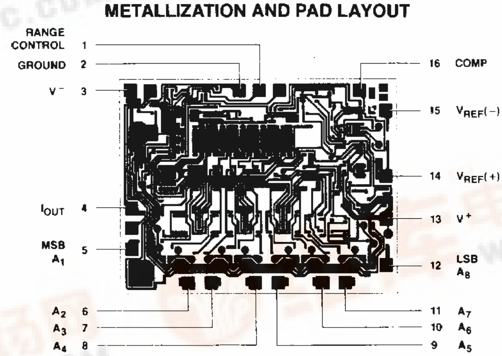
METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.068″ X 0.088″

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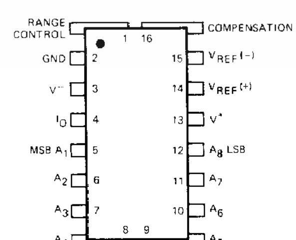
ORDERING INFORMATION*

Part Number	Package Type	Temperature Range	Order Number
Am1408	Hermetic DIP	0 to +70°C	AM1408L8
	Hermetic DIP	0 to +70°C	AM1408L7
	Hermetic DIP	0 to +70°C	AM1408L6
	Hermetic DIP	0 to +70°C	SSS1408A-8Q
	Hermetic DIP	0 to +70°C	SSS1408A-7Q
	Hermetic DIP	0 to +70°C	SSS1408A-6Q
	Plastic DIP	0 to +70°C	AM1408N8
	Plastic DIP	0 to +70°C	AM1408N7
	Plastic DIP	0 to +70°C	AM1408N6
	Dice	0 to +70°C	LD1408
Am1508	Hermetic DIP	−55 to +125°C	AM1508L8
	Hermetic DIP	−55 to +125°C	SSS1508A-8Q
	Dice	−55 to +125°C	LD1508

CONNECTION DIAGRAM
Top View

D-16-1
P-16-1



Am1508/1408 • SSS1508A/1408A

MAXIMUM RATINGS (Above which the useful life may be impaired)

(T_A = +25°C unless otherwise noted)

Power Supply Voltage	
V^+	+5.5Vdc
V^-	−16.5Vdc
Digital Input Voltage, V_5–V_{12}	+5.5, 0Vdc
Applied Output Voltage, V_O	+0.5, −5.2Vdc
Reference Current, I_{14}	5.0mA
Reference Amplifier Inputs, V_{14}, V_{15}	V_{CC}, V_{EE} Vdc

Power Dissipation (Package Limitation), P_D	
Ceramic Package	1000mW
Derate above T_A = +25°C	6.7mW/°C
Operating Temperature Range, T_A	
SSS1508A-8, Am1508	−55°C to +125°C
SSS1408A Series, Am1408 Series	0°C to +75°C
Storage Temperature, T_{stg}	−65°C to +150°C

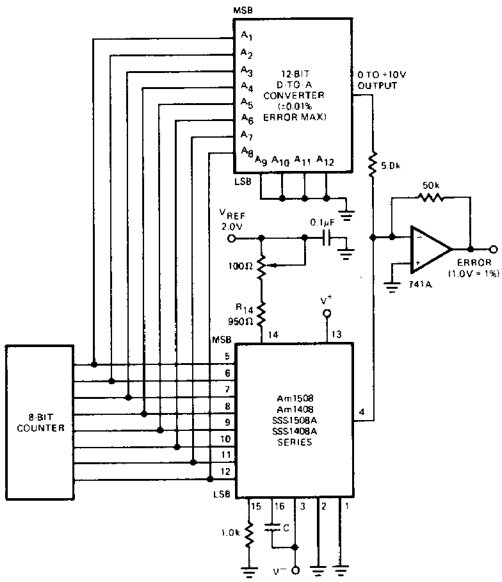
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

(V^+ = 5.0V, V^- = −15V, $\frac{V_{ref}}{R_{14}}$ = 2.0mA, SSS1508A-8/Am1508L8: T_A = −55 to +125°C, SSS1408A/Am1408 Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
E_R	**Relative Accuracy**					% IFS
	SSS1508A-8, SSS1408A-8, Am1508L8, Am1408L8				±0.19	
	SSS1408A-7, Am1408L7				±0.39	
	SSS1408A-6, Am1408L6				±0.78	
t_S	**Settling Time to within 1/2 LSB (includes t_{PLH})**					ns
	SSS1508A/1408A	T_A = +25°C		250		
	Am1508/1408			300		
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = +25°C		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		PPM/°C
	Digital Input Logic Levels (MSB)					
V_{IH}	High Level, Logic "1"		2.0			Vdc
V_{IL}	Low Level, Logic "0"				0.8	
I_{IH}	Digital Input Current (MSB)	High Level, V_{IH} = 5.0V		0	0.04	mA
I_{IL}		Low Level, V_{IL} = 0.8V		−0.002	−0.8	
I_{15}	**Reference Input Bias Current (Pin 15)**					μA
	SSS1508A/1408A			−1.0	−3.0	
	Am1508/1408			−1.0	−5.0	
ΔI_O	Output Current Range	V^- = −5.0V	0	2.0	2.1	mA
		V^- = −7.0V to −15V	0	2.0	4.2	
I_O	Output Current	V_{ref} = 2.000V, R_{14} = 1000Ω	1.9	1.99	2.1	mA
$I_{O\,(min.)}$	Output Current (All Bits Low)			0	4.0	μA
V_O	Output Voltage Compliance	V^- = −5V			−0.6, +0.5	Vdc
	(E_r ≤ 0.19% at T_A = +25°C)	V^- below −10V			−5.0, +0.5	
SRI_{ref}	Reference Current Slew Rate			4.0		mA/μs
$PSSI_O$	Output Current Power Supply Sensitivity			0.5	2.7	μA/V
	Power Supply Current					mA
I^+	SSS1508A/1408A			2.5	14	
I^-				−6.4	−13	
I^+	Am1508/1408			2.5	22	
I^-				−6.4	−13	
ΔV^+	Power Supply Voltage Range	T_A = +25°C	4.5	5.0	5.5	Vdc
ΔV^-			−4.5	−15	−16.5	
P_d	**Power Dissipation**	All Bits Low				mW
	SSS1508A/1408A	V^- = −5.0Vdc		34	136	
		V^- = −15Vdc		108	265	
		All Bits High				
		V^- = −5.0Vdc		34		
		V^- = −15Vdc		108		
	Am1508/1408	All Bits Low				
		V^- = −5.0Vdc		34	170	
		V^- = −15Vdc		108	305	

TYPICAL APPLICATIONS

RELATIVE ACCURACY TEST CIRCUIT



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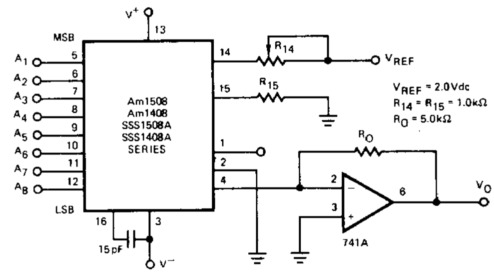
USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R_{14}}(R_O)\left[\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{126}+\frac{A_8}{256}\right]$$

ADJUST V_{REF}, R_{14} OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS

$$V_O = \frac{2V}{1k}(5k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{126}+\frac{1}{256}\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

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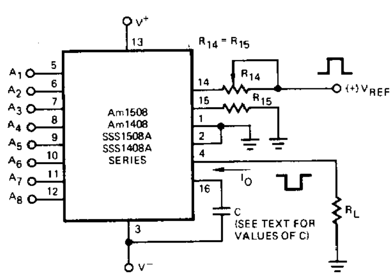
USE WITH POSITIVE V_{REF}



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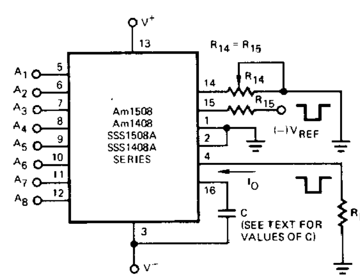
USE WITH NEGATIVE V_{REF}



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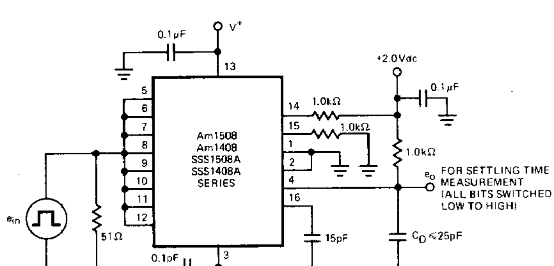
TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive voltage are shown on the previous page. The reference voltage source supplies the full current I_{14}. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0 kilohms, minumum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V^- or ground, but using V^- increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V^- on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0 volts above the V^- supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of −0.6 to +0.5 volts when $V^- = -5.0V$ due to the current switching methods employed in the SSS1508A-8, Am1508.

The negative output voltage compliance of the SSS1508A-8, Am1508 is extended to −5.0V where the negative supply voltage is more negative than −10 volts. Using a full scale current of 1.992mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and −4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance but a 2.5-kilohm load increases "worst case" settling time to 1.2μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than −12.0 volts,

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the SSS1508A-8, Am1508 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the SSS1508A-8 has a very low full scale current drift with temperature.

The SSS1508A-8/Am1508 Series is guaranteed accurate to within ±1/2 LSB at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0μA) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown on page 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the SSS1508A-8, Am1508 accuracy is essentially the same between 1.5 and 2.5mA. Then the SSS1508A-8, Am1508 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65,536 or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the SSS1508A-8, Am1508.

MULTIPLYING ACCURACY

The SSS1508A-8, Am1508 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16μA to 4.0mA, the additional error contributions are less than 1.6μA. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the SSS1508A-8, Am1508 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25pF$.

The slowest single switch is the least significant bit. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring