SBAS326C–JUNE 2004–REVISED DECEMBER 2004

4-Channel, 12-Bit, 40MSPS ADC with Serial LVDS Interface

FEATURES

- **Maximum Sample Rate: 40MSPS**
- **12-Bit Resolution**
- **No Missing Codes**
- **Power Dissipation: 607mW**
- **CMOS Technology**
- **Simultaneous Sample-and-Hold**
- **70.5dBFS SNR at 10MHz IF**
- **Internal and External References**
- **3.3V Digital/Analog Supply**
- **Serialized LVDS Outputs**
- **Integrated Frame and Bit Patterns**
- **MSB and LSB First Modes**
- **Option to Double LVDS Clock Output Currents**
- **Pin- and Format-Compatible Family**
- **HTQFP-64 PowerPAD™ Package**

APPLICATIONS

- **Portable Ultrasound Systems**
- **Tape Drives**
- **Test Equipment**
- **Optical Networking**

DESCRIPTION

The ADS5240 is a high-performance, 4-channel, 40MSPS analog-to-digital converter (ADC). Internal references are provided, simplifying system design requirements. Low power consumption allows for the highest of system integration densities. Serial LVDS (low-voltage differential signaling) outputs reduce the number of interface lines and package size.

RELATED PRODUCTS

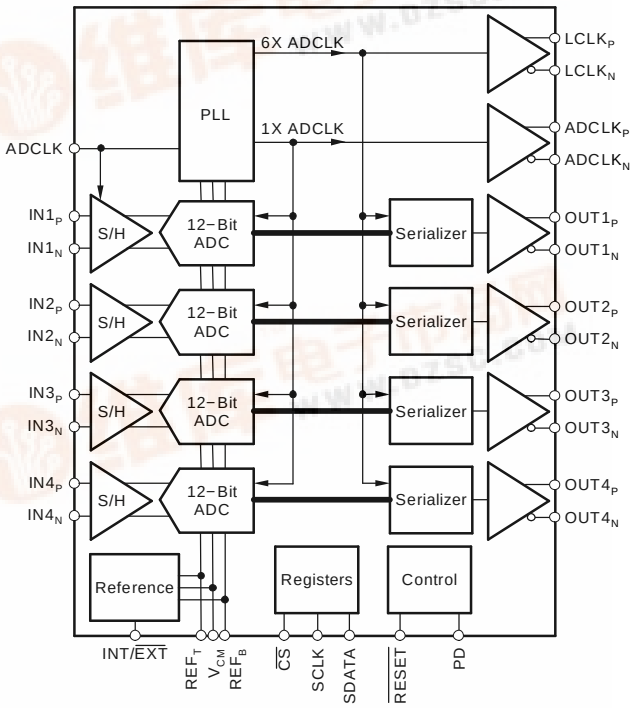
MODEL	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CHANNELS
ADS5242(1)	12	65	4

(1) Available Q1 2005.

An integrated phase lock loop multiplies the incoming ADC sampling clock by a factor of 12. This 12x clock is used in the process of serializing the data output from each channel. The 12x clock is also used to generate a 1x and a 6x clock, both of which are transmitted as LVDS clock outputs. The 6x clock is denoted by the differential pair $LCLK_P$ and $LCLK_N$, while the 1x clock is denoted by $ADCLK_P$ and $ADCLK_N$. The word output of each ADC channel can be transmitted either as MSB or LSB first. The bit coinciding with the rising edge of the 1x clock output is the first bit of the word. Data is to be latched by the receiver on both the rising and falling edges of the 6x clock.

The ADS5240 provides internal references, or can optionally be driven with external references. Best performance can be achieved through the internal reference mode.

The device is available in an HTQFP-64 PowerPAD package and is specified over a -40°C to +85°C operating range.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5240	HTQFP-64(2)	PAP	-40°C to +85°C	ADS5240I	ADS5240IPAP	Tray, 160
					ADS5240IPAPT	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 5.29mm × 5.29mm (min), 6.50mm × 6.50mm (max).

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage Range, AVDD	-0.3V to +3.8V
Supply Voltage Range, LVDD	-0.3V to +3.8V
Voltage Between AVSS and LVSS	-0.3V to +0.3V
Voltage Between AVDD and LVDD	-0.3V to +0.3V
Voltage Applied to External REF Pins	-0.3V to +2.4V
All LVDS Data and Clock Outputs	-0.3V to +2.4V
Analog Input Pins	-0.15V to +3.0V
Peak Total Input Current (all inputs)	30mA
Junction Temperature	+105°C
Operating Free-Air Temperature Range, T_A	-40°C to +85°C
Lead Temperature, 1.6mm (1/16" from case for 10s)	220°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

RECOMMENDED OPERATING CONDITIONS

	ADS5240			
	MIN	TYP	MAX	UNITS
SUPPLIES AND REFERENCES				
Analog Supply Voltage, AVDD	3.0	3.3	3.6	V
Output Driver Supply Voltage, LVDD	3.0	3.3	3.6	V
CLOCK INPUT AND OUTPUTS				
ADCLK Input Sample Rate (low-voltage TTL)	20		40	MSPS
Low-Level Voltage Clock Input			0.6	V
High-Level Voltage Clock Input	2.2			V
$ADCLK_P$ and $ADCLK_N$ Outputs (LVDS)	20		40	MHz
$LCLK_P$ and $LCLK_N$ Outputs (LVDS)(1)	120		240	MHz
Operating Free-Air Temperature, T_A	-40		+85	°C
Thermal Characteristics:				
θ_{JA}		24		°C/W
θ_{JC}		15		°C/W

(1) 6 × ADCLK.

REFERENCE SELECTION

MODE	INT/$\overline{EXT}$	DESCRIPTION
Internal Reference	1	Full-scale range = $2.0V_{PP}$. Default with internal pull-up.
External Reference	0	Internal reference is powered down. Common mode of external reference should be within 50mV of V_{CM}. V_{CM} is derived from the internal bandgap voltage.

ELECTRICAL CHARACTERISTICS

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = 40MSPS, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V differential, transformer coupled inputs, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LDVS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS5240 MIN	ADS5240 TYP	ADS5240 MAX	UNITS
DC ACCURACY						
	No Missing Codes			Assured		
DNL	Differential Nonlinearity	f_{IN} = 5MHz	-0.9	±0.4	+0.9	LSB
INL	Integral Nonlinearity	f_{IN} = 5MHz	-2.0	±0.75	+2.0	LSB
	Offset Error(1)		-0.75	±0.2	+0.75	%FS
	Offset Temperature Coefficient			14		ppm/°C
	Fixed Attenuation in Channel(2)			1		%FS
	Variable Attenuation in Channel(3)			±0.2		%FS
	Gain Error(4)	REF_T - REF_B	-5	±1.0	+5	%FS
	Attenuation Temperature Coefficient(5)			44		ppm/°C
POWER SUPPLY						
I_{CC}	Total Supply Current	V_{IN} = FS, F_{IN} = 5MHz		184		mA
I(AVDD)	Analog Supply Current	V_{IN} = FS, F_{IN} = 5MHz		142		mA
I(LVDD)	Digital Output Driver Supply Current	V_{IN} = FS, F_{IN} = 5MHz, LVDS into 100Ω Load		42		mA
	Power Dissipation			607	650	mW
	Power-Down	Clock Running		95		mW
REFERENCE VOLTAGES						
$VREF_T$	Reference Top (internal)		1.95	2.0	2.05	V
$VREF_B$	Reference Bottom (internal)		0.95	1.0	1.05	V
V_{CM}	Common-Mode Voltage		1.45	1.5	1.55	V
	V_{CM} Output Current(6)	±50mV Change in Voltage		±2		mA
$VREF_T$	Reference Top (external)		1.875			V
$VREF_B$	Reference Bottom (external)				1.125	V
	External Reference Input Current(7)			1.0		mA
ANALOG INPUT						
	Differential Input Capacitance			4.0		pF
	Analog Input Common-Mode Range			V_{CM} ± 0.05		V
	Differential Input Voltage Range		1.5		2.02	V_{PP}
	Voltage Overhead Recovery Time	Differential Input Signal at 4V_{PP} Recovery to Within 1% of Code		4.0		CLK Cycles
	Input Bandwidth	-3dBFS		300		MHz
DIGITAL DATA OUTPUTS						
	Data Bit Rate		240		480	MBPS

(1) Offset error is the deviation of the average code from mid-code for a zero input. Offset error is expressed in terms of % of full-scale.
(2) Fixed attenuation in the channel arises due to a fixed attenuation of about 1% in the sample-and-hold amplifier. When the differential voltage at the analog input pins are changed from -V_{REF} to +V_{REF}, the swing of the output code is expected to deviate from the full-scale code (4096LSB) by the extent of this fixed attenuation.
NOTE: V_{REF} is defined as (REF_T - REF_B).
(3) Variable attenuation in the channel refers to the attenuation of the signal in the channel over and above the fixed attenuation.
(4) The reference voltages are trimmed at production so that ($VREF_T$ - $VREF_B$) is within ± 50mV of the ideal value of 1V. It does not include fixed attenuation.
(5) The attenuation temperature coefficient refers to the temperature coefficient of the attenuation in the channel. It does not account for the variation of the reference voltages with temperature.
(6) V_{CM} provides the common-mode current for the inputs of all four channels when the inputs are AC-coupled. The V_{CM} output current specified is the additional drive of the V_{CM} buffer if loaded externally.
(7) Average current drawn from the reference pins in the external reference mode.

AC CHARACTERISTICS

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = 40MSPS, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V differential, transformer coupled inputs, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER	CONDITIONS	ADS5240			UNITS
		MIN	TYP	MAX	
DYNAMIC CHARACTERISTICS					
SFDR Spurious-Free Dynamic Range	f_{IN} = 1MHz		87		dBc
	f_{IN} = 5MHz	78	85		dBc
	f_{IN} = 10MHz		85		dBc
HD_2 2nd-Order Harmonic Distortion	f_{IN} = 1MHz		95		dBc
	f_{IN} = 5MHz	85	95		dBc
	f_{IN} = 10MHz		90		dBc
HD_3 3rd-Order Harmonic Distortion	f_{IN} = 1MHz		87		dBc
	f_{IN} = 5MHz	78	85		dBc
	f_{IN} = 10MHz		85		dBc
SNR Signal-to-Noise Ratio	f_{IN} = 1MHz		70.5		dBFS
	f_{IN} = 5MHz	68	70.5		dBFS
	f_{IN} = 10MHz		70		dBFS
SINAD Signal-to-Noise and Distortion	f_{IN} = 1MHz		70		dBFS
	f_{IN} = 5MHz	67	70		dBFS
	f_{IN} = 10MHz		69.5		dBFS
IMD Two-Tone Intermodulation Distortion	f_1 = 9.5MHz at -7dBFS f_2 = 10.2MHz at -7dBFS		-88		dBc
ENOB Effective Number of Bits	f_{IN} = 5MHz		11.3		Bits
Crosstalk	Signal Applied to 3 Channels; Measurement Taken on the Channel with No Input Signal		-90		dBc

LVDS DIGITAL DATA AND CLOCK OUTPUTS

Test conditions at I_O = 3.5mA, R_{LOAD} = 100Ω, and C_{LOAD} = 6pF. I_O refers to the current setting for the LVDS buffer. R_{LOAD} is the differential load resistance between the LVDS pair. C_{LOAD} is the effective single-ended load capacitance between each of the LVDS pins and ground. C_{LOAD} includes the receiver input parasitics as well as the routing parasitics. Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. All LVDS specifications are characterized, but not tested at production.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS (1)						
V_{OH}	Output Voltage High, OUT_P or OUT_N	R_{LOAD} = 100Ω± 1% See LVDS Timing Diagram, Page 7		1375	1500	mV
V_{OL}	Output Voltage Low, OUT_P or OUT_N	R_{LOAD} = 100Ω± 1%	900	1025		mV
$\|V_{OD}\|$	Output Differential Voltage, $\|OUT_P - OUT_N\|$	R_{LOAD} = 100Ω± 1%	300	350	400	mV
V_{OS}	Output Offset Voltage (2)	R_{LOAD} = 100Ω± 1% See LVDS Timing Diagram, Page 7	1100	1200	1300	mV
C_O	Output Capacitance (3)	V_{CM} = 1.5V		4		pF
$\|\Delta V_{OD}\|$	Change in $\|V_{OD}\|$ Between 0 and 1	R_{LOAD} = 100Ω± 1%			25	mV
ΔV_{OS}	Change Between 0 and 1	R_{LOAD} = 100Ω± 1%			25	mV
ISOUT	Output Short-Circuit Current	Drivers Shorted to Ground			40	mA
$ISOUT_{NP}$	Output Current	Drivers Shorted Together			12	mA
DRIVER AC SPECIFICATIONS						
Clock	LVDS Clock Duty Cycle	6 × ADCLK ($LCLK_P$, $LCLK_N$)	45	50	55	%
	Minimum Data Setup Time (4) (5)			650		ps
	Minimum Data Hold Time (4) (5)			650		ps
t_{RISE}/t_{FALL}	V_{OD} Rise Time or V_{OD} Fall Time	I_O = 2.5mA		400		ps
		I_O = 3.5mA		250		ps
		I_O = 4.5mA		200		ps
		I_O = 6mA		150		ps

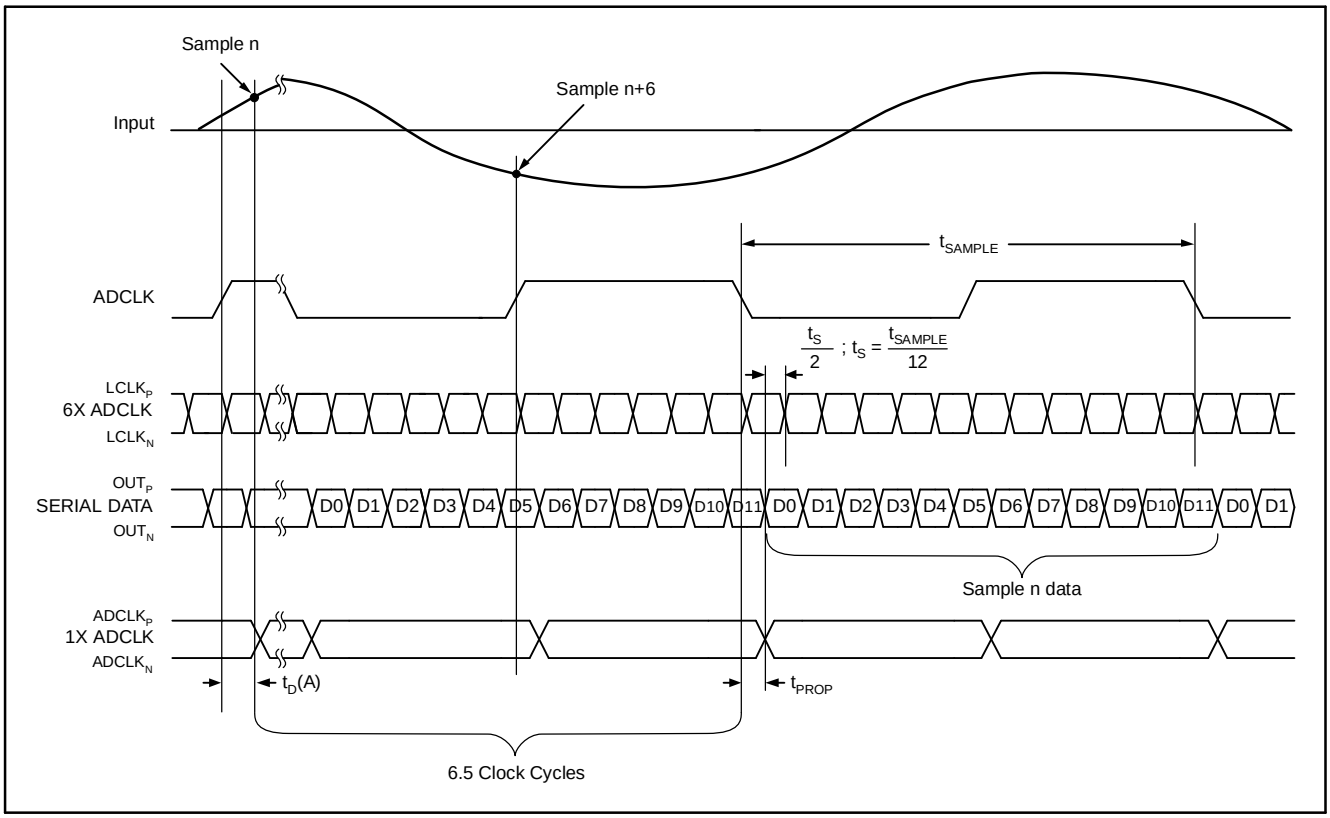
(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1.
(2) V_{OS} refers to the common-mode of OUT_P and OUT_N.
(3) Output capacitance inside the device, from either OUT_P or OUT_N to ground.
(4) Refer to the LVDS application note (SBAA118) for a description of data setup and hold times.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins.

SWITCHING CHARACTERISTICS

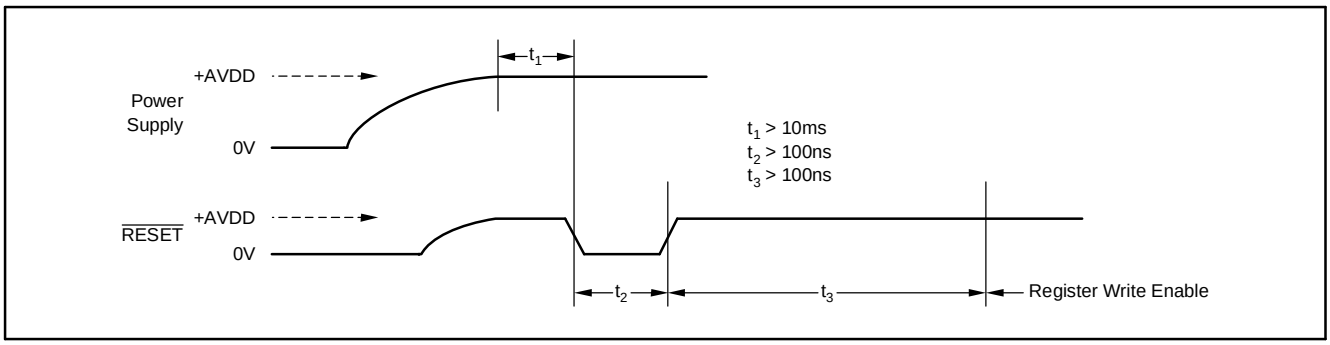
T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = 40MSPS, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER		CONDITIONS	ADS5240			UNITS
			MIN	TYP	MAX	
SWITCHING SPECIFICATIONS						
	t_{SAMPLE}		25		50	ns
t_D(A)	Aperture Delay			3.1		ns
	Aperture Jitter (uncertainty)			1		ps rms
t_D(pipeline)	Latency			6.5		Cycles
t_{PROP}	Propagation Delay			5		ns

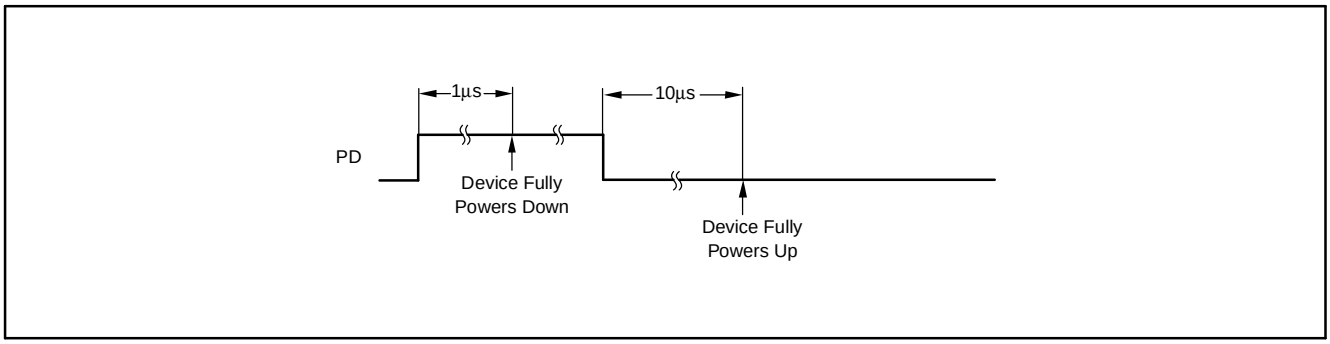
LVDS TIMING DIAGRAM (PER ADC CHANNEL)



RESET TIMING



POWER-DOWN TIMING



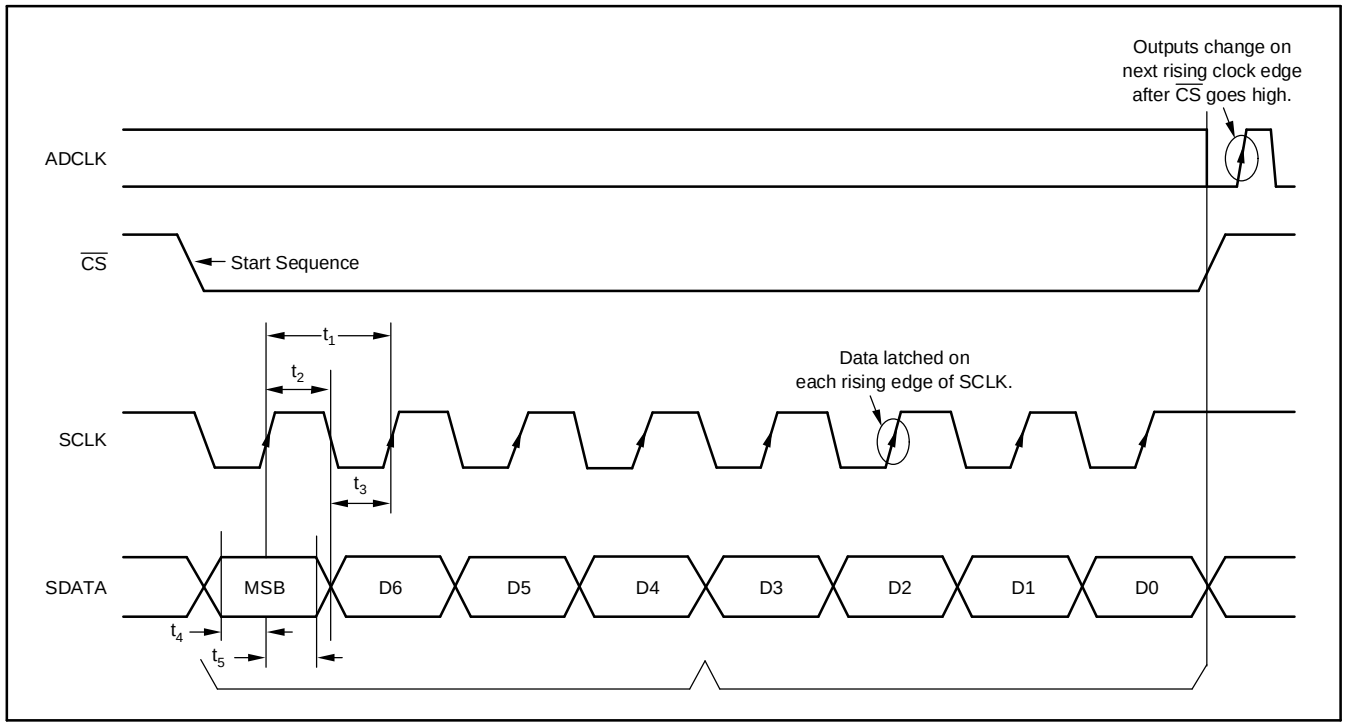
SERIAL INTERFACE

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS5240			UNITS
		MIN	TYP	MAX	
SCLK Serial Clock Input Frequency				20	MHz
V_{IN} LOW Input Low Voltage		0		0.6	V
V_{IN} HIGH Input High Voltage		2.2		AVDD	V
Input Current			±10		µA
Input Pin Capacitance			5.0		pF

SERIAL INTERFACE TIMING

Data is shifted in MSB first.



PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Serial CLK Period	50			ns
t_2	Serial CLK High Time		25		ns
t_3	Serial CLK Low Time		25		ns
t_4	Minimum Data Setup Time		5		ns
t_5	Minimum Data Hold Time		5		ns

SERIAL INTERFACE REGISTERS

ADDRESS				DATA				DESCRIPTION	REMARKS
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0					**LVDS BUFFERS (register 0)**	
				0	0			Normal ADC Output	(default after reset)
				0	1			Deskew Pattern	
				1	0			Sync Pattern	Patterns Get Reversed in MSB First Mode of LVDS
				1	1			Custom Pattern	
						0	0	Output Current in LVDS = 3.5mA	(default after reset)
						0	1	Output Current in LVDS = 2.5mA	
						1	0	Output Current in LVDS = 4.5mA	
						1	1	Output Current in LVDS = 6.0mA	
0	0	0	1					**LSB/MSB MODE (register 1)**	
				0	X	X	0	Default LVDS Clock Output Current	I_{OUT} = 3.5mA
				0	X	X	1	2X LVDS Clock Output Current	I_{OUT} = 7.0mA
				0	0	X	X	LSB First Mode	(default after reset)
				0	1	X	X	MSB First Mode	
0	0	1	0					**POWER-DOWN ADC CHANNELS (register 2)**	
				0	1	0	X	D2: Power-Down for Channel 2	Logic 1 = Channel Powered Down
				0	X	0	1	D0: Power-Down for Channel 1	
0	0	1	1					**POWER-DOWN ADC CHANNELS (register 3)**	
				1	0	X	0	D3: Power-Down for Channel 4	Logic 1 = Channel Powered Down
				X	0	1	0	D1: Power-Down for Channel 3	
								CUSTOM PATTERN (registers 4-6)	
				D3	**D2**	**D1**	**D0**	Bits for Custom Pattern	See *Test Patterns*
0	1	0	0	X	X	X	X		
0	1	0	1	X	X	X	X		
0	1	1	0	X	X	X	X		

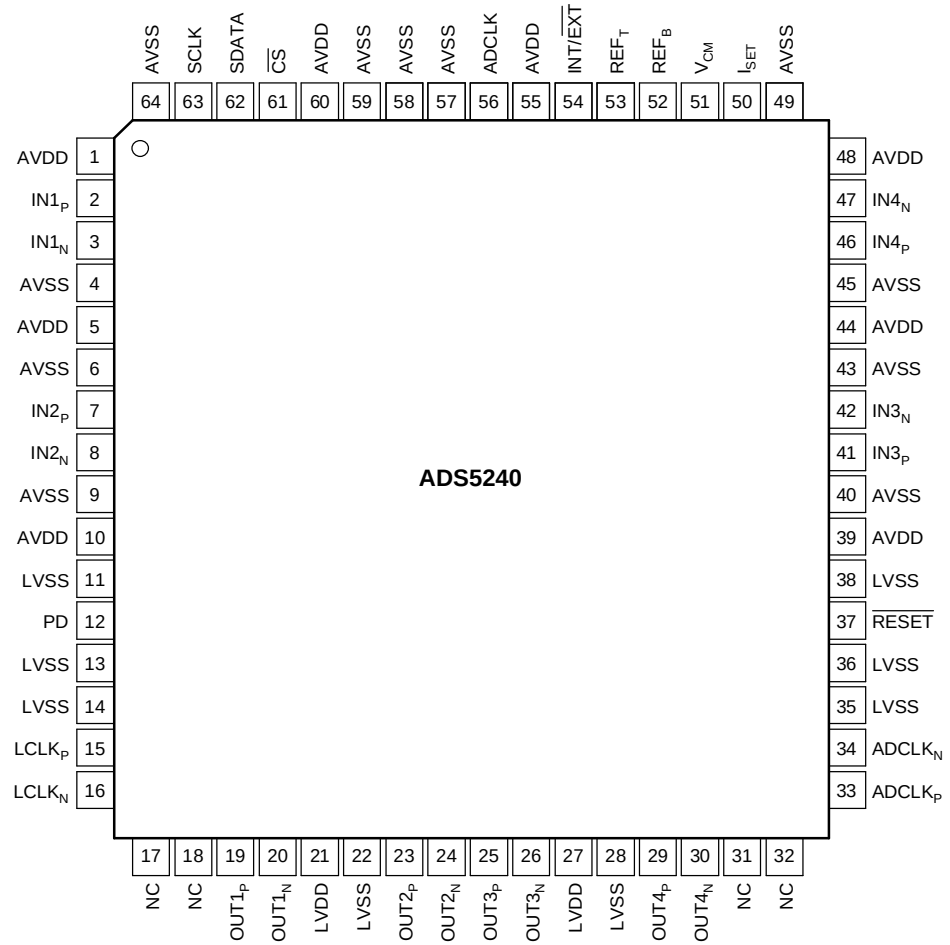
TEST PATTERNS(1)

Deskew	101010101010
Sync	000000111111
Custom	Any 12-bit pattern that is defined in the custom pattern registers 4 to 6. The output comes out in the following order: D0(4) D1(4) D2(4) D3(4) D0(5) D1(5) D2(5) D3(5) D0(6) D1(6) D2(6) D3(6) where, for example, D0(4) refers to the D0 bit of register 4, etc.

(1) Default is LSB first. If MSB first is selected, the above patterns will be reversed.

PIN CONFIGURATION

Top View **HTQFP**



PIN DESCRIPTIONS

NAME	PIN #	I/O	DESCRIPTION
AVDD	1, 5, 10, 39, 44, 48, 55, 60	I	Analog Power Supply
$IN1_P$	2	I	Channel 1 Differential Analog Input High
$IN1_N$	3	I	Channel 1 Differential Analog Input Low
AVSS	4, 6, 9, 40, 43, 45, 49, 57-59, 64	I	Analog Ground
$IN2_P$	7	I	Channel 2 Differential Analog Input High
$IN2_N$	8	I	Channel 2 Differential Analog Input Low
LVSS	11, 13, 14, 22, 28, 35, 36, 38	I	LVDS Ground
PD	12	I	Power-Down; 0 = Normal, 1 = Power-Down
$LCLK_P$	15	O	Positive LVDS Clock
$LCLK_N$	16	O	Negative LVDS Clock
NC	17, 18, 31, 32	—	No Connection
$OUT1_P$	19	O	Channel 1 Positive LVDS Data Output
$OUT1_N$	20	O	Channel 1 Negative LVDS Data Output
LVDD	21, 27	I	LVDS Power Supply
$OUT2_P$	23	O	Channel 2 Positive LVDS Data Output
$OUT2_N$	24	O	Channel 2 Negative LVDS Data Output
$OUT3_P$	25	O	Channel 3 Positive LVDS Data Output
$OUT3_N$	26	O	Channel 3 Negative LVDS Data Output
$OUT4_P$	29	O	Channel 4 Positive LVDS Data Output
$OUT4_N$	30	O	Channel 4 Negative LVDS Data Output
$ADCLK_P$	33	O	Positive LVDS ADC Clock Output
$ADCLK_N$	34	O	Negative LVDS ADC Clock Output
$\overline{RESET}$	37	I	Reset Registers to Default; 0 = Reset, 1 = Normal
$IN3_P$	41	I	Channel 3 Differential Analog Input High
$IN3_N$	42	I	Channel 3 Differential Analog Input Low
$IN4_P$	46	I	Channel 4 Differential Analog Input High
$IN4_N$	47	I	Channel 4 Differential Analog Input Low
I_{SET}	50	I/O	Bias Current Setting Resistor of 56.2kΩ to Ground
V_{CM}	51	O	Common-Mode Output Voltage
REF_B	52	I/O	Reference Bottom Voltage (2Ω resistor in series with 0.1µF capacitor to ground)
REF_T	53	I/O	Reference Top Voltage (2Ω resistor in series with 0.1µF capacitor to ground)
INT/$\overline{EXT}$	54	I	Internal/External Reference Select; 0 = External, 1 = Internal
ADCLK	56	I	Data Converter Clock Input
$\overline{CS}$	61	I	Chip-Select; 0 = Select, 1 = No Select
SDATA	62	I	Serial Data Input
SCLK	63	I	Serial Data Clock

DEFINITION OF SPECIFICATIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3dB.

Aperture Delay

The delay in time between one of the edges of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic '1' state to achieve rated performance. Pulse width low is the minimum time that the ENCODE pulse should be left in a low state (logic '0'). At a given clock rate, these specifications define an acceptable clock duty cycle.

Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation of any single LSB transition at the digital output from an ideal 1 LSB step at the analog input. If a device claims to have no missing codes, it means that all possible codes (for a 12-bit converter, 4096 codes) are present over the full operating range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

If SINAD is not known, SNR can be used exceptionally to calculate ENOB ($ENOB_{SNR}$).

Integral Nonlinearity (INL)

INL is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a *best straight line* or *best fit* determined by a least square curve fit. INL is independent from effects of offset, gain or quantization errors.

Maximum Conversion Rate

The encode rate at which parametric testing is performed. This is the maximum sampling rate where certified operation is given.

Minimum Conversion Rate

This is the minimum sampling rate where the ADC still works.

Nyquist Sampling

When the sampled frequencies of the analog input signal are below $f_{CLOCK/2}$, it is called Nyquist sampling. The Nyquist frequency is $f_{CLOCK/2}$, which can vary depending on the sample rate (f_{CLOCK}).

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Propagation Delay

This is the delay between the input clock of one of the edges and the time when all data bits are within valid logic levels.

Signal-to-Noise and Distortion (SINAD)

The RMS value of the sine wave f_{IN} (input sine wave for an ADC) to the RMS value of the noise of the converter from DC to the Nyquist frequency, including harmonic content. It is typically expressed in decibels (dB). SINAD includes harmonics, but excludes DC.

$$\text{SINAD} = 20\text{Log}_{(10)}\frac{\text{Input}(V_S)}{\text{Noise} + \text{Harmonics}}$$

Signal-to-Noise Ratio (without harmonics)

SNR is a measure of signal strength relative to background noise. The ratio is usually measured in dB. If the incoming signal strength in µV is V_S and the noise level (also in µV) is V_N, then the SNR in dB is given by the formula:

$$SNR = 20Log_{(10)}\frac{V_S}{V_N}$$

This is the ratio of the RMS signal amplitude, V_S (set 1dB below full-scale), to the RMS value of the sum of all other spectral components, V_N, excluding harmonics and DC.

Spurious-Free Dynamic Range (SFDR)

The ratio of the RMS value of the analog input sine wave to the RMS value of the peak spur observed in the frequency domain. It may be reported in dBc (that is, it degrades as signal levels are lowered), or in dBFS (always related back to converter full-scale). The peak spurious component may or may not be a harmonic.

Temperature Drift

Temperature drift (for offset error and gain error) specifies the maximum change from the initial temperature value to the value at T_{MIN} or T_{MAX}.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS signal amplitude of the input sine wave to the RMS value of distortion appearing at multiples (harmonics) of the input, typically given in dBc.

Two-Tone Intermodulation Distortion Rejection

The ratio of the RMS value of either input tone (f_1, f_2) to the RMS value of the worst third-order intermodulation product ($2f_1 - f_2$; $2f_2 - f_1$). It is reported in dBc.

TYPICAL CHARACTERISTICS

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

SPECTRAL PERFORMANCE

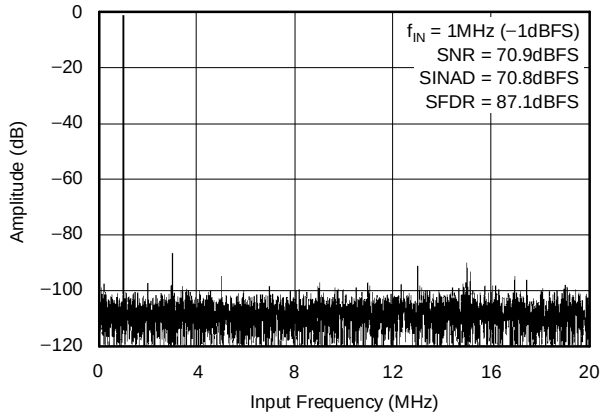


Figure 1.

SPECTRAL PERFORMANCE

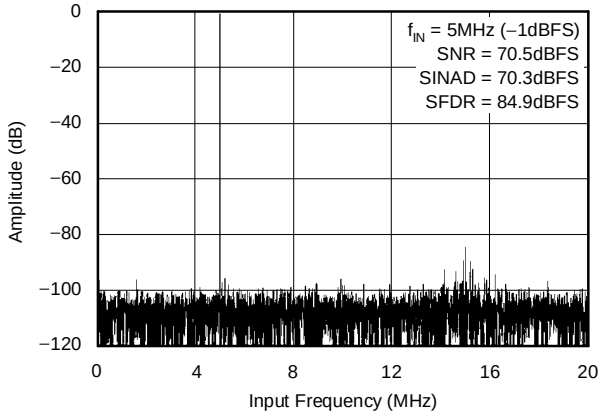


Figure 2.

SPECTRAL PERFORMANCE

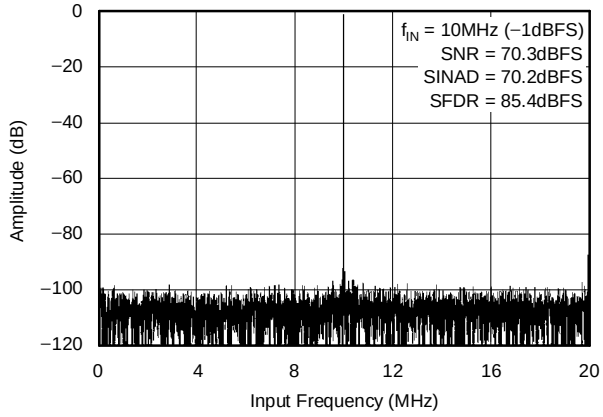


Figure 3.

TWO-TONE INTERMODULATION

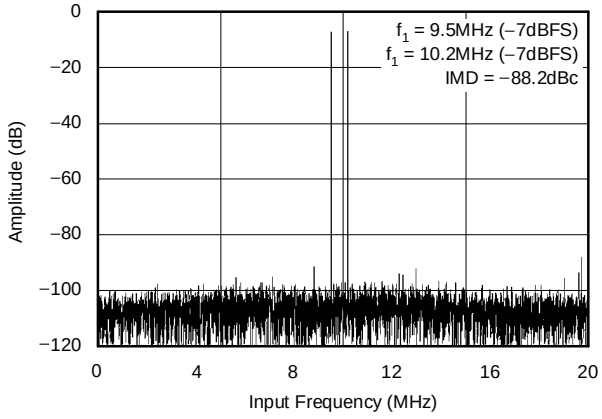


Figure 4.

DIFFERENTIAL NONLINEARITY ERROR

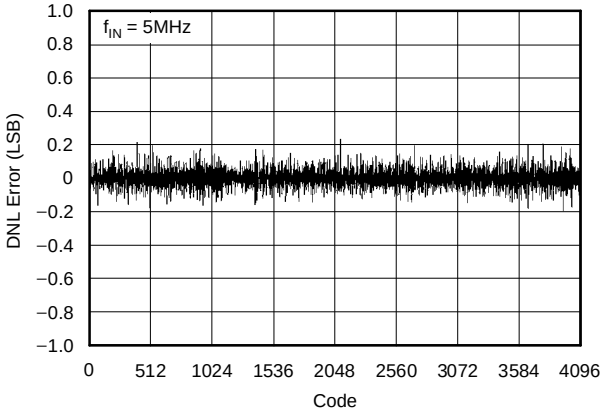


Figure 5.

INTEGRAL NONLINEARITY ERROR

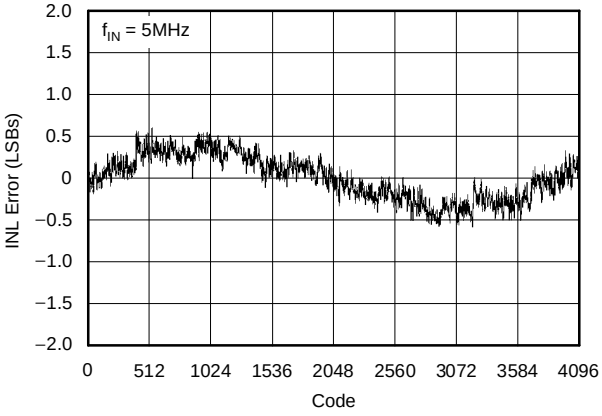


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

SWEPT INPUT POWER

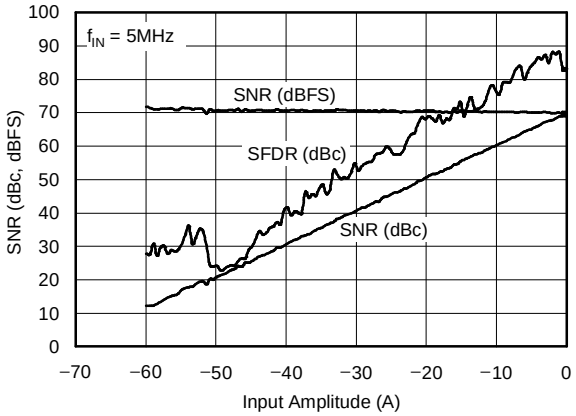


Figure 7.

SWEPT INPUT POWER

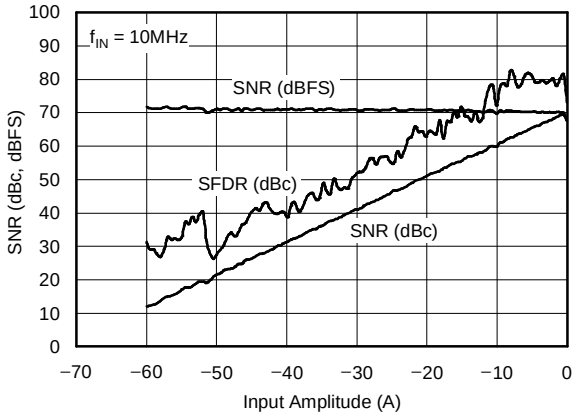


Figure 8.

IAVDD, IDVDD vs SAMPLE RATE

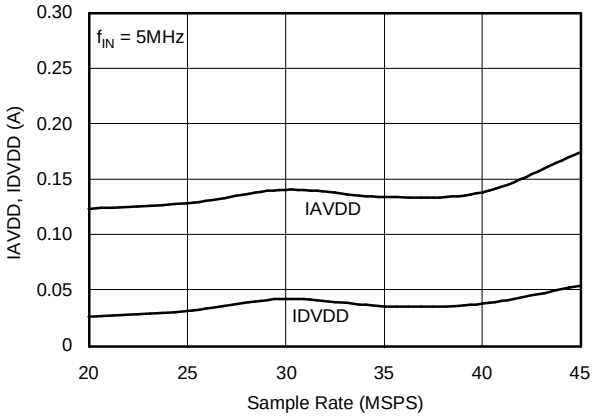


Figure 9.

DYNAMIC PERFORMANCE vs SAMPLE RATE

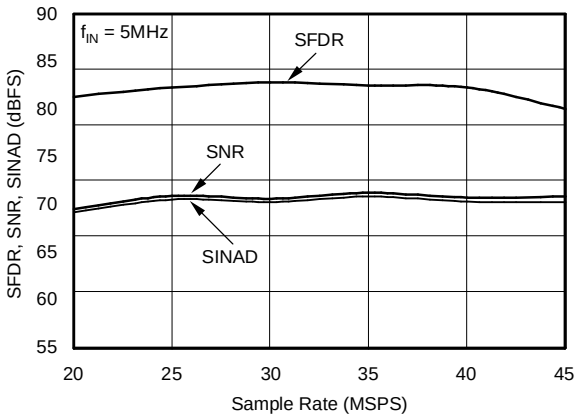


Figure 10.

DYNAMIC PERFORMANCE vs SAMPLE RATE

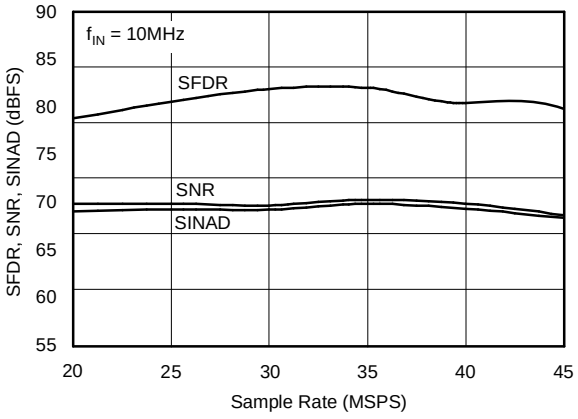


Figure 11.

POWER DISSIPATION vs TEMPERATURE

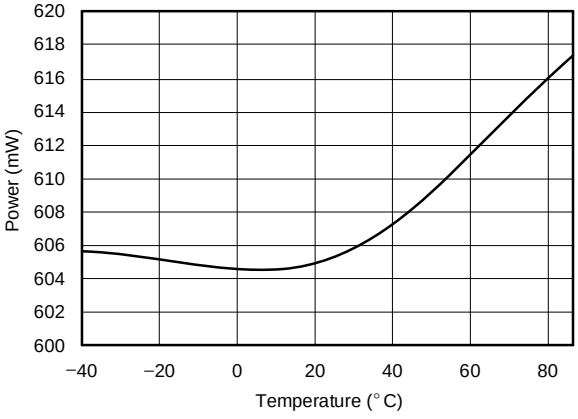


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_{MIN} = -40°C and T_{MAX} = +85°C. Typical values are at T_A = 25°C, clock frequency = maximum specified, 50% clock duty cycle, AVDD = 3.3V, LVDD = 3.3V, -1dBFS, I_{SET} = 56.2kΩ, internal voltage reference, and LVDS buffer current at 3.5mA per channel, unless otherwise noted.

OUTPUT NOISE HISTOGRAM

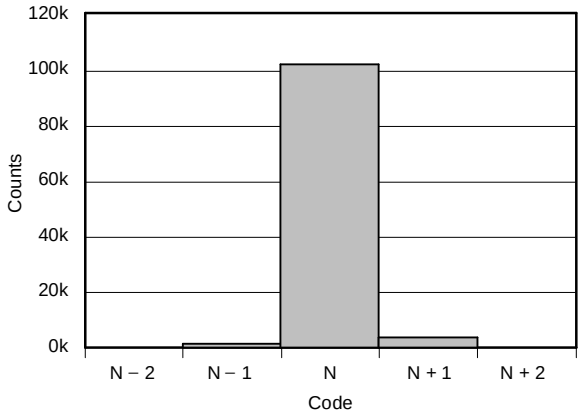


Figure 13.

THEORY OF OPERATION

OVERVIEW

The ADS5240 is a 4-channel, high-speed, CMOS ADC. It consists of a high-performance sample-and-hold circuit at the input, followed by a 12-bit ADC. The 12 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All four channels of the ADS5240 operate from a single clock referred to as ADCLK. The sampling clocks for each of the four channels are generated from the input clock using a carefully matched clock buffer tree. The 12x clock required for the serializer is generated internally from ADCLK using a phase lock loop (PLL). A 6x and a 1x clock are also output in LVDS format along with the data to enable easy data capture. The ADS5240 operates from internally-generated reference voltages that are trimmed to improve matching across multiple devices on a board. This feature eliminates the need for external routing of reference lines and also improves matching of the gain across devices. The nominal values of REF_T and REF_B are 2V and 1V, respectively. These values imply that a differential input of -1V corresponds to the zero code of the ADC, and a differential input of +1V corresponds to the full-scale code (4095 LSB). V_{CM} (common-mode voltage of REF_T and REF_B) is also made available externally through a pin, and is nominally 1.5V.

The ADC employs a pipelined converter architecture consisting of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level. The pipeline architecture results in a data latency of 6.5 clock cycles.

The output of the ADC goes to a serializer that operates from a 12x clock generated by the PLL. The 12 data bits from each channel are serialized and sent LSB first. In addition to serializing the data, the serializer also generates a 1x clock and a 6x clock. These clocks are generated in the same way the serialized data is generated, so these clocks maintain perfect synchronization with the data. The data and clock outputs of the serializer are buffered externally using LVDS buffers. Using LVDS buffers to transmit data externally has multiple advantages, such as reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the ADS5240.

The ADS5240 operates from two sets of supplies and grounds. The analog supply/ground set is denoted as AVDD/AVSS, while the digital set is denoted by LVDD/LVSS.

DRIVING THE ANALOG INPUTS

The analog input biasing is shown in Figure 14. The recommended method to drive the inputs is through AC coupling. AC coupling removes the worry of setting the common-mode of the driving circuit, since the inputs are biased internally using two 600Ω resistors.

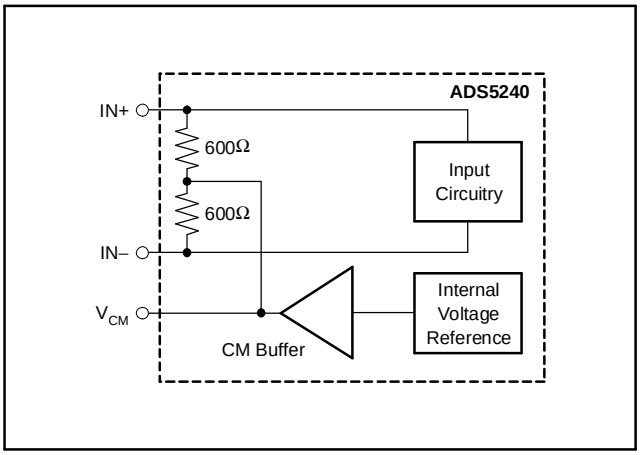


Figure 14. Analog Input Bias Circuitry

The sampling capacitor used to sample the inputs is 4pF. The choice of the external AC coupling capacitor is dictated by the attenuation at the lowest desired input frequency of operation. The attenuation resulting from using a 10nF AC coupling capacitor is 0.04%.

If the input is DC-coupled, then the output common-mode voltage of the circuit driving the ADS5240 should match the V_{CM} (which is provided as an output pin) to within ±50mV. It is recommended that the output common-mode of the driving circuit be derived from V_{CM} provided by the device.

The sampling circuit consists of a low-pass RC filter at the input to filter out noise components that might be differentially coupled on the input pins. The inputs are sampled on two 4pF capacitors, see Figure 15. The sampling on the capacitors is done with respect to an internally-generated common-mode voltage (INCM). The switches connecting the sampling capacitors to the INCM are opened out first (before the switches connecting them to the analog inputs). This ensures that the charge injection arising out of the switches opening is independent of the input signal amplitude to a first-order of approximation. SP refers to a sampling clock whose falling edge comes an instant before the SAMPLE clock. The falling edge of SP determines the sampling instant.

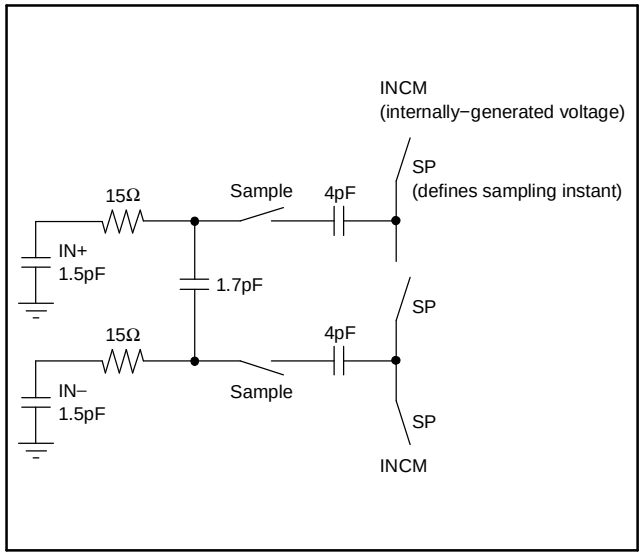


Figure 15. Input Circuitry

INPUT OVER-VOLTAGE RECOVERY

The differential full-scale input peak-to-peak supported by the ADS5240 is 2V. For a nominal value of V_{CM} (1.5V), IN_P and IN_N can swing from 1V to 2V. The ADS5240 is specially designed to handle an over-voltage differential peak-to-peak voltage of 4V (2.5V and 0.5V swings on IN_P and IN_N). If the input common-mode is not considerably off from V_{CM} during overload (less than 300mV), recovery from an over-voltage input condition is expected to be within 4 clock cycles. All of the amplifiers in the SHA and ADC are specially designed for excellent recovery from an overload signal.

REFERENCE CIRCUIT DESIGN

The digital beam-forming algorithm relies on gain matching across all receiver channels. (A typical system would have about 128 ADCs on the board.) In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the four channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at pin I_{SET}. Using a 56.2kΩ resistor on I_{SET} generates an internal reference current of 20µA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external resistor at I_{SET} reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56.2kΩ so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates a voltage called V_{CM}, which is set to the midlevel of REF_T and REF_B, and is accessible on a pin. The internal buffer driving V_{CM} has a drive of ±2mA. It is meant as a reference voltage to derive the input common-mode in case the input is directly coupled.

When using the internal reference mode, a resistor of 2Ω should be added between the reference pins (REF_T and REF_B) and the decoupling capacitor, as shown in Figure 16.

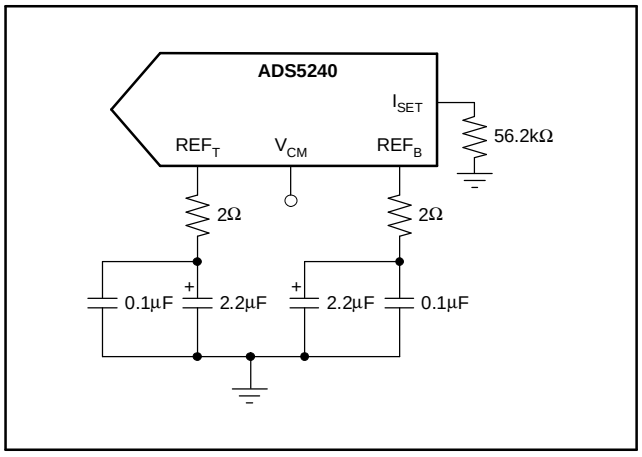


Figure 16. Internal Reference Mode

The device also supports the use of external reference voltages. This mode involves forcing REF_T and REF_B externally. In this mode, the internal reference buffer is tri-stated. Since the switching current for the four ADCs come from the externally-forced references, it is possible for the performance to be slightly less than when the internal references are used. It should be noted that in this mode, V_{CM} and ISET continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM}.

CLOCKING

The four channels on the chip run off a single ADCLK input. To ensure that the aperture delay and jitter are same for all the channels, a clock tree network is used to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point all the way to the sample-and-hold. This ensures that the performance and timing for all the channels are identical. The use

of the clock tree for matching introduces an aperture delay, which is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched. The aperture delays for all channels are matched. However, across conditions of temperature, supply voltage, and devices, the aperture delay averages 3.1ns.

The input ADCLK should ideally have a 50% duty cycle. However, while routing ADCLK to different components on board, the duty cycle of the ADCLK reaching the ADS5240 could deviate from 50%. A smaller (or larger) duty cycle eats into the time available for sample or hold phases of each circuit, and is therefore not optimal. For this reason, the internal PLL is used to generate an internal clock that has 50% duty cycle.

The use of the PLL automatically dictates the minimum sampling rate to be about 20MSPS.

LVDS BUFFERS

The LVDS buffer has two current sources, as shown in Figure 17. OUT_P and OUT_N are loaded externally by a resistive load that is ideally about 100Ω. Depending on the data being 0 or 1, the currents are directed in one or the other direction through the resistor. While the lower side current source is a constant current source, the higher side current source is controlled through a feedback loop to maintain the output common mode constant. The LVDS buffer has four current settings. The default current setting is 3.5mA, and gives a differential drop of about ±350mV across the 100Ω resistor.

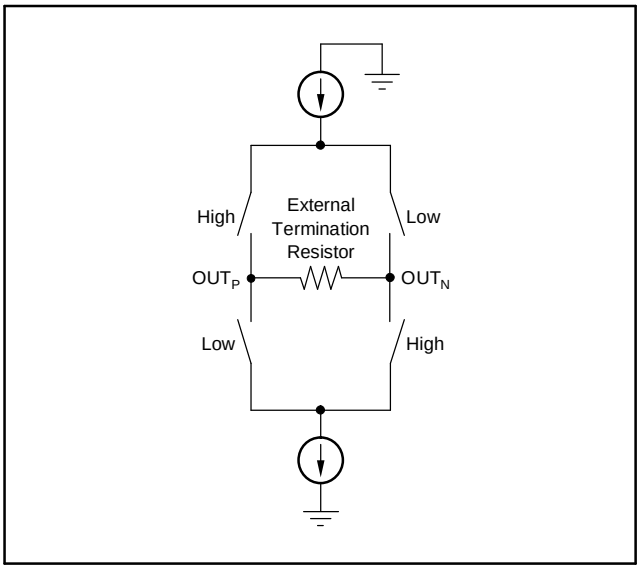


Figure 17. LVDS Buffer

The LVDS buffer gets data from a serializer that takes the output data from each channel and serializes it into a single data stream. For a clock frequency of 40MHz, the data rate output by the serializer is 480MBPS. The data comes out LSB first, with a register programmability to revert to MSB first. The serializer also gives out a 1x clock and a 6x clock. The 6x clock (denoted as $LCLK_P/LCLK_N$) is meant to synchronize the capture of the LVDS data. The deskew mode can be enabled as well, using a register setting. This mode gives out a data stream of alternate 0s and 1s and can be used determine the relative delay between the 6x clock and the output data for optimum capture. A 1x clock is also generated by the serializer and transmitted by the LVDS buffer. The 1x clock (referred to as $ADCLK_P/ADCLK_N$) is used to determine the start of the 12-bit data frame. The sync mode (enabled through a register setting) gives out a data of six 0s followed by six 1s. Using this mode, the 1x clock can be used to determine the start of the data frame. In addition to the deskew mode pattern and the sync pattern, a custom pattern can be defined by the user and output from the LVDS buffer.

NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One of the main sources of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the chip are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on the following:

1. The effective inductances of each of the supply/ground sets.
2. The isolation between the digital and analog supply/ground sets.

Smaller effective inductance of the supply/ground pins leads to better suppression of the noise. For this reason, multiple pins are used to drive each supply/ground. It is also critical to ensure that the impedances of the supply and ground lines on board are kept to the minimum possible values. Use of ground planes in the board as well as large decoupling capacitors between the supply and ground lines are necessary to get the best possible SNR from the device.

It is recommended that the isolation be maintained onboard by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS.

The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

POWER-DOWN MODE

The ADS5240 has a power-down pin, PD. Pulling PD high causes the device to enter the power-down mode. In this mode, the reference and clock circuitry as well as all the channels are powered down. Device power consumption drops to less than 100mW in this mode. Individual channels can also be selectively powered down by programming registers.

The ADS5240 also has an internal circuit that monitors the state of stopped clocks. If ADCLK is stopped (or if it runs at a speed < 3MHz), this monitoring circuit generates a logic signal that puts the device in a power-down state. As a result, the power consumption of the device is reduced when ADCLK is stopped. This circuit can also be disabled using register options.

SUPPLY SEQUENCE

The following supply sequence is recommended for powering up the device:

1. AVDD is powered up.
2. LVDD is powered up.

During the power-up ramp, the AVDD and LVDD supplies should track each other to within 0.6V.

If this sequencing is not possible, then it is recommended that AVDD and LVDD be powered up simultaneously.

After the supplies have stabilized, it is required to give the device an active RESET pulse. This results in all internal registers getting reset to their default value of 0 (inactive). Without RESET, it is possible that some registers might be in their non-default state on power-up. This could cause the device to malfunction.

LAYOUT OF PCB WITH PowerPAD THERMALLY-ENHANCED PACKAGES

The ADS5240 is housed in an 64-lead PowerPAD thermally-enhanced package. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the printed circuit board (PCB) must be designed with this technology in mind. Please refer to PowerPAD brief SLMA004 *PowerPAD Made Easy* (refer to our web site at www.ti.com), which addresses the specific considerations required when integrating a PowerPAD package into a PCB design. For more detailed information, including thermal modeling and repair procedures, please see technical brief SLMA002, *PowerPAD Thermally-Enhanced Package* (available for download at www.ti.com).

CONNECTING HIGH-SPEED, MULTI-CHANNEL ADCs TO XILINX FPGAs

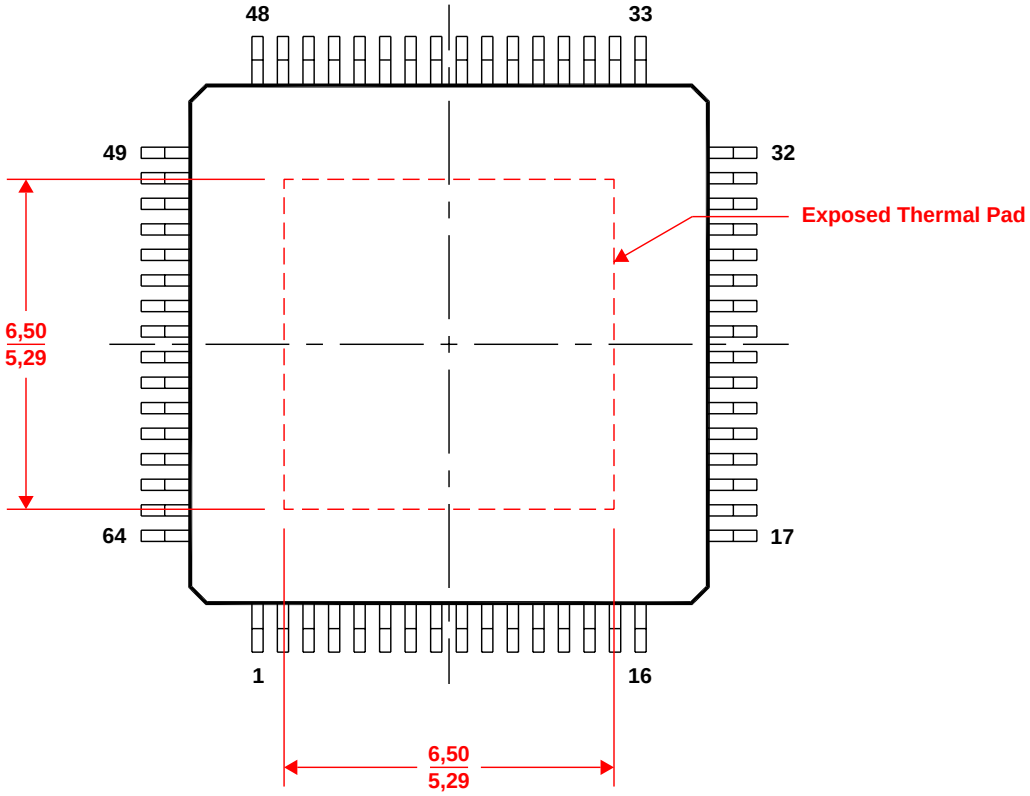
A separate application note (XAPP774) describing how to connect TI's high-speed, multi-channel ADCs with serial LVDS outputs to XILINX FPGAs can be downloaded directly from the XILINX website (http://www.xilinx.com).

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

PPTD012

Exposed Thermal Pad Dimensions

PACKAGE OPTION ADDENDUM

12-May-2005

PACKAGING INFORMATION

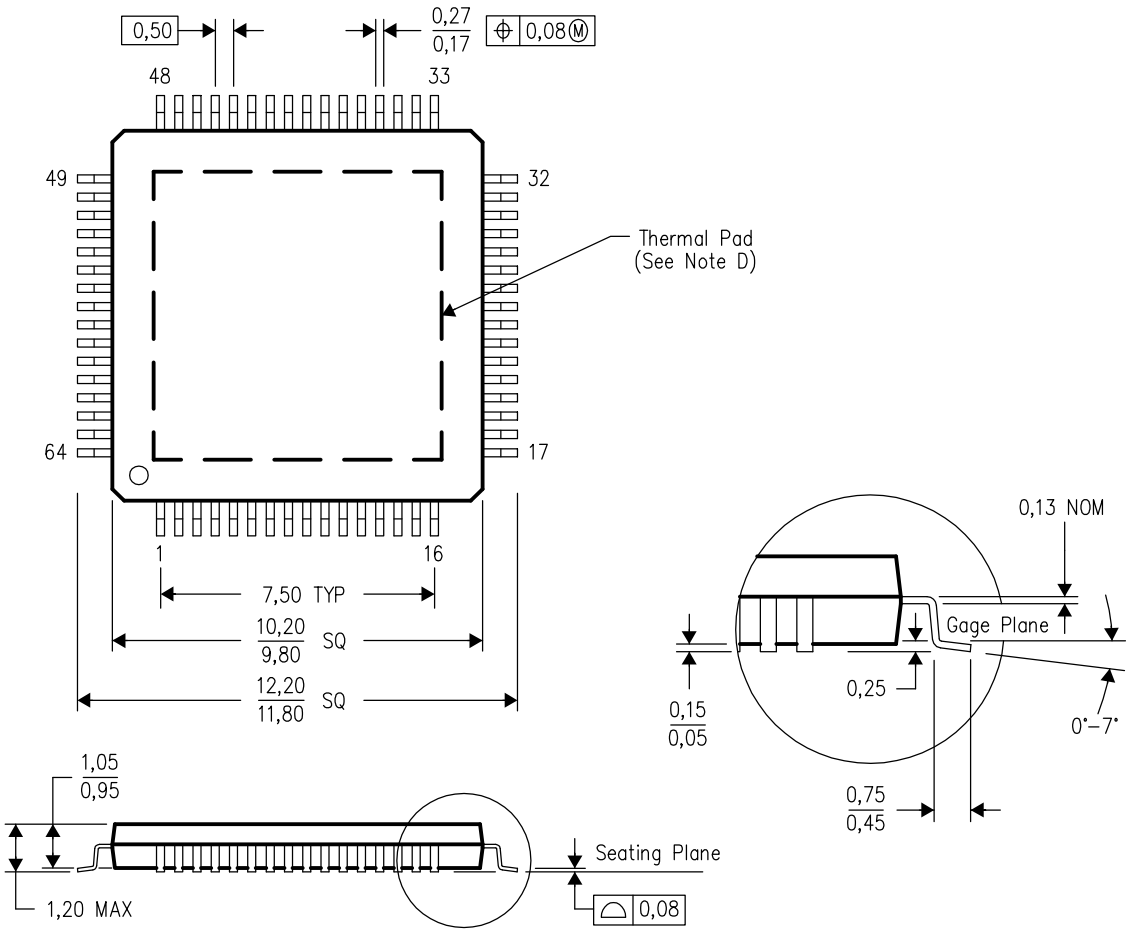
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS5240IPAP	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5240IPAPG4	ACTIVE	HTQFP	PAP	64	160	TBD	Call TI	Call TI
ADS5240IPAPT	ACTIVE	HTQFP	PAP	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS5240IPAPTG4	ACTIVE	HTQFP	PAP	64	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



4147702/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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