



CY74FCT2240T CY74FCT2244T

SCCS036 - September 1994 - Revised March 2000

8-Bit Buffers/Line Drivers

Features

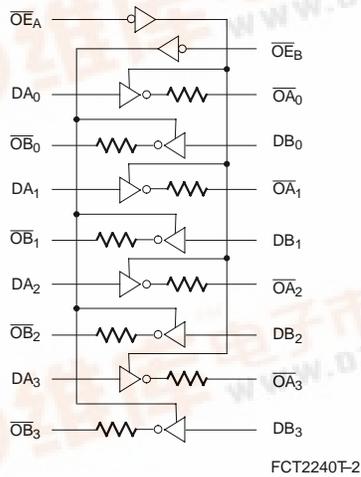
- Function and pinout compatible with FCT and F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 4.1 ns max. (Com'I) FCT-A speed at 4.8 ns max. (Com'I)
- TTL output level versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature permits live insertion
- ESD > 2000V
- Fully compatible with TTL input and output logic levels
- Sink current 12 mA
Source current 15 mA
- Extended commercial temp. range of -40°C to +85°C
- Three-state outputs

Functional Description

The FCT2240T and FCT2244T are octal buffers and line drivers that include on-chip 25Ω terminating resistors at each of the outputs, to minimize noise resulting from reflections or standing waves in high-performance applications. The on-chip resistors reduce overall board space and component count. Designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers, these devices provide speed and drive capabilities commensurate with their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without the need for external components.

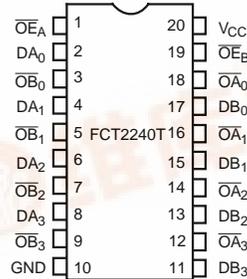
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram FCT2240T



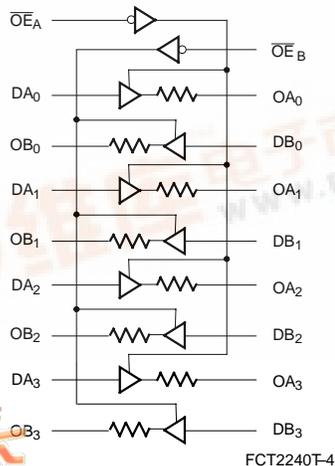
Pin Configurations

SOIC/QSOP Top View

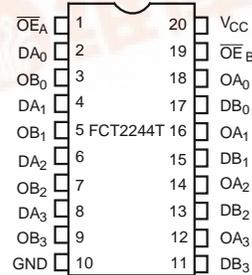


FCT2240T-3

Logic Block Diagram FCT2244T



DIP/SOIC/QSOP Top View



FCT2240T-6



Function Table FCT2240T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	H
L	L	H	L
H	H	X	Z

Function Table FCT2244T^[1]

Inputs			Output
\overline{OE}_A	\overline{OE}_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -65°C to +135°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) 120 mA

Power Dissipation 0.5W

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	T, AT, CT	-40°C to +85°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	Com'l	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =12 mA	Com'l		0.3	0.55	V
R _{OUT}	Output Resistance	V _{CC} =Min., I _{OL} =12 mA	Com'l	20	25	40	Ω
V _{IH}	Input HIGH Voltage			2.0			V
V _{IL}	Input LOW Voltage					0.8	V
V _H	Hysteresis ^[6]	All inputs			0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA			-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}				5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V				±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V				±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} =Max., V _{OUT} =2.7V				10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} =Max., V _{OUT} =0.5V				-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V		-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V				±1	μA

Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
- T_A is the "instant on" case temperature.
- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤ 0.2V, V _{IN} ≥ V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE ₁ =OE ₂ =GND, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE ₁ =OE ₂ =GND, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f ₁ =10 MHz, OE ₁ =OE ₂ =GND, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE ₁ =OE ₂ =GND, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f ₁ =2.5 MHz, OE ₁ =OE ₂ =GND, V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics FCT2240T Over the Operating Range^[12]

Parameter	Description	FCT2240T		FCT2240AT		FCT2240CT		Unit	Fig. No. ^[13]
		Commercial		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	8.0	1.5	8.0	1.5	4.1	ns	1, 2
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.0	1.5	10.0	1.5	5.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	9.5	1.5	9.5	1.5	5.2	ns	1, 7, 8

Switching Characteristics FCT2244T Over the Operating Range^[12]

Parameter	Description	FCT2244T		FCT2244AT		FCT2244CT		Unit	Fig. No. ^[13]
		Commercial		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Input	1.5	6.5	1.5	4.6	1.5	4.1	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	8.0	1.5	6.2	1.5	5.8	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	7.0	1.5	5.6	1.5	5.2	ns	1, 7, 8

Notes:

12. Minimum limits are specified but not tested on Propagation Delays.
13. See "Parameter Measurement Information" in the General Information section.

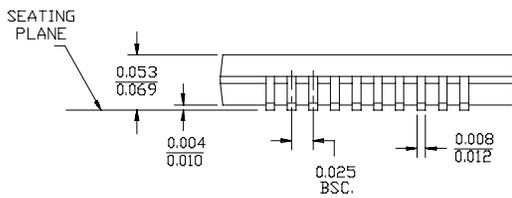
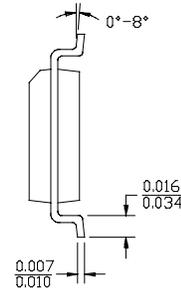
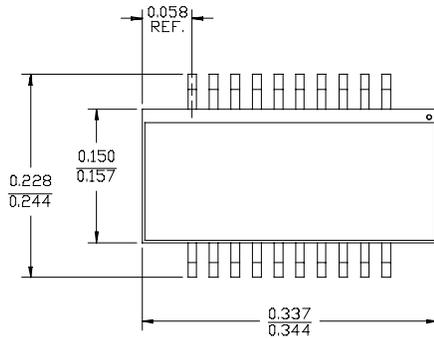
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT2240CTQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2240CTSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
4.8	CY74FCT2240ATQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
8.0	CY74FCT2240TSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	Commercial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT2244CTQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2244CTSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY74FCT2244ATQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2244ATSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	
6.5	CY74FCT2244TQCT	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT2244TSOC/SOCT	S5	20-Lead (300-Mil) Molded SOIC	

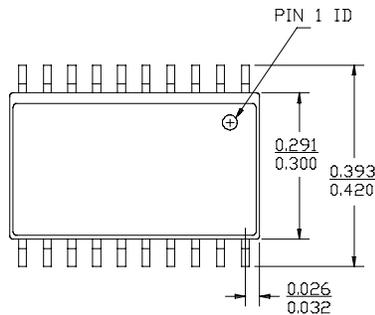
Package Diagrams

20-Lead Quarter Size Outline Q5

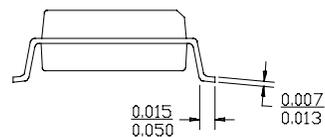
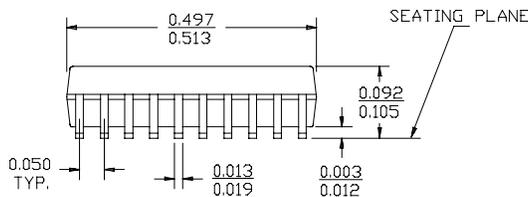


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

20-Lead (300-Mil) Molded SOIC S5



DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.



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