Data sheet acquired from Cypress Semiconductor Corporation.
Data sheet modified to remove devices not offered.

TEXAS INSTRUMENTS

CY74FCT652T

8-Bit Registered Transceiver

SCCS032 - September 1994 - Revised March 2000

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.4 ns max. (Com'l)**
  FCT-A speed at 6.3 ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **Sink Current 64 mA**
  Source Current 32 mA
- **Independent register for A and B buses**
- **Multiplexed real-time and stored data transfer**
- **Extended commercial range of –40˚C to +85˚C**

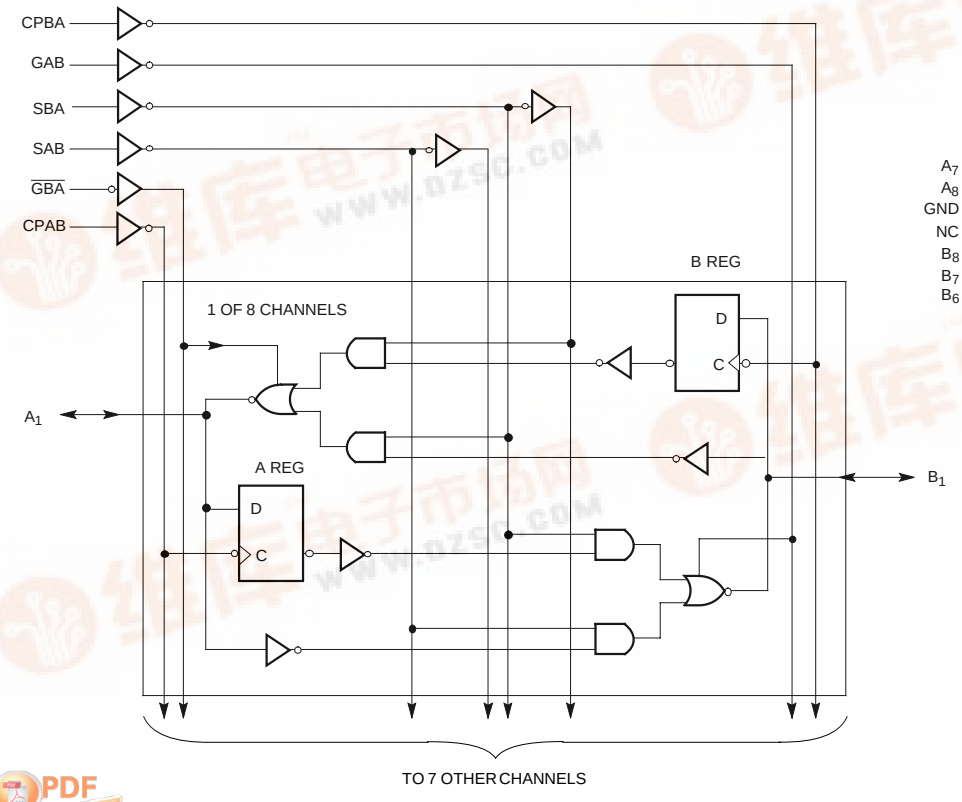
Functional Description

The FCT652T consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

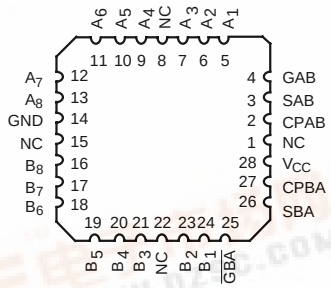
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

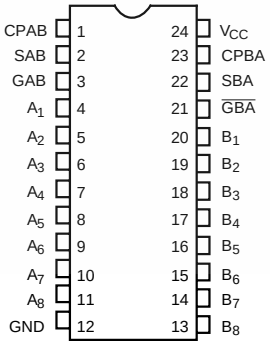


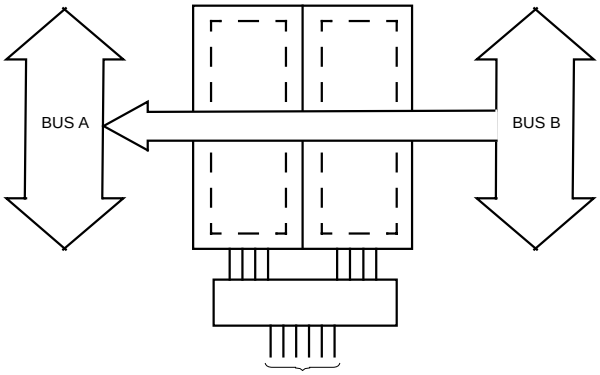
Pin Configurations

LCC
Top View



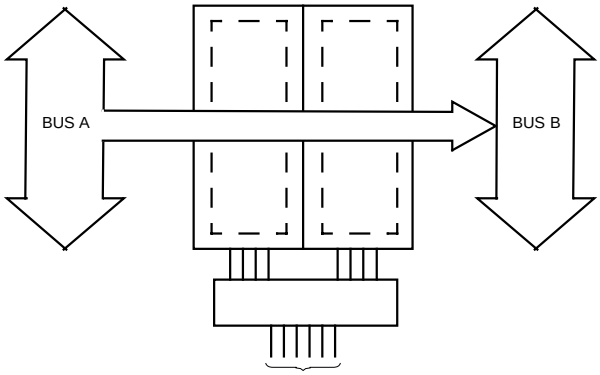
SOIC/QSOP
Top View





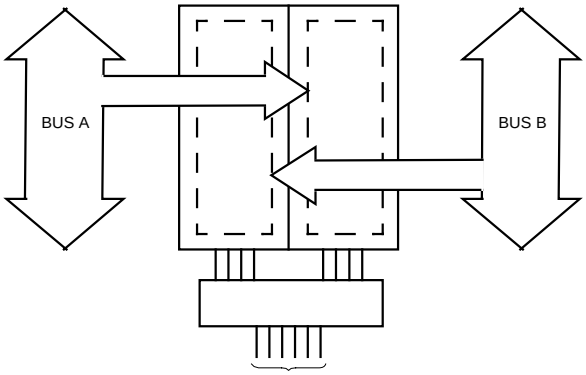
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A



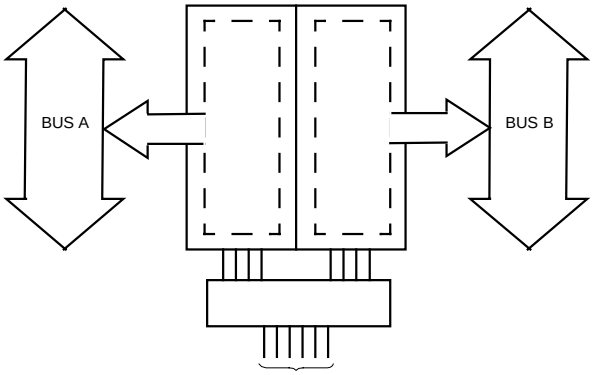
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

Real-Time Transfer
Bus A to Bus B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
X	H	⌐	X	X	X
L	X	X	⌐	X	X
L	H	⌐	⌐	X	X

Store Data from A and/or B



GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

Transferred Stored Data
to A and/or B

Function Table[1]

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	
L L	H H	H or L ⌐	H or L ⌐	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	⌐ ⌐	H or L ⌐	X X[1]	X X	Input Input	Unspecified[2] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ⌐	⌐ ⌐	X X	X X[1]	Unspecified[2] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

1. Select control=L: clocks can occur simultaneously. Select control=H: clocks must be staggered in order to load both registers. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. ⌐ = LOW-to-HIGH Transition.
2. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage.....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	T, AT, CT	–40°C to +85°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	2.0			V
		V_{CC}=Min., I_{OH}=–15 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.3	0.55	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Hysteresis[6]	All inputs		0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA		–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}			5	µA
I_{IH}	Input HIGH Current[6]	V_{CC}=Max., V_{IN}=2.7V			±1	µA
I_{IL}	Input LOW Current[6]	V_{CC}=Max., V_{IN}=0.5V			±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC}=Max., V_{OUT}=2.7V			10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT}=0.5V			–10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V	–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V			±1	µA

Capacitance[6]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Notes:

3. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V, f_1=0, Outputs Open[8]	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, GAB=GND, $\overline{GBA}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND SBA=V_{CC}, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, GAB=GND, $\overline{GBA}$=GND, SAB=CPAB=GND SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND SBA=V_{CC}, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	2.8	5.6[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=5 MHz, GAB=$\overline{GBA}$=GND, SAB=CPAB=GND SBA=V_{CC}, V_{IN}=3.4V or V_{IN}=GND	5.1	14.6[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[12]

Parameter	Description	FCT652T Commercial		FCT652AT Commercial		FCT652CT Commercial		Unit	Fig. No.[13]
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	9.0	1.5	6.3	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	1.5	14.0	1.5	9.8	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	1.5	9.0	1.5	6.3	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	9.0	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	1.5	11.0	1.5	7.7	1.5	6.2	ns	1, 5
t_S	Set-Up Time HIGH or LOW Bus to Clock	4.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW Bus to Clock	2.0		1.5		1.5		ns	4
t_W	Clock Pulse Width,[14] HIGH or LOW	6.0		5.0		5.0		ns	5

Ordering Information

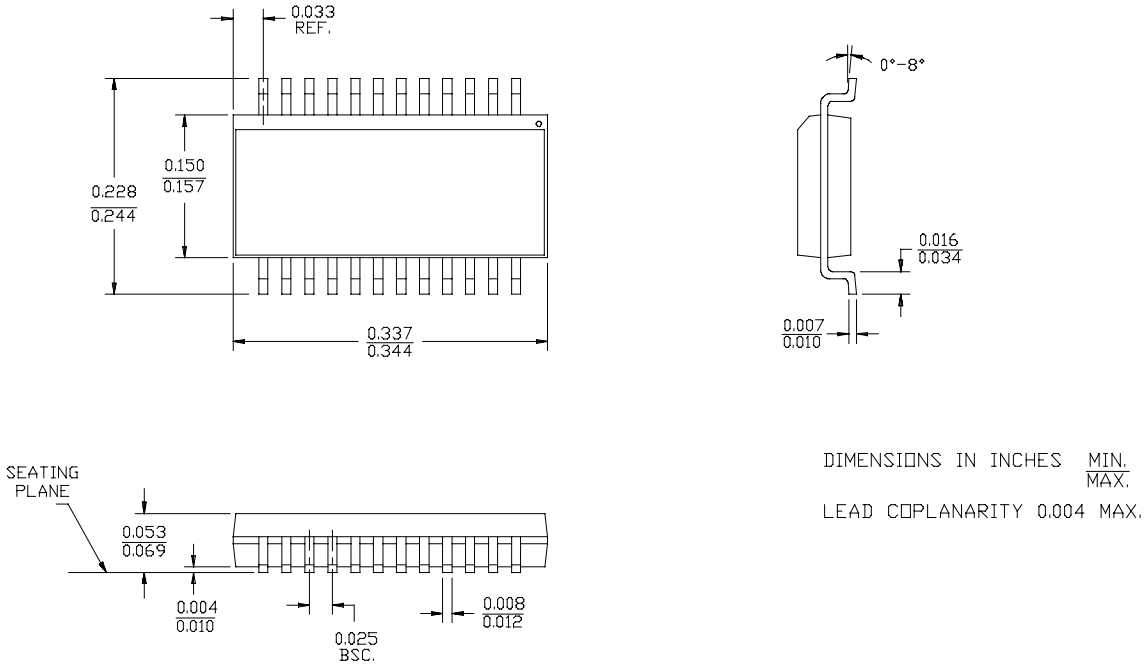
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT652CTQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
6.3	CY74FCT652ATQCT	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT652ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
9.0	CY74FCT652TQCT	Q13	24-Lead (150-Mil) QSOP	Commercial

Notes:

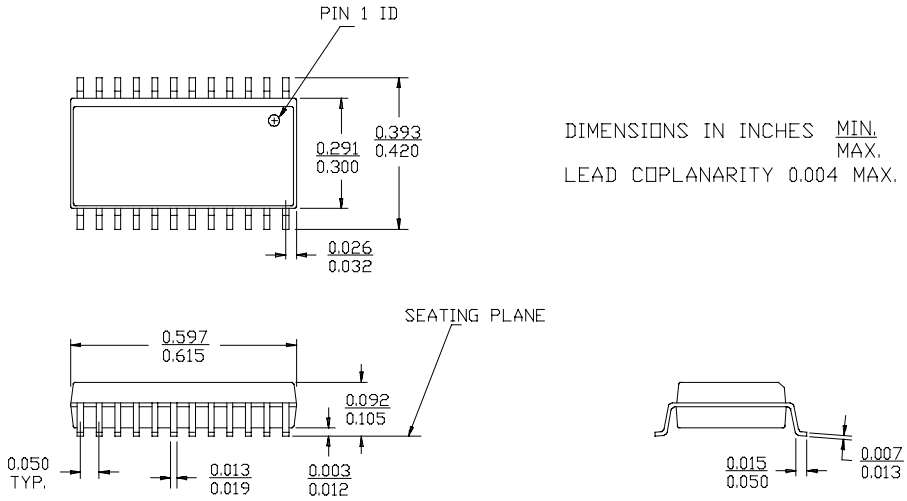
12. Minimum limits are specified but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.
14. With one data channel toggling, $t_W(L)=t_W(H)=4.0$ ns and $t_r=t_f=1.0$ ns.

Package Diagrams

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13



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