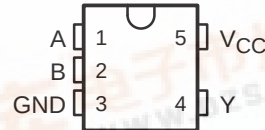
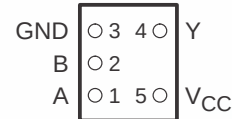


- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t_{pd} of 2.2 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single 2-input positive-NAND gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Tape and reel	SN74AUC1G00YEAR	___UA_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74AUC1G00YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74AUC1G00YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUC1G00YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74AUC1G00DBVR	U00_
	SOT (SC-70) – DCK	Tape and reel	SN74AUC1G00DCKR	UA_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN74AUC1G00
SINGLE 2-INPUT POSITIVE-NAND GATE

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description/ordering information (continued)

For more information about AUC Little Logic devices, please refer to the TI application report, *Applications of Texas Instruments AUC Sub-1-V Little Logic Devices*, literature number SCEA027.

FUNCTION TABLE		
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 3.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 3.6 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
YEA/YZA package	154°C/W
YEP/YZP package	132°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUC1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

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recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$	-0.7	mA
		$V_{CC} = 1.1\text{ V}$	-3	
		$V_{CC} = 1.4\text{ V}$	-5	
		$V_{CC} = 1.65\text{ V}$	-8	
		$V_{CC} = 2.3\text{ V}$	-9	
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7	mA
		$V_{CC} = 1.1\text{ V}$	3	
		$V_{CC} = 1.4\text{ V}$	5	
		$V_{CC} = 1.65\text{ V}$	8	
		$V_{CC} = 2.3\text{ V}$	9	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 0.8\text{ V to }1.95\text{ V}$	20	ns/V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	10	
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP [†]	MAX	UNIT
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	0.8 V to 2.7 V	$V_{CC}-0.1$			V
	$I_{OH} = -0.7\text{ mA}$	0.8 V		0.55		
	$I_{OH} = -3\text{ mA}$	1.1 V		0.8		
	$I_{OH} = -5\text{ mA}$	1.4 V		1		
	$I_{OH} = -8\text{ mA}$	1.65 V		1.2		
	$I_{OH} = -9\text{ mA}$	2.3 V		1.8		
V_{OL}	$I_{OL} = 100\text{ }\mu\text{A}$	0.8 V to 2.7 V			0.2	V
	$I_{OL} = 0.7\text{ mA}$	0.8 V		0.25		
	$I_{OL} = 3\text{ mA}$	1.1 V			0.3	
	$I_{OL} = 5\text{ mA}$	1.4 V			0.4	
	$I_{OL} = 8\text{ mA}$	1.65 V			0.45	
	$I_{OL} = 9\text{ mA}$	2.3 V			0.6	
I_I	A or B input	$V_I = V_{CC}$ or GND	0 to 2.7 V		± 5	μA
I_{off}		V_I or $V_O = 2.7\text{ V}$	0		± 10	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	μA
C_i		$V_I = V_{CC}$ or GND	2.5 V		3	pF

[†] All typical values are at $T_A = 25^\circ\text{C}$.

SN74AUC1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

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switching characteristics over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V ± 0.1 V		$V_{CC} = 1.5$ V ± 0.1 V		$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.7	0.9	3.2	0.5	2.2	†	†	†	†	†	ns

† This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V			$V_{CC} = 2.5$ V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.7	1.3	2.2	0.5	2	ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 0.8$ V	$V_{CC} = 1.2$ V	$V_{CC} = 1.5$ V	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10$ MHz	15	15	15	15	19	pF

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From Output Under Test

C_L
(see Note A)

R_L

R_L

$S1$

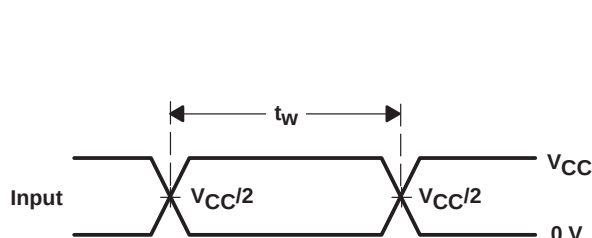
$2 \times V_{CC}$
Open

GND

LOAD CIRCUIT

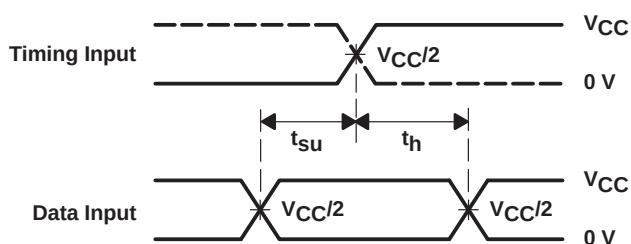
TEST	S1
t _{PLH} /t _{PHL} t _{PLZ} /t _{PZL} t _{PHZ} /t _{PZH}	Open 2 × V _{CC} GND

V _{CC}	C _L	R _L	V _Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V

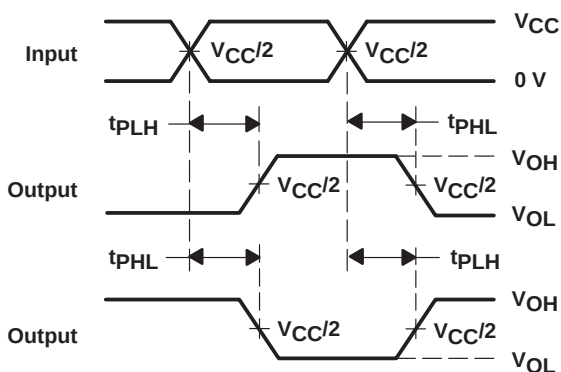


VOLTAGE WAVEFORMS

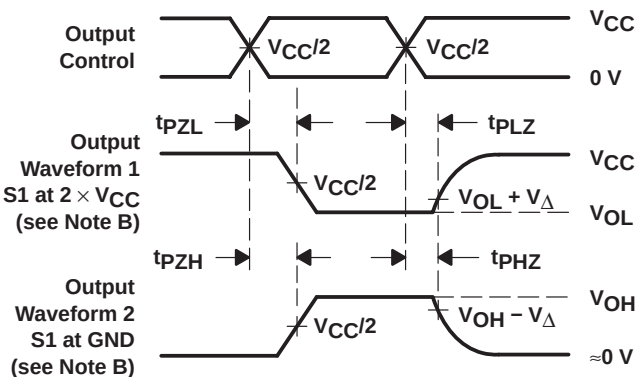
PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



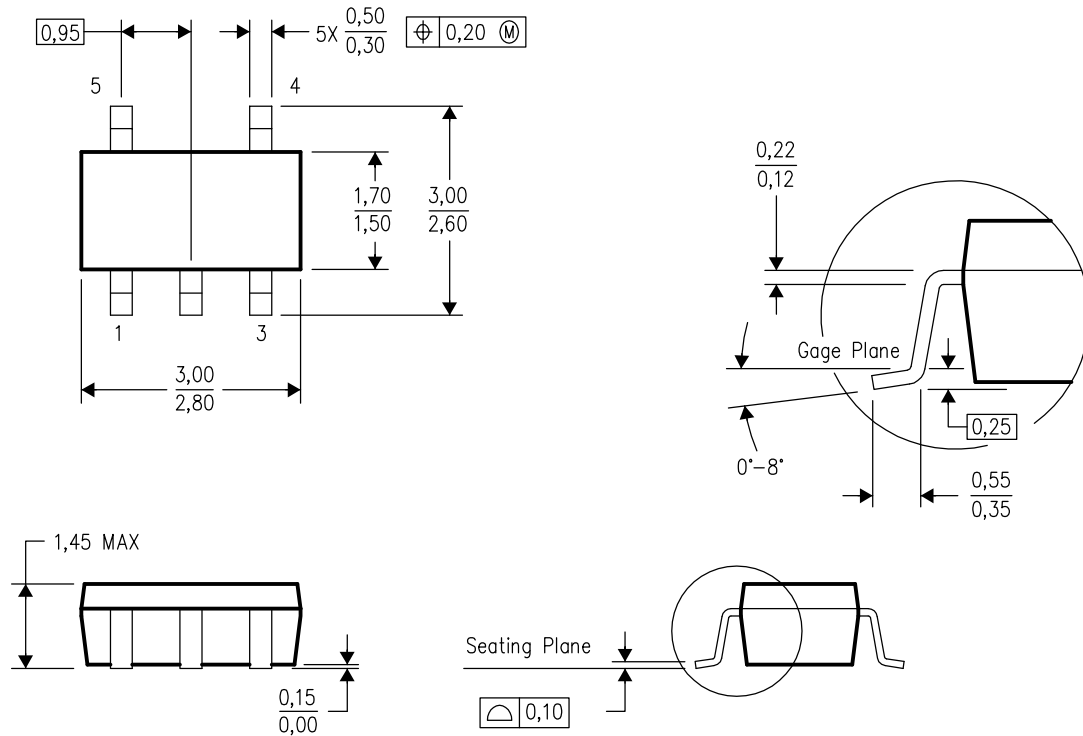
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- ### Figure 1. Load Circuit and Voltage Waveforms

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/H 10/2003

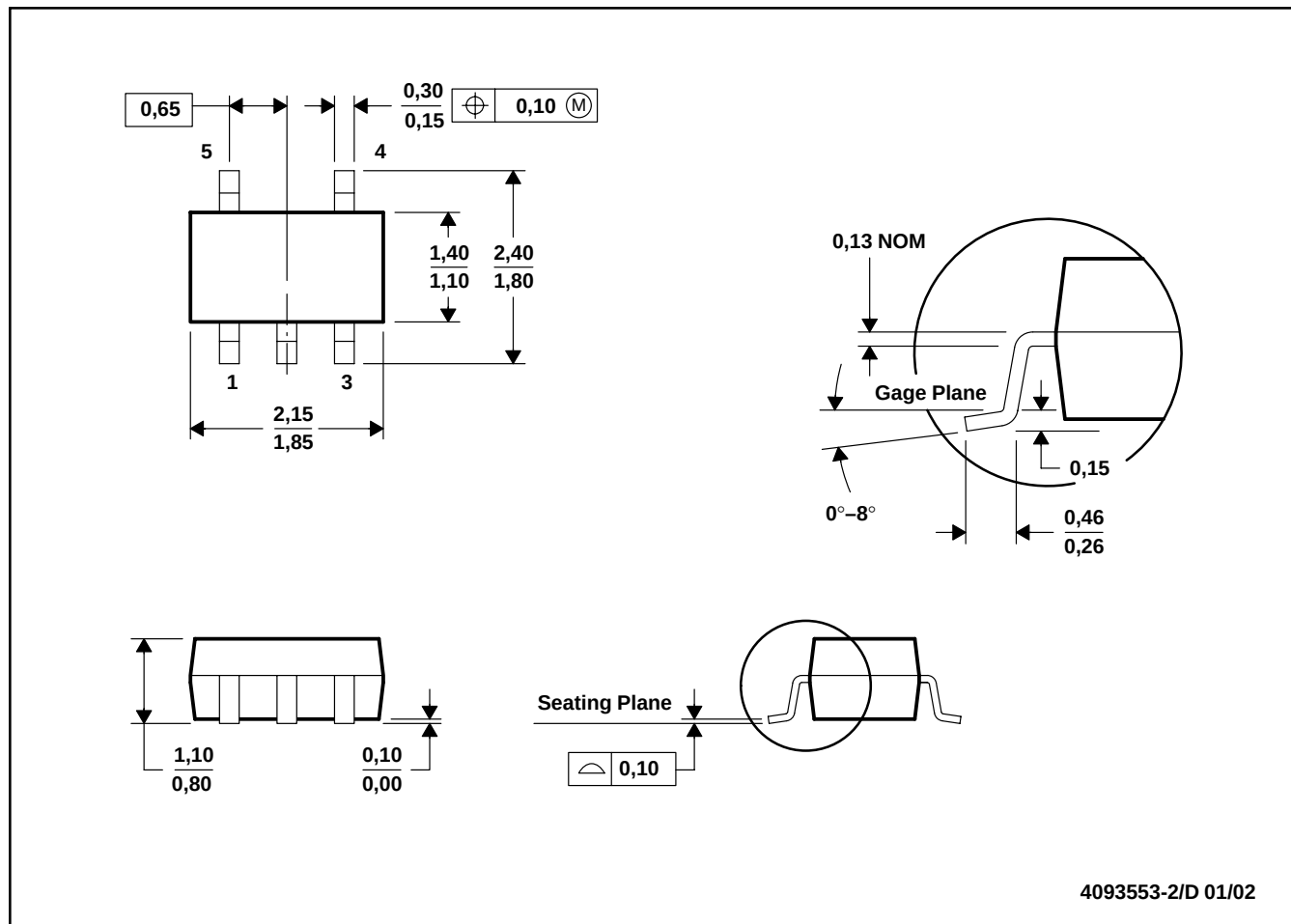
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178 Variation AA.

MECHANICAL DATA

MPDS025C – FEBRUARY 1997 – REVISED FEBRUARY 2002

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

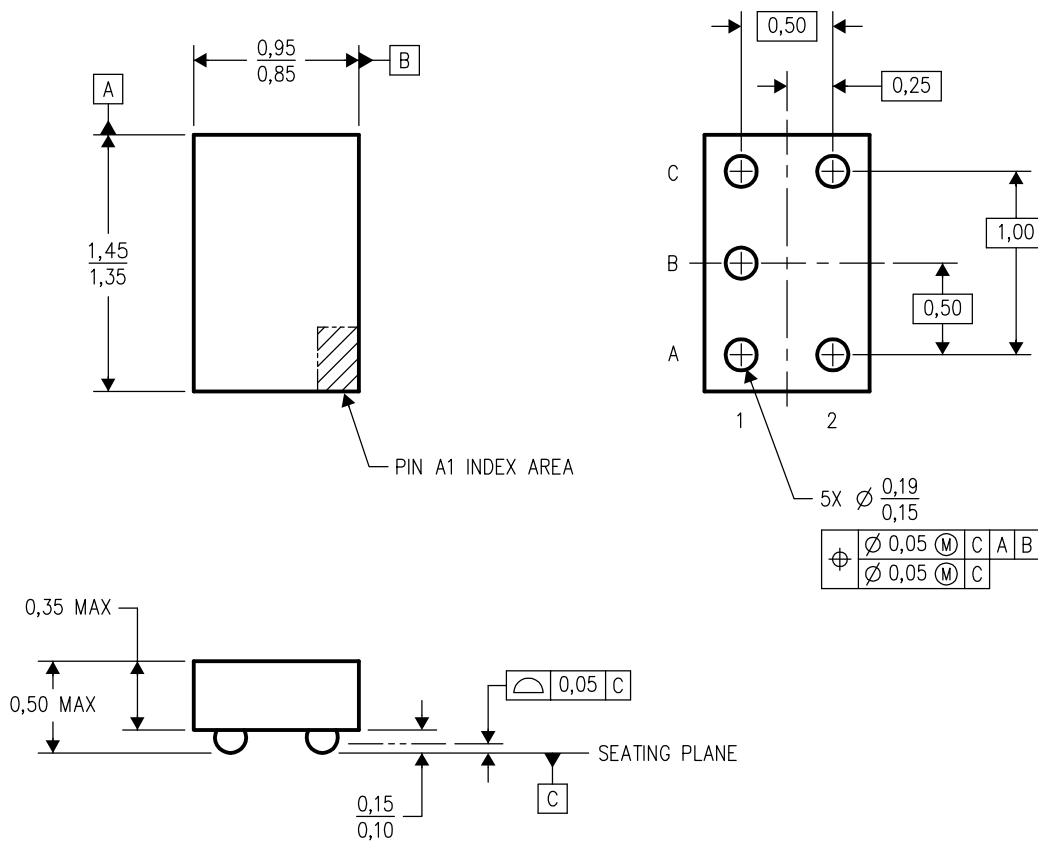


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-203

MECHANICAL DATA

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4203167-2/C 04/2002

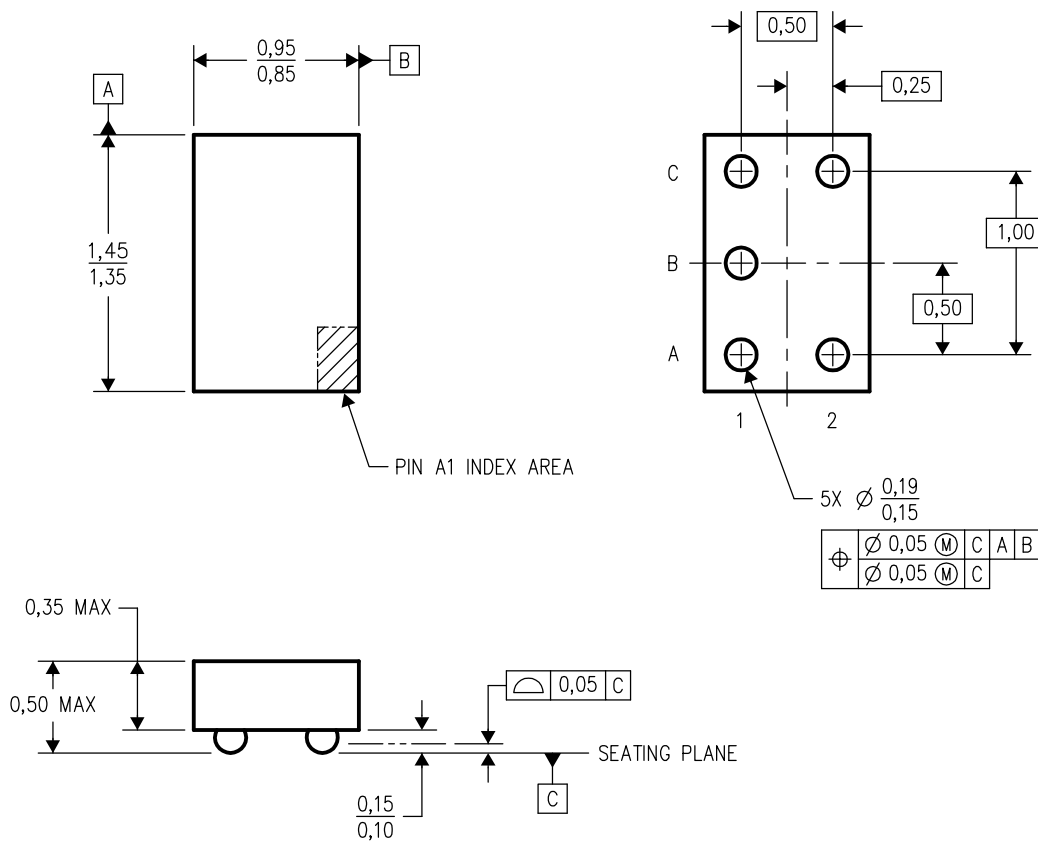
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

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MECHANICAL DATA

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204151-2/B 03/2002

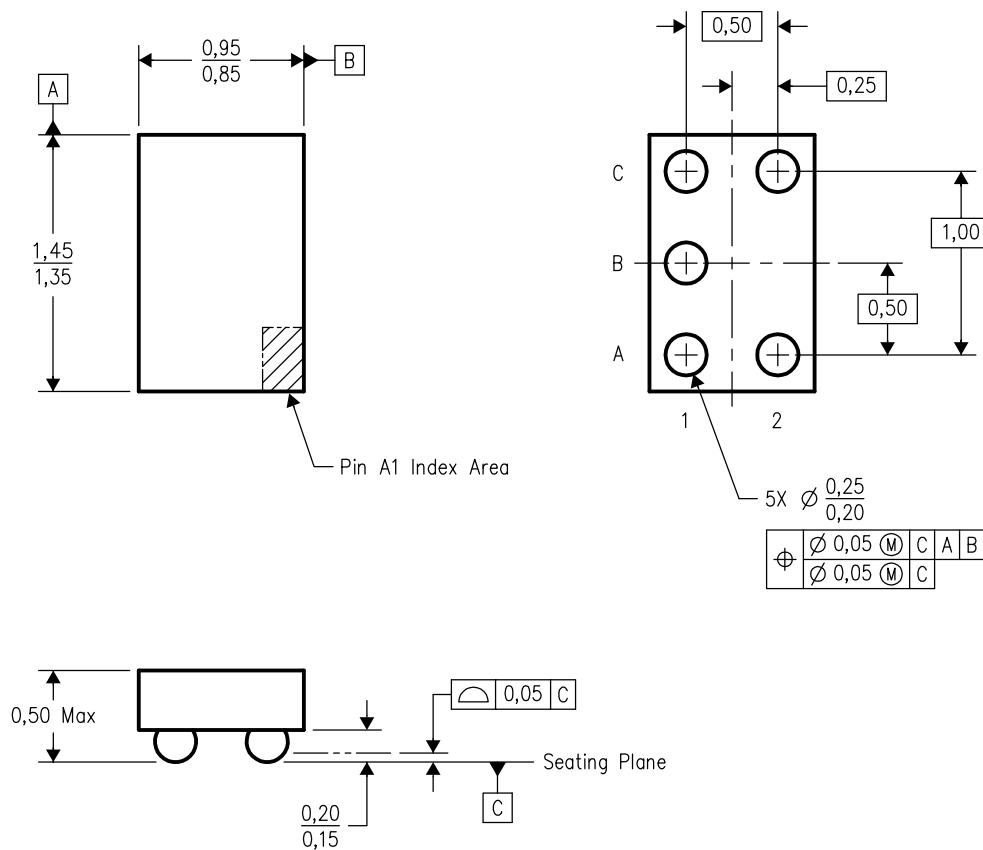
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. Package complies to JEDEC MO-211 variation EA.
 - E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

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MECHANICAL DATA

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204741-2/A 10/2002

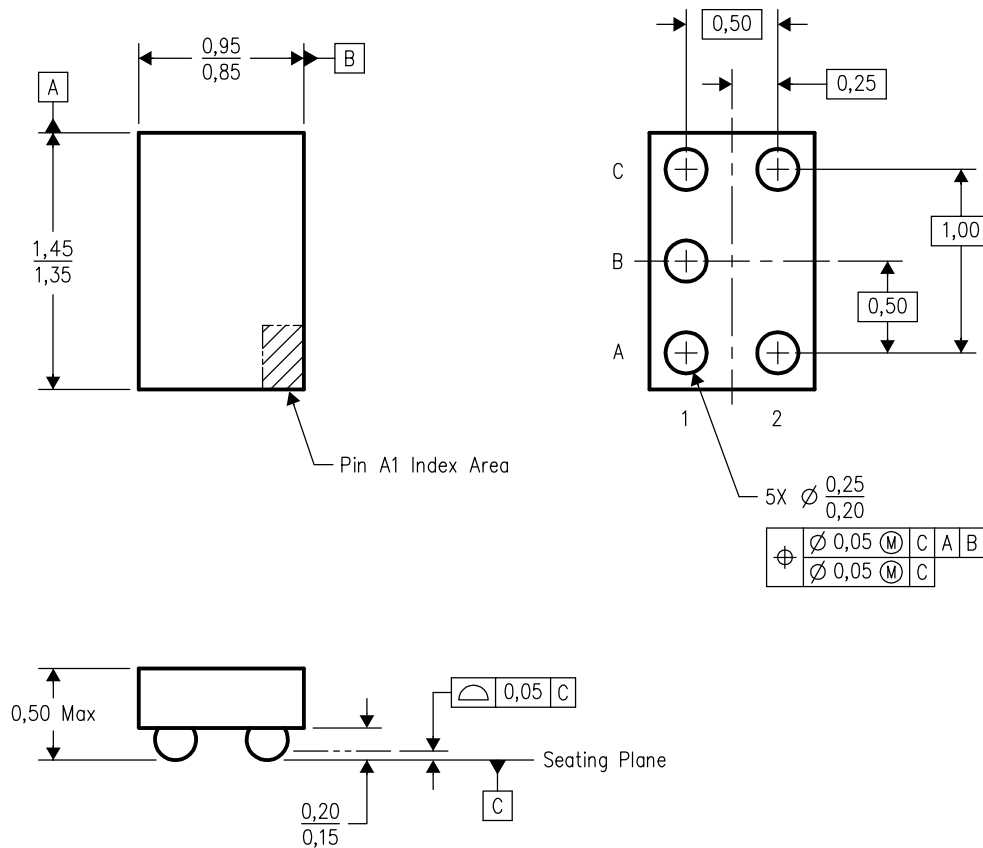
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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MECHANICAL DATA

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



4204725-2/A 10/2002

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

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