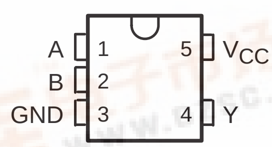
SN74AUP1G00
LOW-POWER SINGLE 2-INPUT POSITIVE-NAND GATE

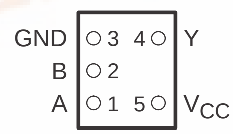
SCES604A – SEPTEMBER 2004 – REVISED APRIL 2005

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Low Static-Power Consumption; I_{CC} = 0.9-µA Max**
- **Low Dynamic-Power Consumption; C_{pd} = 4 pF Typical at 3.3 V**
- **Low Input Capacitance; C_i = 1.5 pF Typical**
- **Low Noise − Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typical at 3.3 V)**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.8 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **ESD Protection Exceeds ±5000-V With Human-Body Model**

DBV, DCK, OR DRL PACKAGE
(TOP VIEW)

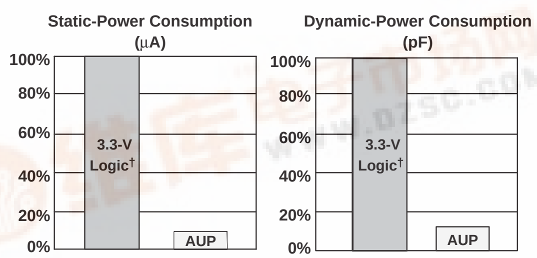


YEP OR YZP PACKAGE
(BOTTOM VIEW)



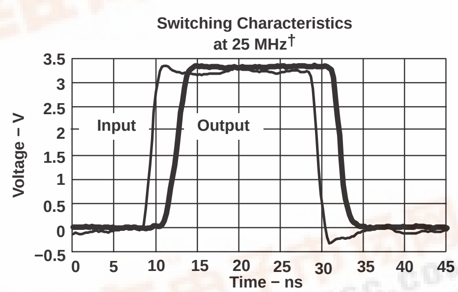
description/ordering information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figures 1 and 2).



† Single, dual, and triple gates.

Figure 1. AUP−The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF.

Figure 2. Excellent Signal Integrity

This single 2-input positive-NAND gate performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ − WCSP (DSBGA) 0.23-mm Large Bump − YEP	Tape and reel	SN74AUP1G00YEPR	_ _ _HA_
	NanoFree™ − WCSP (DSBGA) 0.23-mm Large Bump − YZP (Pb-free)	Tape and reel	SN74AUP1G00YZPR	
	SOT (SOT-23) − DBV	Tape and reel	SN74AUP1G00DBVR	H00_
	SOT (SC-70) − DCK	Tape and reel	SN74AUP1G00DCKR	HA_
	SOT (SOT-533) − DRL	Reel or 4000	SN74AUPG00DRLR	PREVIEW

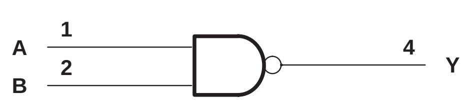
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . −0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . −0.5 V to 4.6 V
Output voltage range in the high or low state, V_O (see Note 1) . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . −50 mA
Continuous output current, I_O . . . ±20 mA
Continuous current through V_{CC} or GND . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package . . . 206°C/W
DCK package . . . 252°C/W
DRL package . . . 142°C/W
YEP/YZP package . . . 132°C/W
Storage temperature range, T_{stg} . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		−20	μA
		V_{CC} = 1.1 V		−1.1	mA
		V_{CC} = 1.4 V		−1.7	
		V_{CC} = 1.65		−1.9	
		V_{CC} = 2.3 V		−3.1	
		V_{CC} = 3 V		−4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25 °C MIN	T_A = 25 °C TYP	T_A = 25 °C MAX	T_A = −40 °C TO 85 °C MIN	T_A = −40 °C TO 85 °C MAX	UNIT
V_{OH}	I_{OH} = −20 μA	0.8 V to 3.6 V	V_{CC} − 0.1			V_{CC} − 0.1		V
	I_{OH} = −1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
	I_{OH} = −1.7 mA	1.4 V	1.11			1.03		
	I_{OH} = −1.9 mA	1.65 V	1.32			1.3		
	I_{OH} = −2.3 mA	2.3 V	2.05			1.97		
	I_{OH} = −3.1 mA		1.9			1.85		
	I_{OH} = −2.7 mA	3 V	2.72			2.67		
	I_{OH} = −4 mA		2.6			2.55		
V_{OL}	I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
	I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
	I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
	I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
	I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
	I_{OL} = 3.1 mA				0.44		0.45	
	I_{OL} = 2.7 mA	3 V			0.31		0.33	
	I_{OL} = 4 mA				0.44		0.45	
I_I A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}	V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}	V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}	V_I = V_{CC} − 0.6 V†, I_O = 0	3.3 V			40		50	μA
C_i	V_I = V_{CC} or GND	0 V		1.5				pF
		3.6 V		1.5				
C_o	V_O = GND	0 V		3				pF

† One input at V_{CC} − 0.6 V, other input at V_{CC} or GND

switching characteristics over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C MIN	T_A = 25 °C TYP	T_A = 25 °C MAX	T_A = −40 °C TO 85 °C MIN	T_A = −40 °C TO 85 °C MAX	UNIT
t_{pd}	A or B	Y	0.8 V		16.6				ns
			1.2 V ± 0.1 V	2.6	7	13.8	2.1	17.1	
			1.5 V ± 0.1 V	2.9	5	9.2	2.9	11.1	
			1.8 V ± 0.15 V	2	4	7.1	2	9	
			2.5 V ± 0.2 V	1.3	2.9	4.9	1.3	6.2	
			3.3 V ± 0.3 V	1	2.4	13.8	1	4.8	

switching characteristics over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		18.9				ns
			1.2 V ± 0.1 V	1.5	8	15.7	1	18.8	
			1.5 V ± 0.1 V	2.9	5.8	10.5	2.9	12.1	
			1.8 V ± 0.15 V	2	4.7	8.2	2	9.8	
			2.5 V ± 0.2 V	1.3	3.4	5.7	1.3	6.8	
			3.3 V ± 0.3 V	1	2.9	4.5	1	5.2	

switching characteristics over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		21.3				ns
			1.2 V ± 0.1 V	3.6	9	17.3	3.1	21.5	
			1.5 V ± 0.1 V	2.9	6.5	11.6	2.9	14	
			1.8 V ± 0.15 V	2	5.3	9.2	2	11.4	
			2.5 V ± 0.2 V	1.3	3.9	6.4	1.3	8	
			3.3 V ± 0.3 V	1	3.3	5.1	1	6.4	

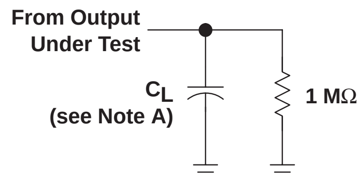
switching characteristics over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figures 3 and 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25 °C			T_A = −40 °C TO 85 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		28.4				ns
			1.2 V ± 0.1 V	4.9	11.9	21.9	4.4	27.1	
			1.5 V ± 0.1 V	2.9	8.6	14.7	2.9	17.7	
			1.8 V ± 0.15 V	2	7.1	11.5	2	14.2	
			2.5 V ± 0.2 V	1.3	5.3	8.1	1.3	10	
			3.3 V ± 0.3 V	1	4.5	6.5	1	8	

operating characteristics, T_A = 25°C

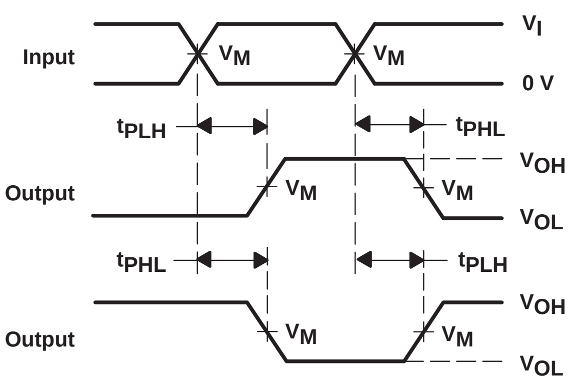
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V± 0.1 V	4	
			1.5 V± 0.1 V	4	
			1.8 V± 0.15 V	4	
			2.5 V± 0.2 V	4	
			3.3 V± 0.3 V	4	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

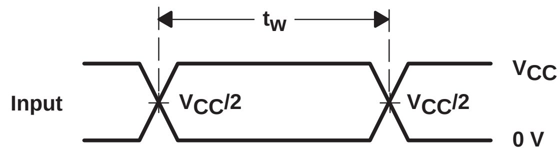


LOAD CIRCUIT

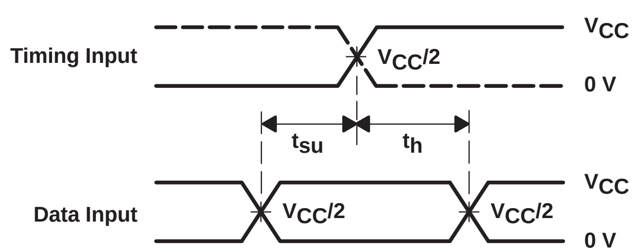
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

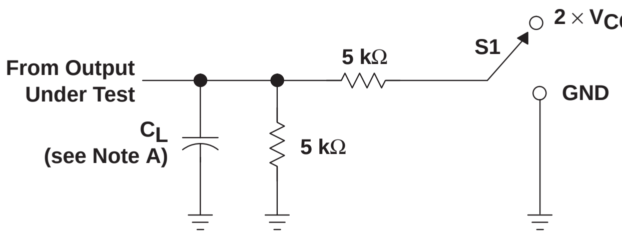


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd}.
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

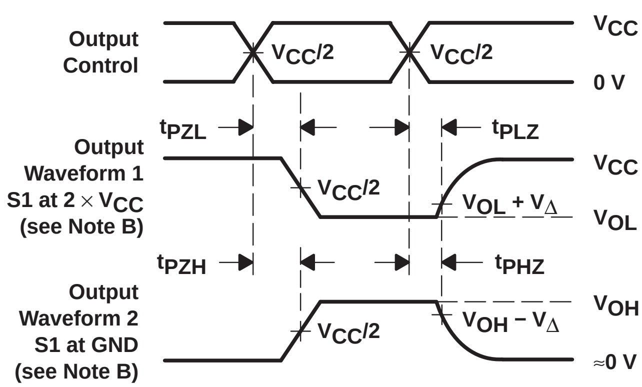
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74AUP1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DBVT	ACTIVE	SOT-23	DBV	5	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00DRLR	ACTIVE	SOP	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G00YEPR	ACTIVE	WCSP	YEP	5	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74AUP1G00YZPR	ACTIVE	WCSP	YZP	5	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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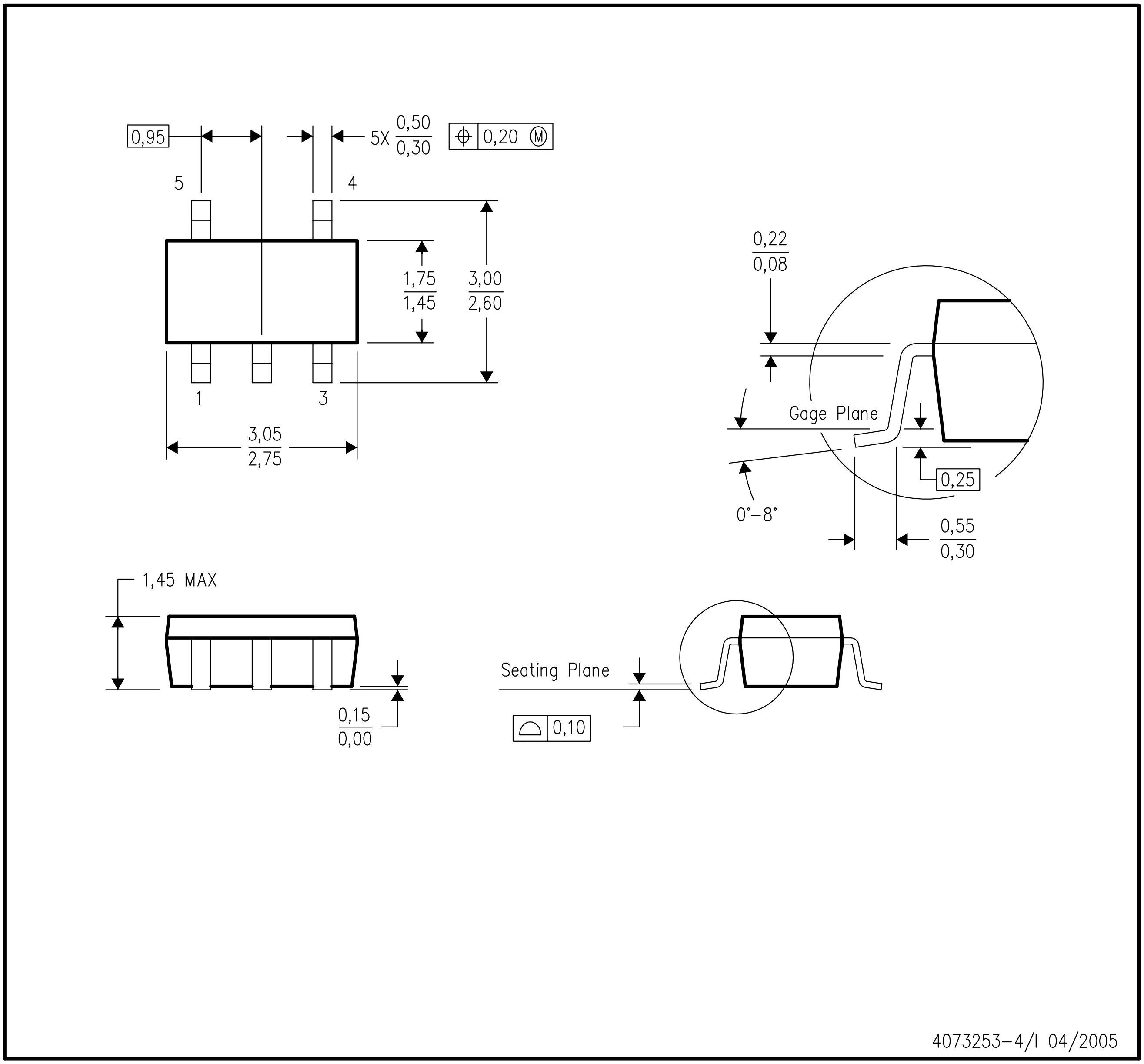
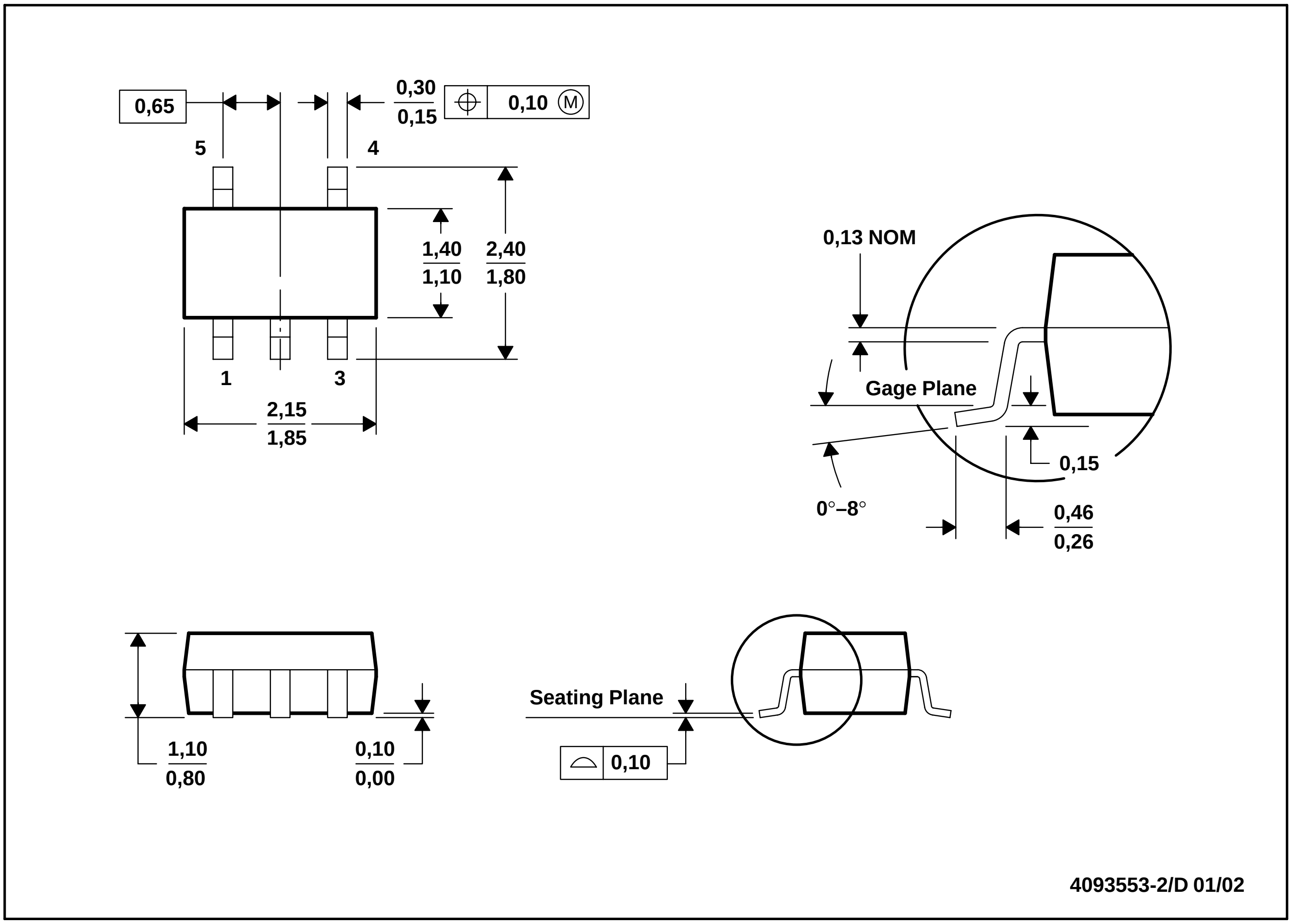
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



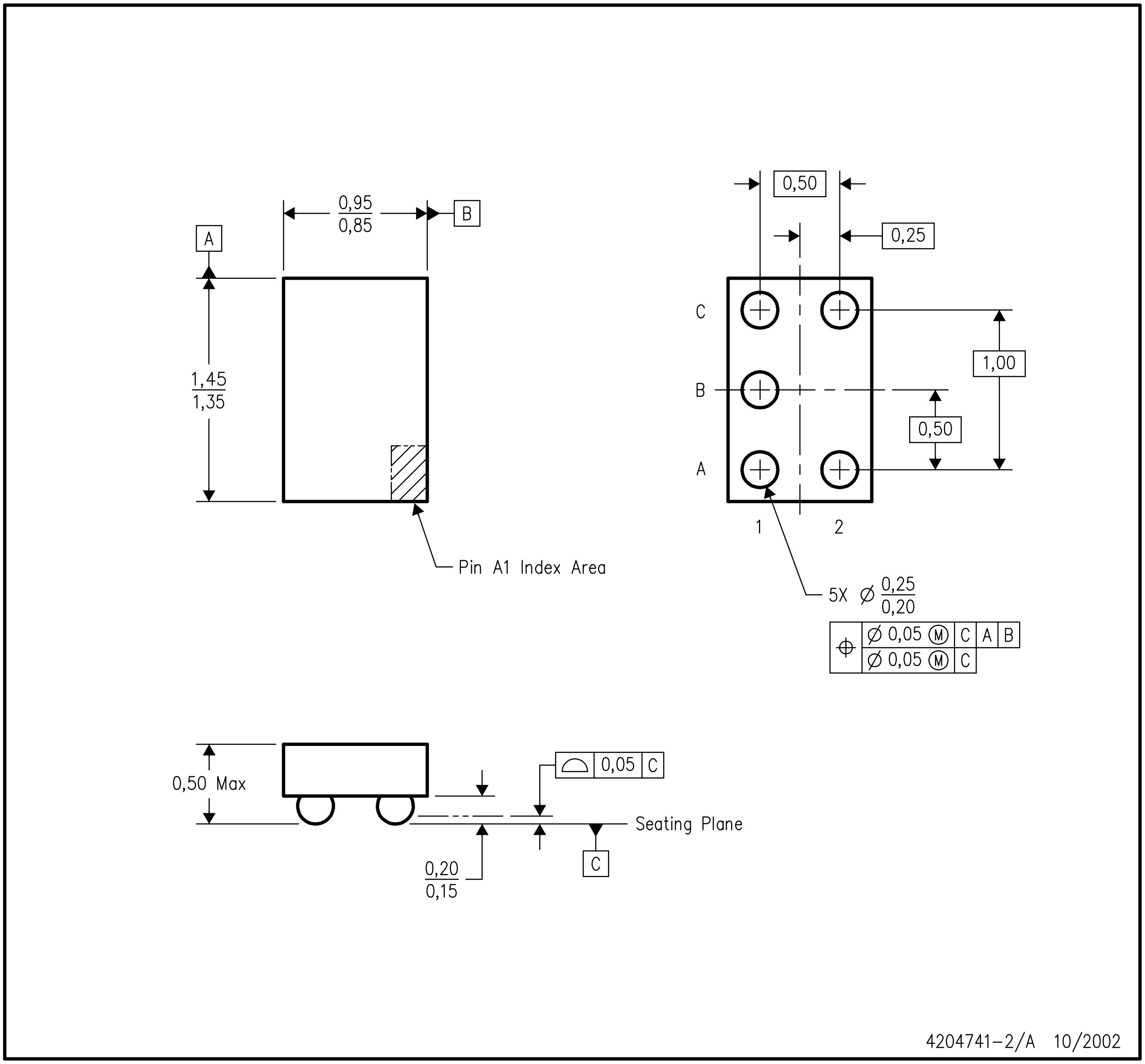
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

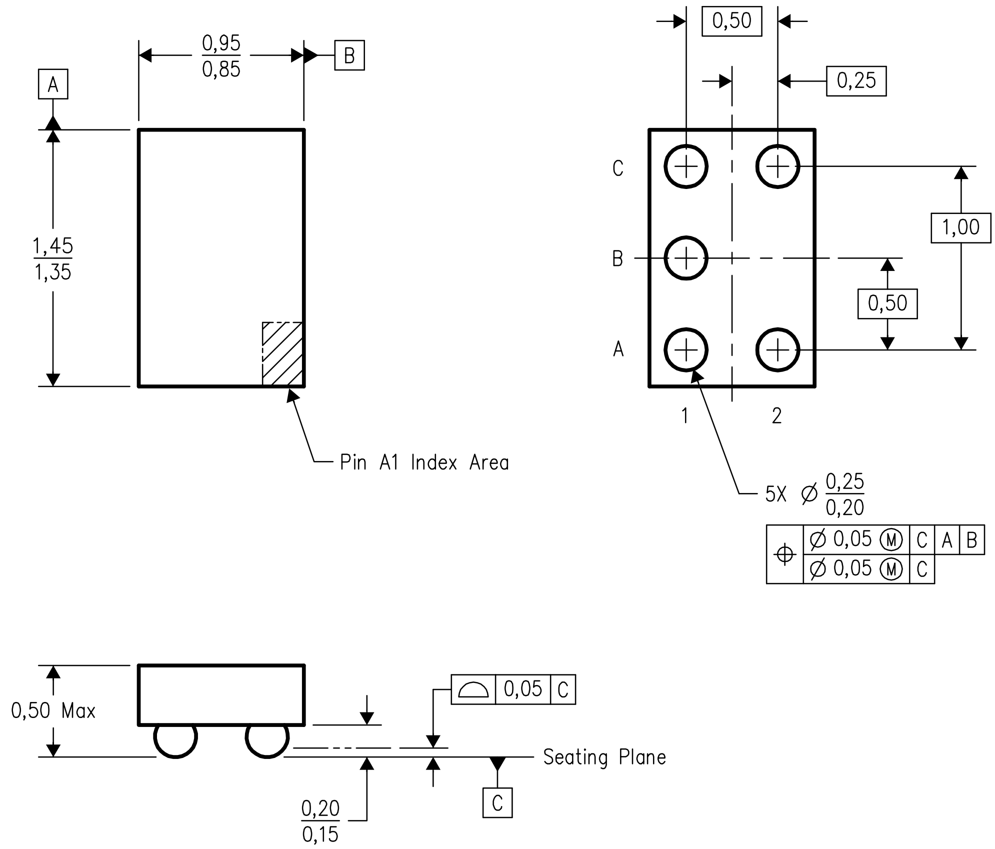
YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



4204725–2/A 10/2002

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin–lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead–free.

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