1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

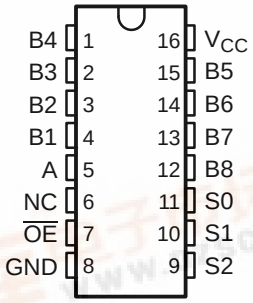
SCDS173A–AUGUST 2004–REVISED MARCH 2005

FEATURES

- High-Bandwidth Data Path (up to 500 MHz (1))
- Equivalent to IDTQS3VH251 Device
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4 Ω Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V V_{CC}
  - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typ)
- Fast Switching Frequency ($f_{\overline{OE}}$ or f_S = 20 MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (I_{CC} = 1 mA Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

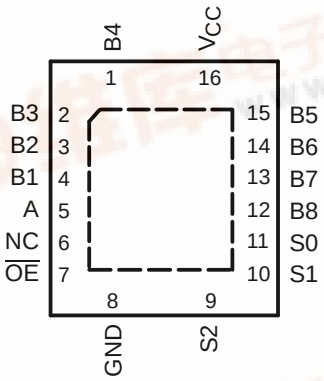
(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



NC - No internal connection

RGY PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q3251 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3251 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74CB3Q3251 is a 1-of-8 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S0, S1, S2) inputs control the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

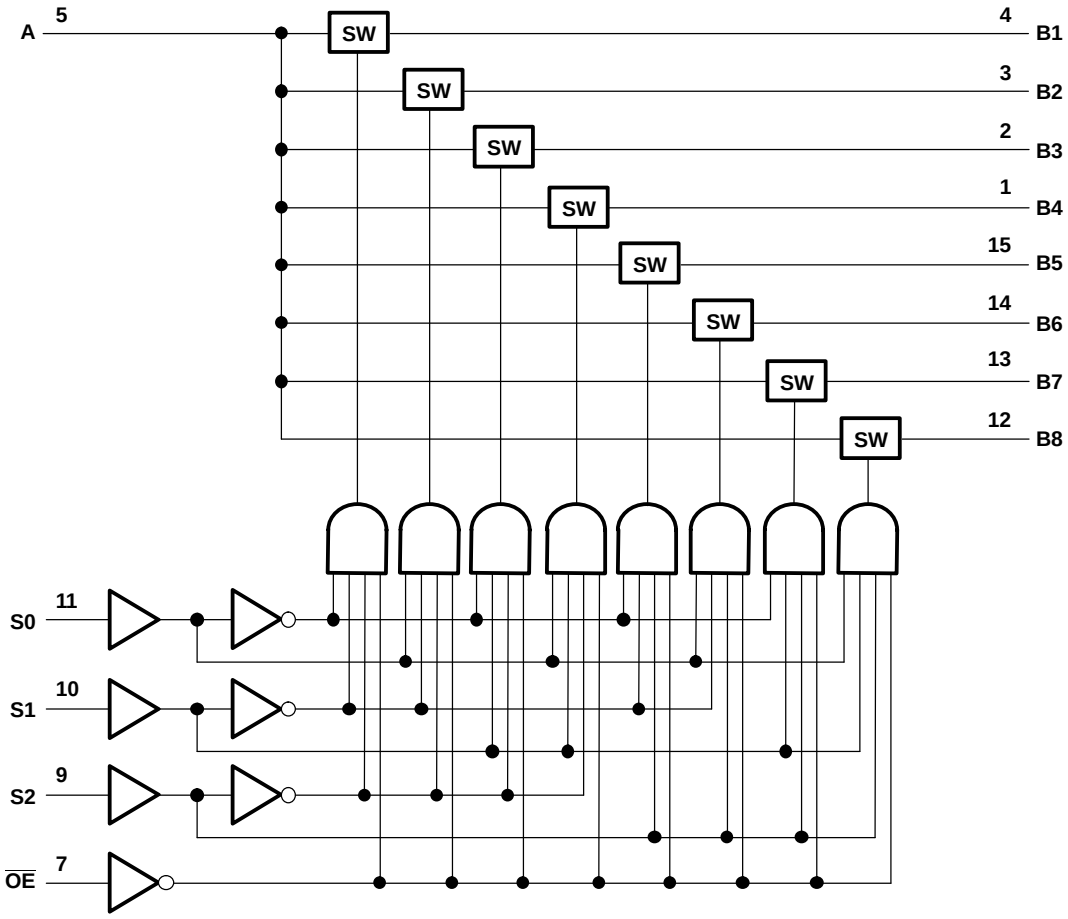
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CB3Q3251RGYR	BU251
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3251DBQR	BU251
	TSSOP – PW	Tube	SN74CB3Q3251PW	BU251
		Tape and reel	SN74CB3Q3251PWR	
	TVSOP – DGV	Tape and reel	SN74CB3Q3251DGVR	BU251

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

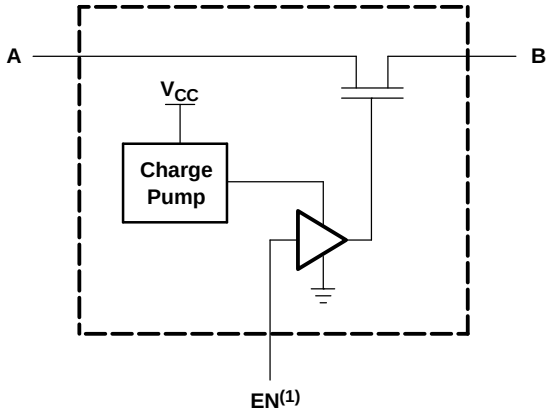
FUNCTION TABLE

INPUTS				INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S2	S1	S0		
L	L	L	L	B1	A port = B1 port
L	L	L	H	B2	A port = B2 port
L	L	H	L	B3	A port = B3 port
L	L	H	H	B4	A port = B4 port
L	H	L	L	B5	A port = B5 port
L	H	L	H	B6	A port = B6 port
L	H	H	L	B7	A port = B7 port
L	H	H	H	B8	A port = B8 port
H	X	X	X	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	DBQ package(6)		90	°C/W
		DGV package(6)		120	
		PW package(6)		108	
		RGY package(7)		39	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	µA
I_{OZ}(3)		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		1	4	mA
ΔI_{CC}(4)	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD}(5)	Per control input	V_{CC} = 3.6 V,	A and B ports open,	Control input switching at 50% duty cycle		0.03	0.1	mA/ MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	4.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		19.5	25	pF
	B port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	4.5	
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		15	19	pF
r_{on}(6)		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4	10	Ω
			V_I = 1.7 V,	I_O = –15 mA		4.5	11	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		3.5	8	
			V_I = 2.4 V,	I_O = –15 mA		4	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ or f_S(1)	$\overline{OE}$ or S	A or B		10		20	MHz
t_{pd}(2)	A or B	B or A		0.12		0.18	ns
$t_{pd(s)}$	S	A	1.5	6.7	1.5	5.9	ns
t_{en}	S	B	1.5	6.7	1.5	5.9	ns
	$\overline{OE}$	A or B	1.5	6.7	1.5	5.9	
t_{dis}	S	B	0.5	6.1	0.5	6.1	ns
	$\overline{OE}$	A or B	0.5	6.1	0.5	6.1	

(1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

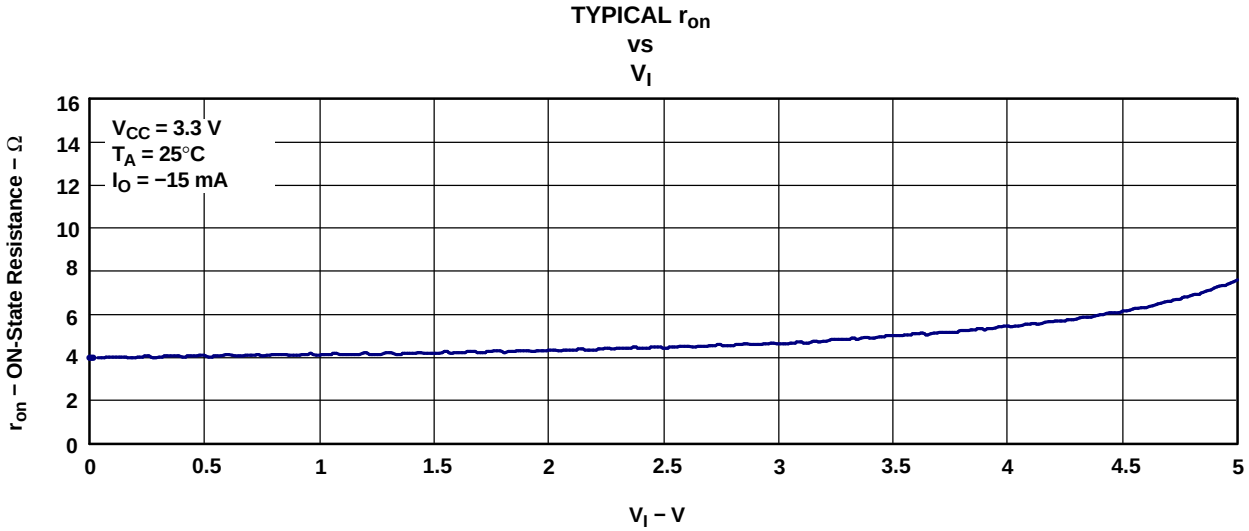


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = –15 mA

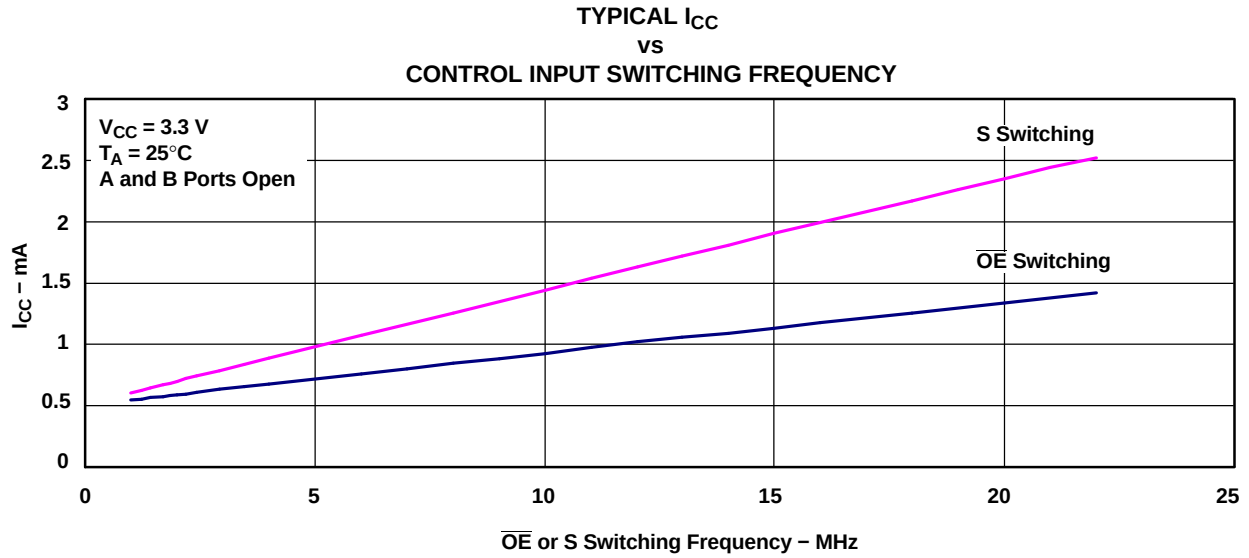
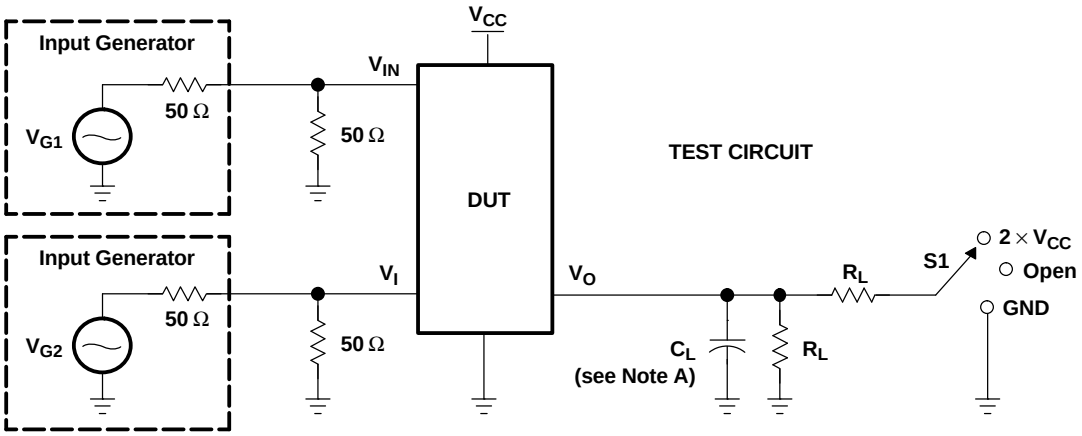
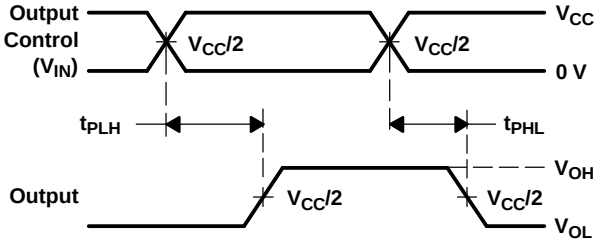


Figure 2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency, V_{CC} = 3.3 V

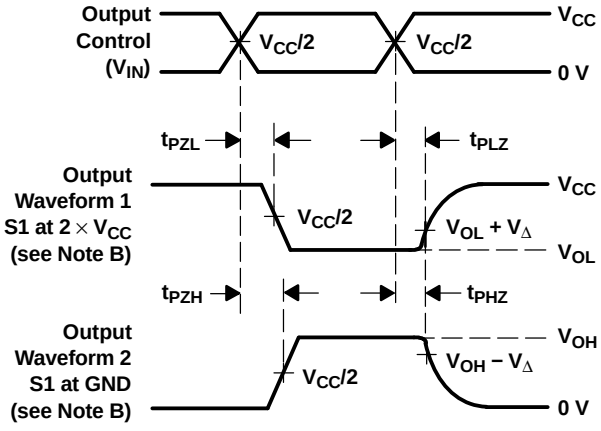
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

THERMAL PAD MECHANICAL DATA

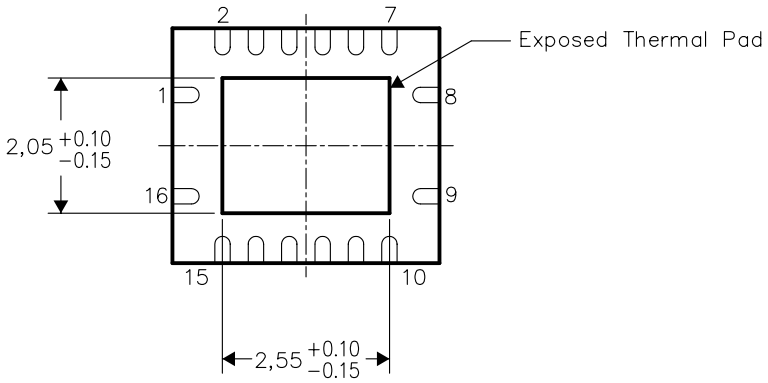
RGY (R–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74CB3Q3251DBQR	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74CB3Q3251DGVR	ACTIVE	TVSOP	DGV	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CB3Q3251PW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CB3Q3251PWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74CB3Q3251RGYR	PREVIEW	QFN	RGY	16	1000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

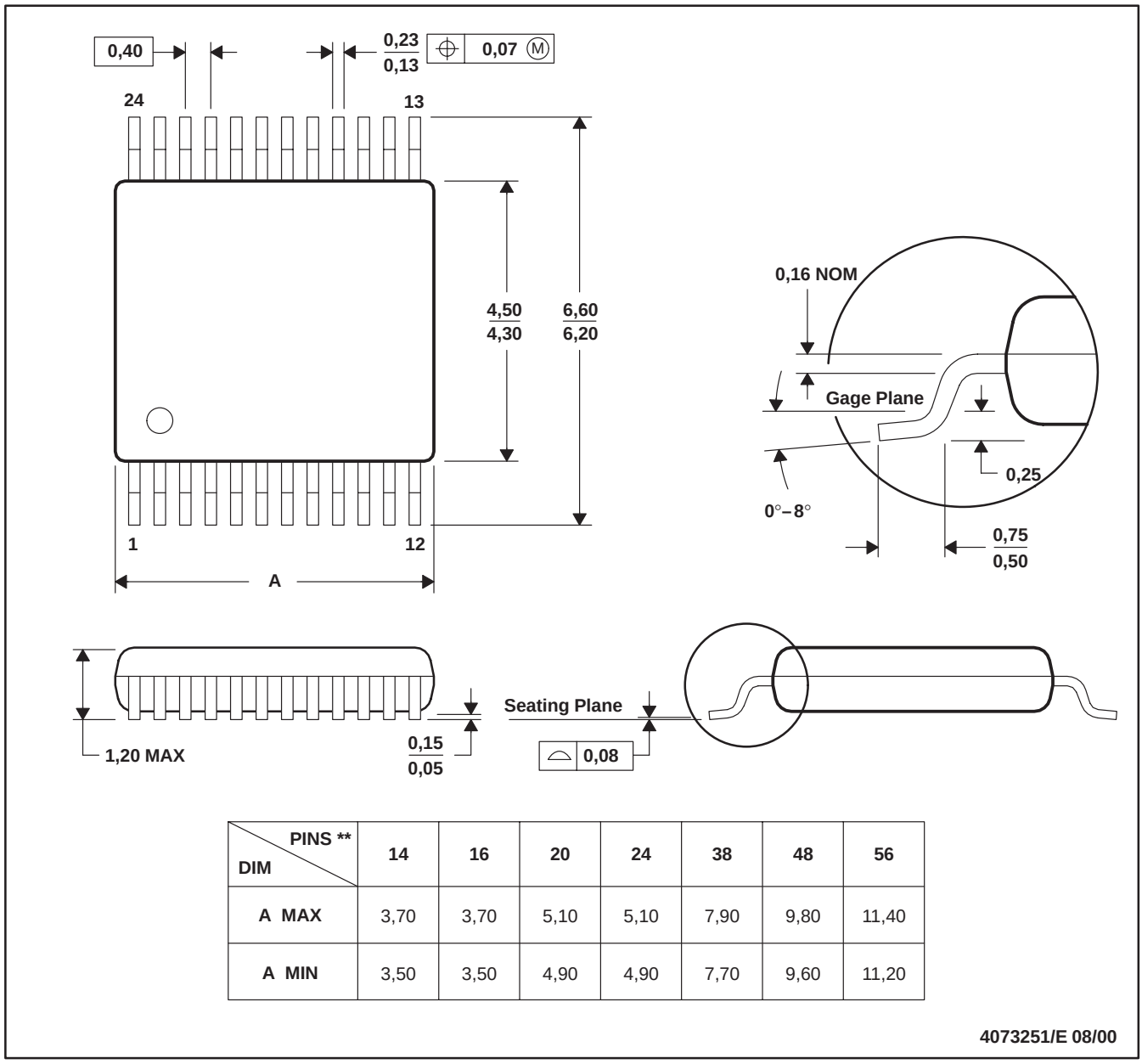
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

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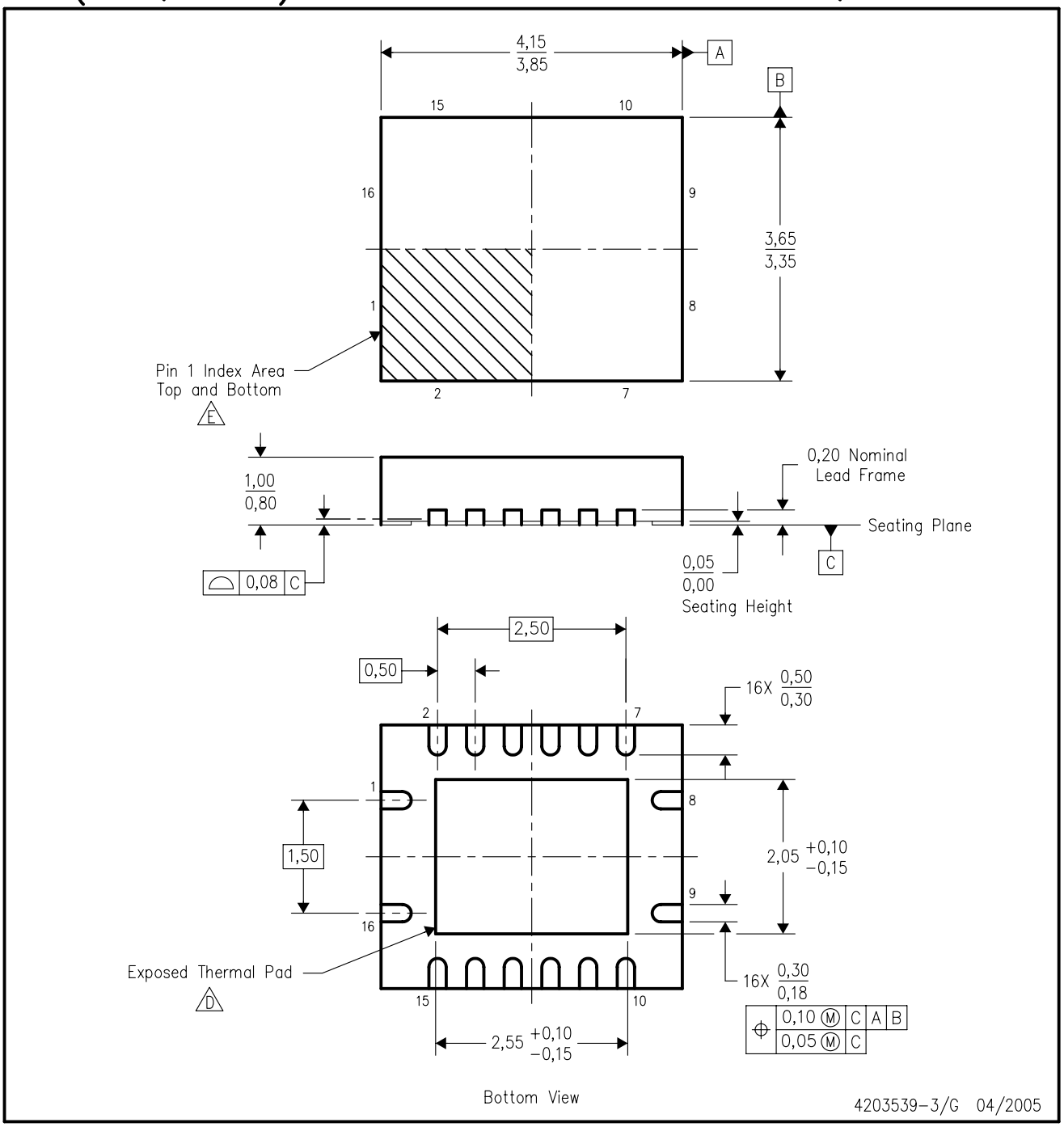
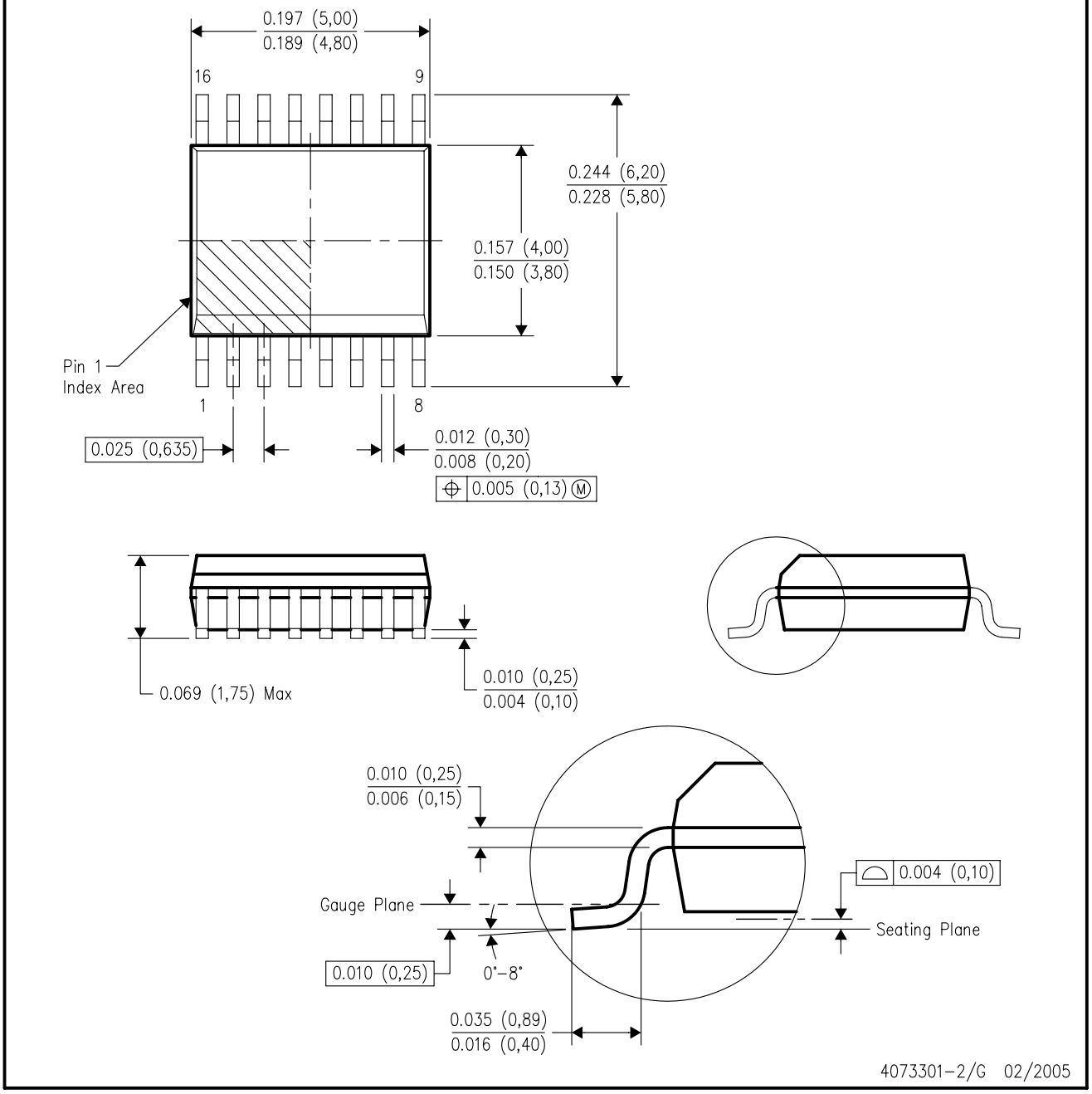
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

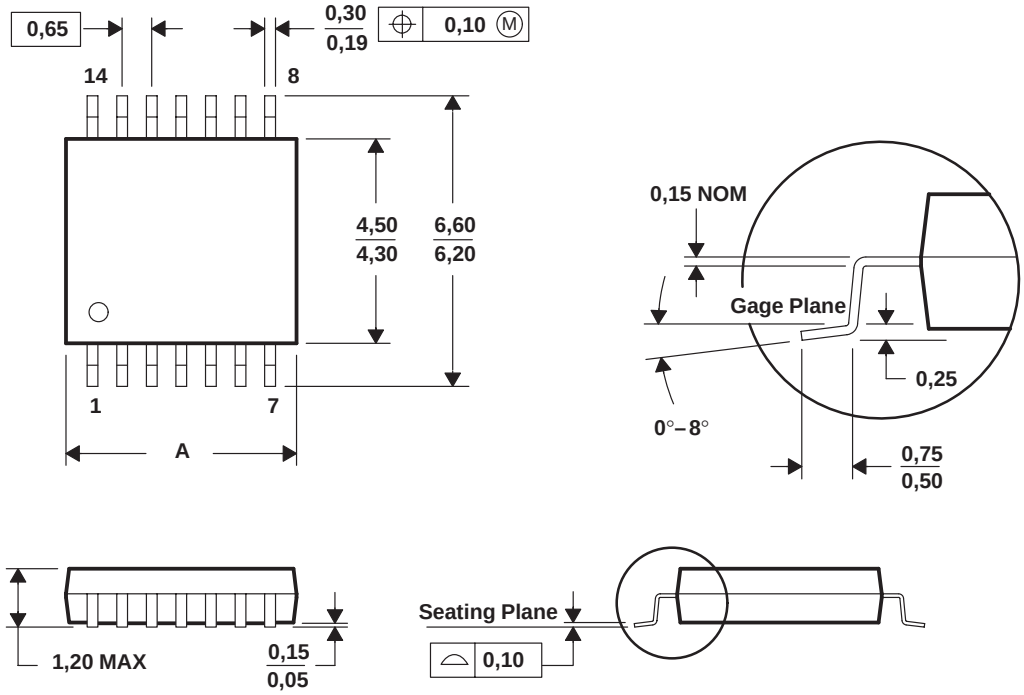
DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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