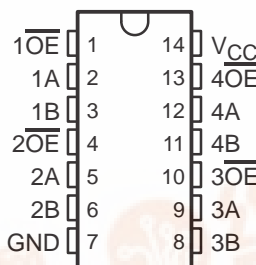


2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
 - 5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V Tolerant I/Os With Device Powered-Up or Powered-Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 5 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading ($C_{iO(OFF)} = 4.5 \text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 20 \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, USB Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

DGV OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3125 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tube	SN74CB3T3125PW	KS125
		Tape and reel	SN74CB3T3125PWR	
	TVSOP – DGV	Tape and reel	SN74CB3T3125DGVR	KS125

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

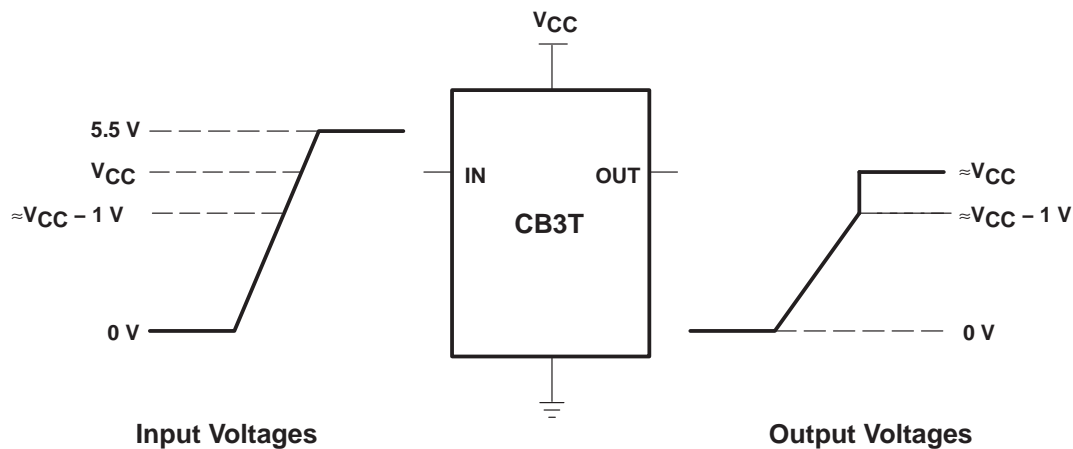
SN74CB3T3125

QUADRUPLE FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1\text{ V}$, and less than or equal to 5.5 V , then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

The SN74CB3T3125 is organized as four 1-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When \overline{OE} is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

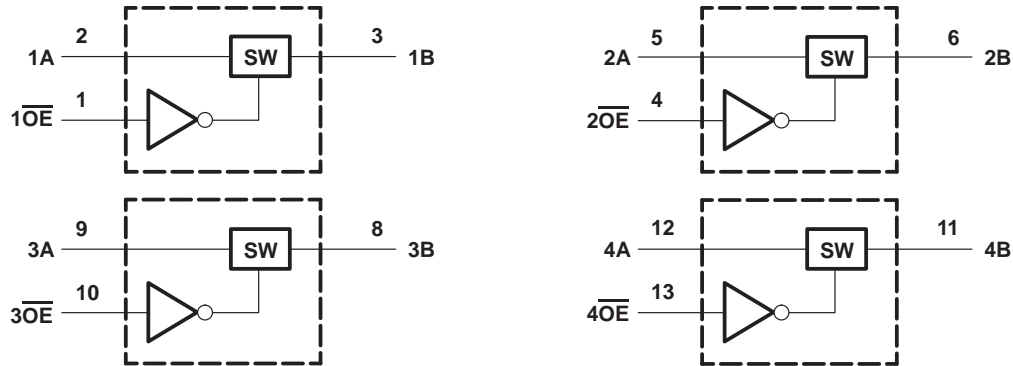
FUNCTION TABLE
(each bus switch)

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

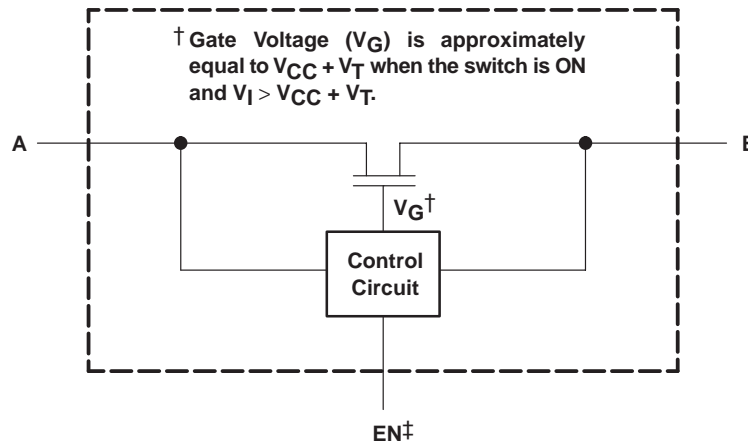
SN74CB3T3125
QUADRUPLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DGV package	127°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74CB3T3125

QUADRUPLE FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V _{CC} = 2.7 V to 3.6 V	2	5.5	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
V _{I/O}	Data input/output voltage		0	5.5	V
T _A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74CB3T3125
QUADRUPLER FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V _{IK}		V _{CC} = 3 V, I _I = −18 mA				−1.2	V	
V _{OH}		See Figures 3 and 4						
I _{IN}	Control inputs	V _{CC} = 3.6 V, V _{IN} = 3.6 V to 5.5 V or GND				±10	μA	
I _I		V _{CC} = 3.6 V, Switch ON, V _{IN} = V _{CC} or GND	V _I = V _{CC} − 0.7 V to 5.5 V			±20	μA	
			V _I = 0.7 V to V _{CC} − 0.7 V			−40		
			V _I = 0 to 0.7 V			±5		
I _{OZ} ‡		V _{CC} = 3.6 V, V _O = 0 to 5.5 V, V _I = 0, Switch OFF, V _{IN} = V _{CC} or GND				±10	μA	
I _{off}		V _{CC} = 0, V _O = 0 to 5.5 V, V _I = 0,				10	μA	
I _{CC}		V _{CC} = 3.6 V, I _{I/O} = 0, Switch ON or OFF, V _{IN} = V _{CC} or GND	V _I = V _{CC} or GND			20	μA	
			V _I = 5.5 V			20		
ΔI _{CC} §	Control inputs	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND				300	μA	
C _{in}	Control inputs	V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND				3	pF	
C _{io} (OFF)		V _{CC} = 3.3 V, V _{I/O} = 5.5 V, 3.3 V, or GND, Switch OFF, V _{IN} = V _{CC} or GND				4.5	pF	
C _{io} (ON)		V _{CC} = 3.3 V, Switch ON, V _{IN} = V _{CC} or GND	V _{I/O} = 5.5 V or 3.3 V			4	pF	
			V _{I/O} = GND			10		
r _{on} ¶		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V, V _I = 0	I _O = 24 mA			5	8	Ω
			I _O = 16 mA			5	8	
		V _{CC} = 3 V, V _I = 0	I _O = 64 mA			5	7	
			I _O = 32 mA			5	7	

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CB3T3125
QUADRUPLE FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

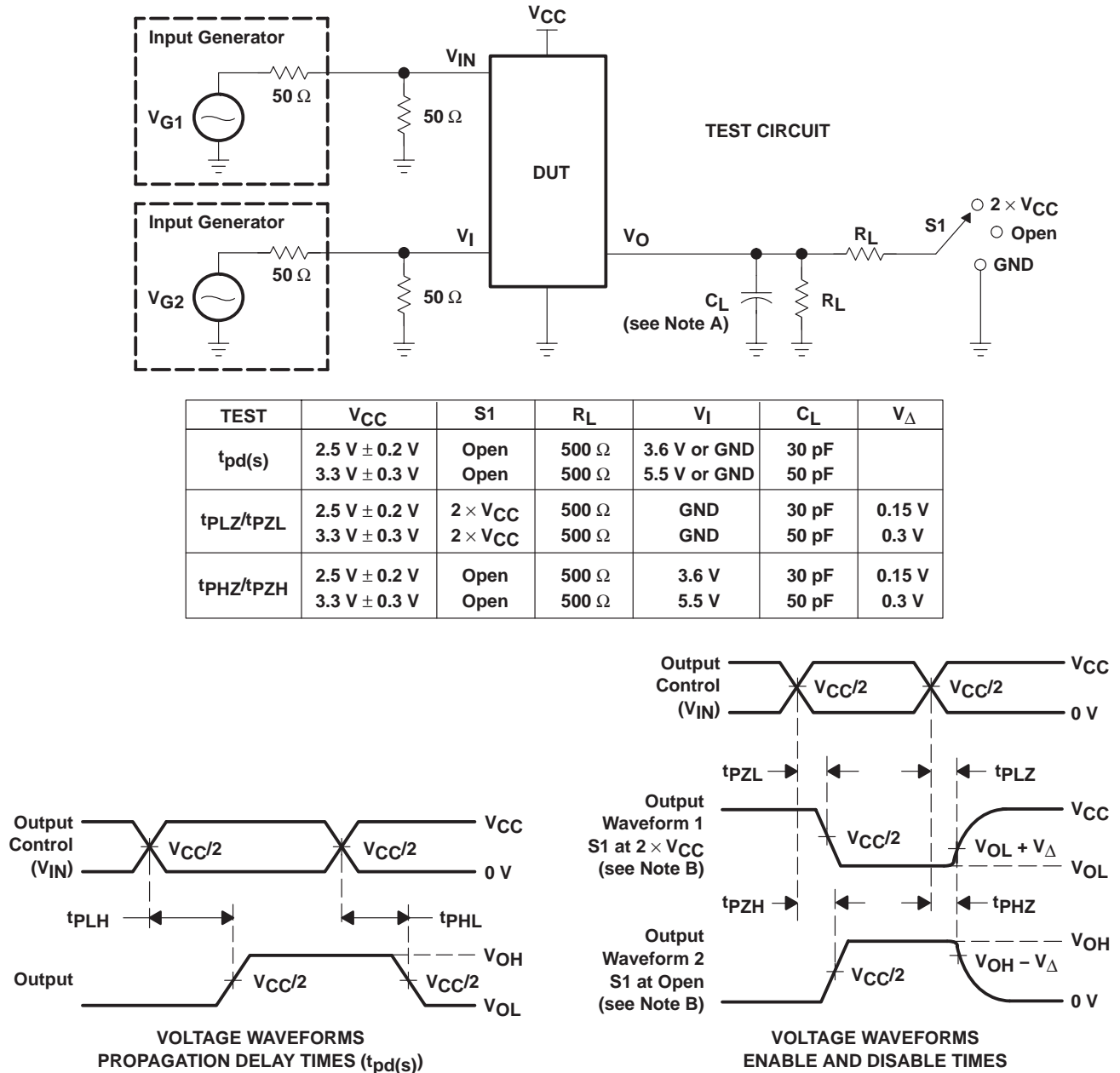
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A		0.15		0.25	ns
t _{en}	$\overline{\text{OE}}$	A or B	1	8.5	1	4.4	ns
t _{dis}	$\overline{\text{OE}}$	A or B	1	9	1	9	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CB3T3125
QUADRUPL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER
SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- B. C_L includes probe and jig capacitance.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - E. The outputs are measured one at a time with one transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - G. t_{PZL} and t_{PZH} are the same as t_{en}.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - I. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

SN74CB3T3125

QUADRUPLE FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

TYPICAL CHARACTERISTICS

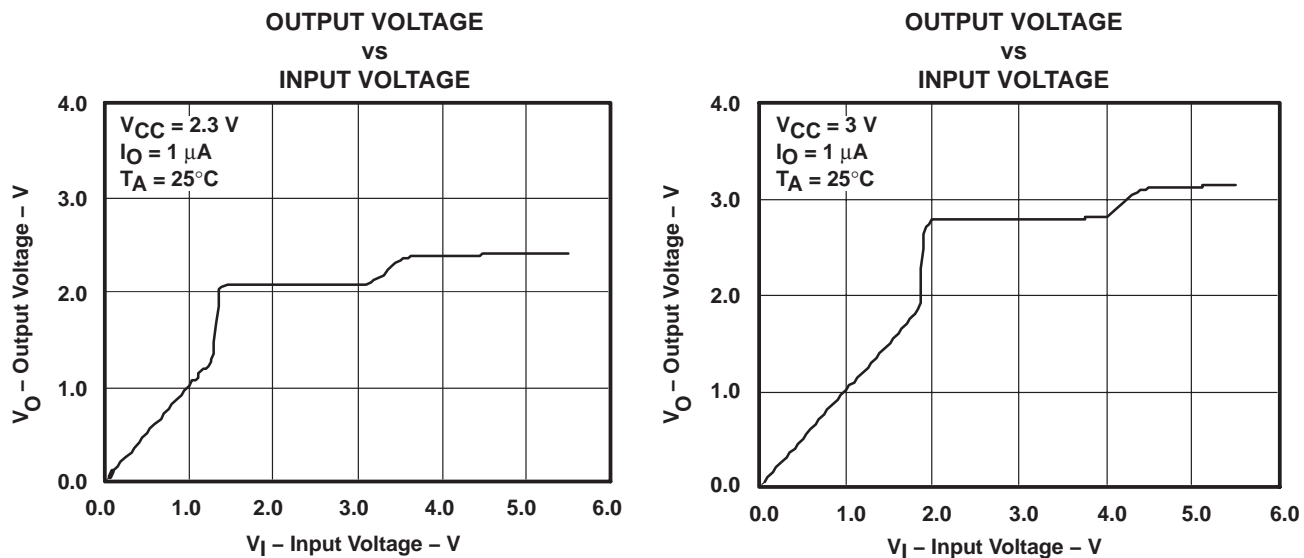


Figure 3. Data Output Voltage vs Data Input Voltage

SN74CB3T3125
QUADRUPLER FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER
SCDS120A – FEBRUARY 2003 – REVISED OCTOBER 2003

TYPICAL CHARACTERISTICS (continued)

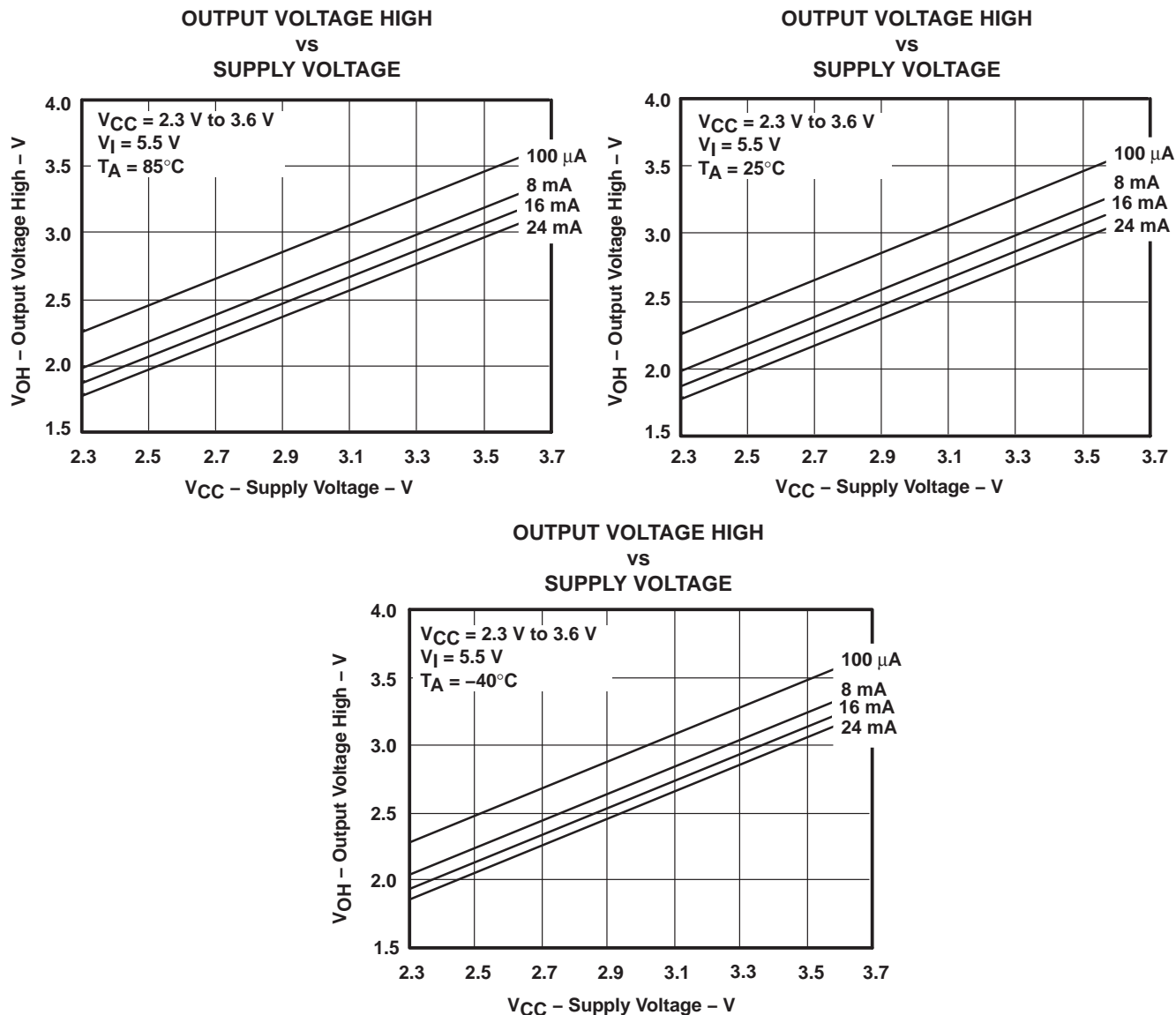


Figure 4. V_{OH} Values

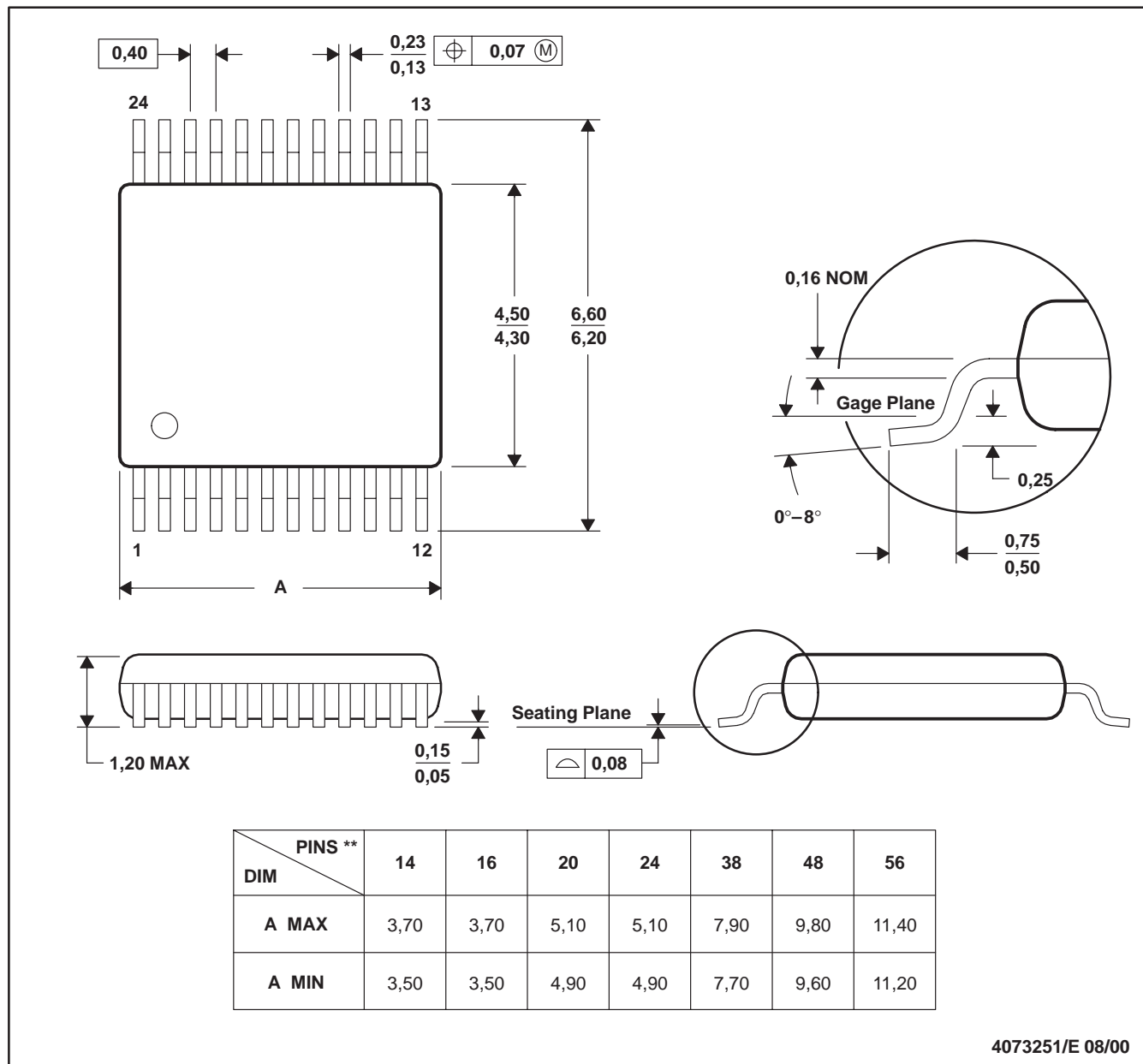
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

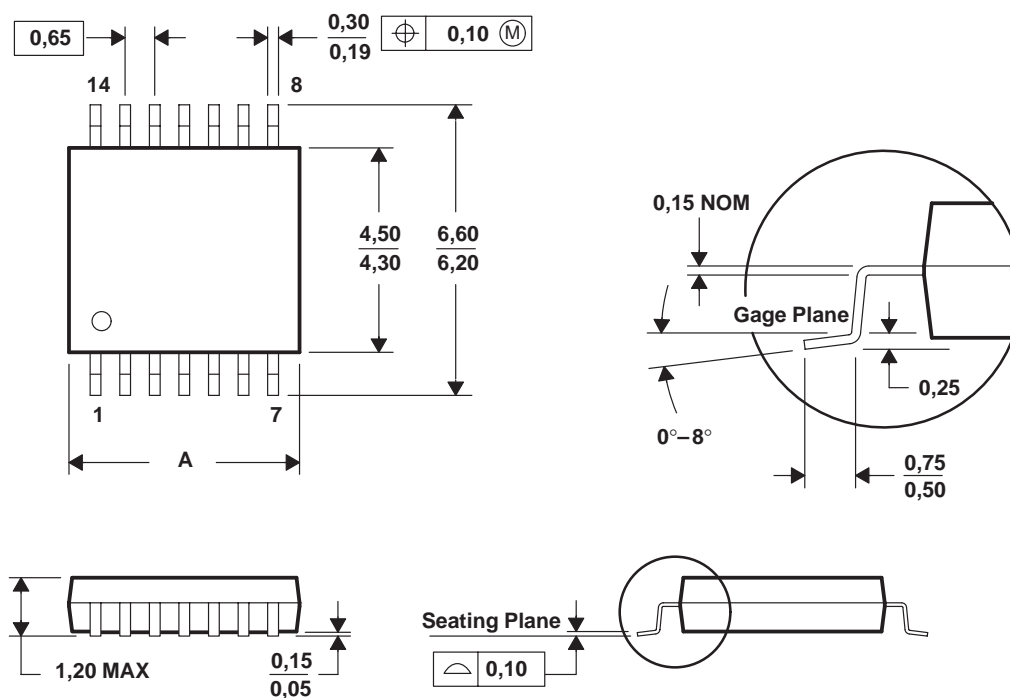
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G^{})**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265