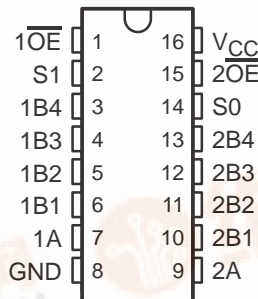


# DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER 2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

SCDS148 – OCTOBER 2003

- Output Voltage Translation Tracks  $V_{CC}$
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
  - 5-V Input Down To 3.3-V Output Level Shift With 3.3-V  $V_{CC}$
  - 5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V  $V_{CC}$
- 5-V Tolerant I/Os With Device Powered-Up or Powered-Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 5\ \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading ( $C_{iO(Off)} = 5\text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 20\ \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, USB Interface, Memory Interleaving, Bus Isolation
- Ideal for Low-Power Portable Equipment

D, DBQ, DGV, OR PW PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74CB3T3253 is a high-speed TTL-compatible FET multiplexer/demultiplexer with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks  $V_{CC}$ . The SN74CB3T3253 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T3253 is organized as two 1-of-4 multiplexer/demultiplexers with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When  $\overline{OE}$  is low, the associated multiplexer/demultiplexer is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated multiplexer/demultiplexer is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

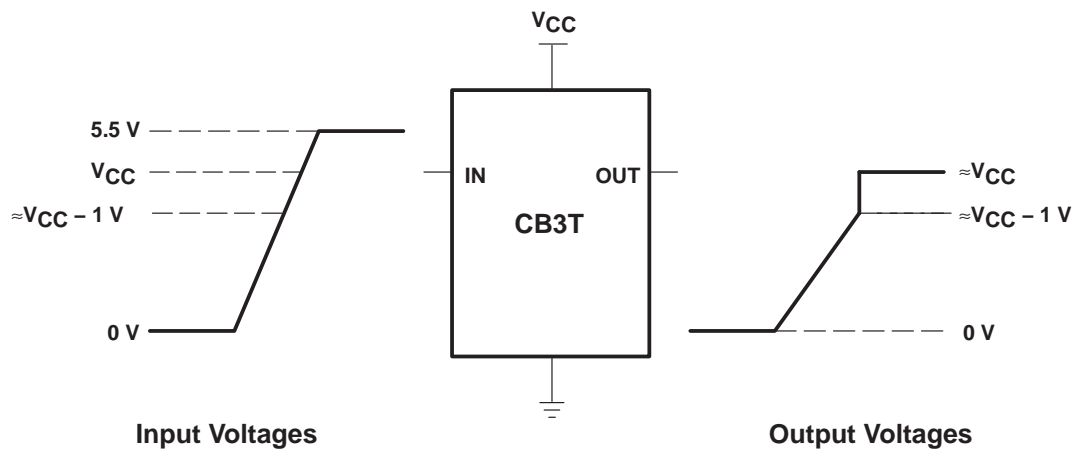
SN74CB3T3253

DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER

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description/ordering information (continued)



NOTE A: If the input high voltage ( $V_{IH}$ ) level is greater than or equal to  $V_{CC} - 1\text{ V}$ , and less than or equal to  $5.5\text{ V}$ , then the output high voltage ( $V_{OH}$ ) level will be equal to approximately the  $V_{CC}$  voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74CB3T3253D	CB3T3253
		Tape and reel	SN74CB3T3253DR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3T3253DBQR	KS253
		Tube	SN74CB3T3253PW	KS253
	TSSOP – PW	Tape and reel	SN74CB3T3253PWR	
	TVSOP – DGV	Tape and reel	SN74CB3T3253DGVR	KS253

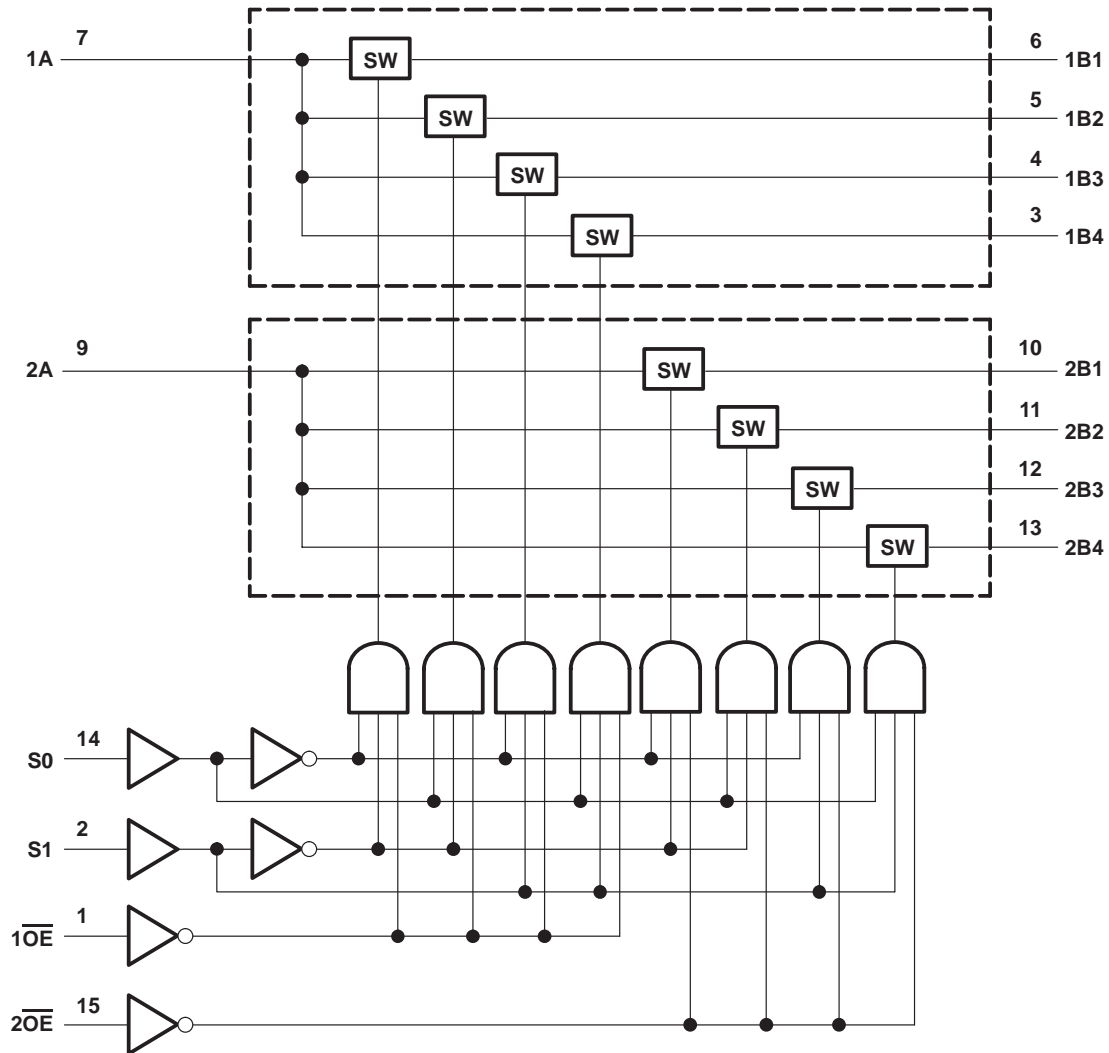
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each multiplexer/demultiplexer)

INPUTS			INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

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logic diagram (positive logic)



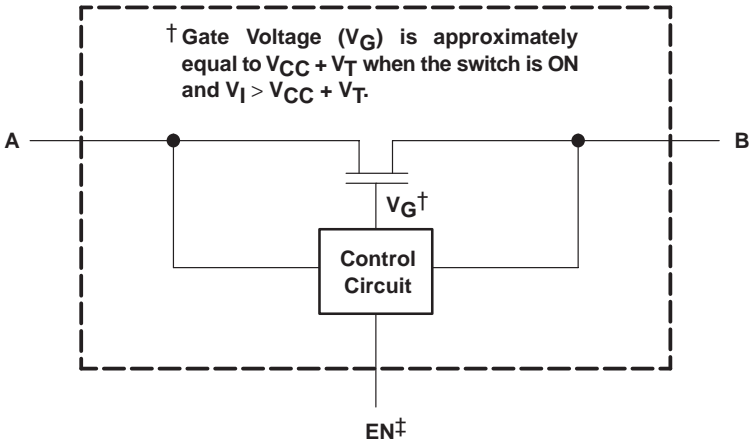
SN74CB3T3253

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simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through $V_{CC}$ or GND terminals	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package	73°C/W
DBQ package	90°C/W
DGV package	120°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2.3	3.6	V
$V_{IH}$	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	5.5	
$V_{IL}$	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
$T_A$	Operating free-air temperature		–40	85	°C

NOTE 6: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IK</sub>		V <sub>CC</sub> = 3 V, I <sub>I</sub> = −18 mA				−1.2	V	
V <sub>OH</sub>		See Figures 3 and 4						
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = 3.6 V to 5.5 V or GND				±10	μA	
I <sub>I</sub>		V <sub>CC</sub> = 3.6 V, Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND	V <sub>I</sub> = V <sub>CC</sub> − 0.7 V to 5.5 V			±20	μA	
			V <sub>I</sub> = 0.7 V to V <sub>CC</sub> − 0.7 V			−40		
			V <sub>I</sub> = 0 to 0.7 V			±5		
I <sub>OZ</sub> ‡		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND				±10	μA	
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0,				10	μA	
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>I/O</sub> = 0, Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND	V <sub>I</sub> = V <sub>CC</sub> or GND			20	μA	
			V <sub>I</sub> = 5.5 V			20		
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND				300	μA	
C <sub>in</sub>	Control inputs	V <sub>CC</sub> = 3.3 V, V <sub>IN</sub> = V <sub>CC</sub> or GND				3	pF	
C <sub>io</sub> (OFF)	A port	V <sub>CC</sub> = 3.3 V, V <sub>I/O</sub> = 5.5 V, 3.3 V, or GND, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND				12	pF	
	B port					5		
C <sub>io</sub> (ON)	A port	V <sub>CC</sub> = 3.3 V, Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND	V <sub>I/O</sub> = 5.5 V or 3.3 V			10	pF	
			V <sub>I/O</sub> = GND			22		
	B port		V <sub>I/O</sub> = 5.5 V or 3.3 V			4		
			V <sub>I/O</sub> = GND			22		
r <sub>on</sub> ¶		V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V, V <sub>I</sub> = 0	I <sub>O</sub> = 24 mA			5	8	Ω
			I <sub>O</sub> = 16 mA			5	8	
		V <sub>CC</sub> = 3 V, V <sub>I</sub> = 0	I <sub>O</sub> = 64 mA			5	7	
			I <sub>O</sub> = 32 mA			5	7	

$V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

† All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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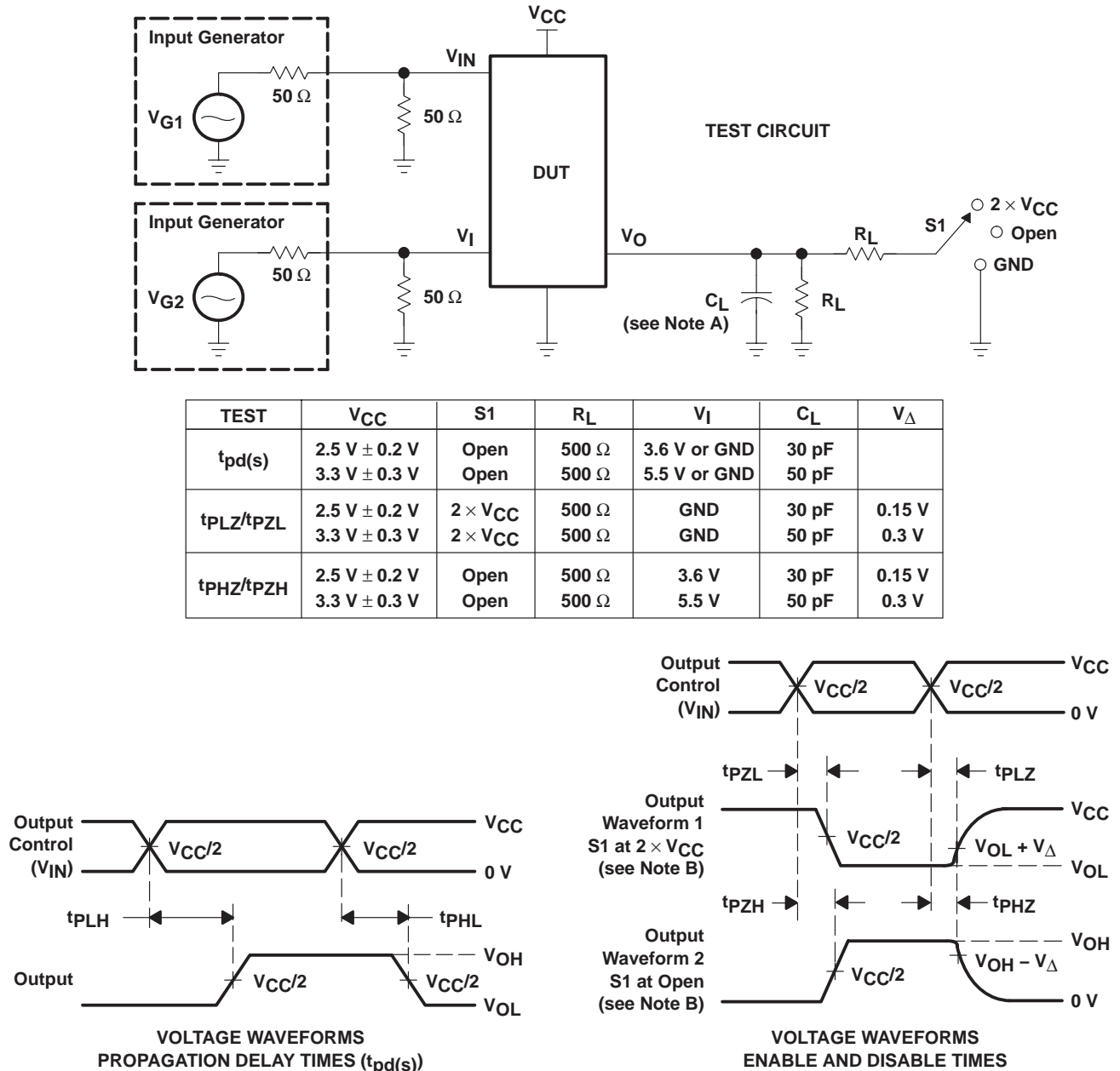
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>†</sup>	A or B	B or A		0.15		0.25	ns
t <sub>pd(s)</sub>	S	A	1	10.5	1	8	ns
t <sub>en</sub>	S	B	1	10	1	8	ns
	$\overline{\text{OE}}$	A or B	1	8.5	1	8	
t <sub>dis</sub>	S	B	1	7.5	1	8.5	ns
	$\overline{\text{OE}}$	A or B	1	6.5	1	8	

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- B.  $C_L$  includes probe and jig capacitance.
  - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - D. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - E. The outputs are measured one at a time with one transition per measurement.
  - F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}(s)$ . The  $t_{pd}$  propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - I. All parameters and waveforms are not applicable to all devices.

**Figure 2. Test Circuit and Voltage Waveforms**

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TYPICAL CHARACTERISTICS

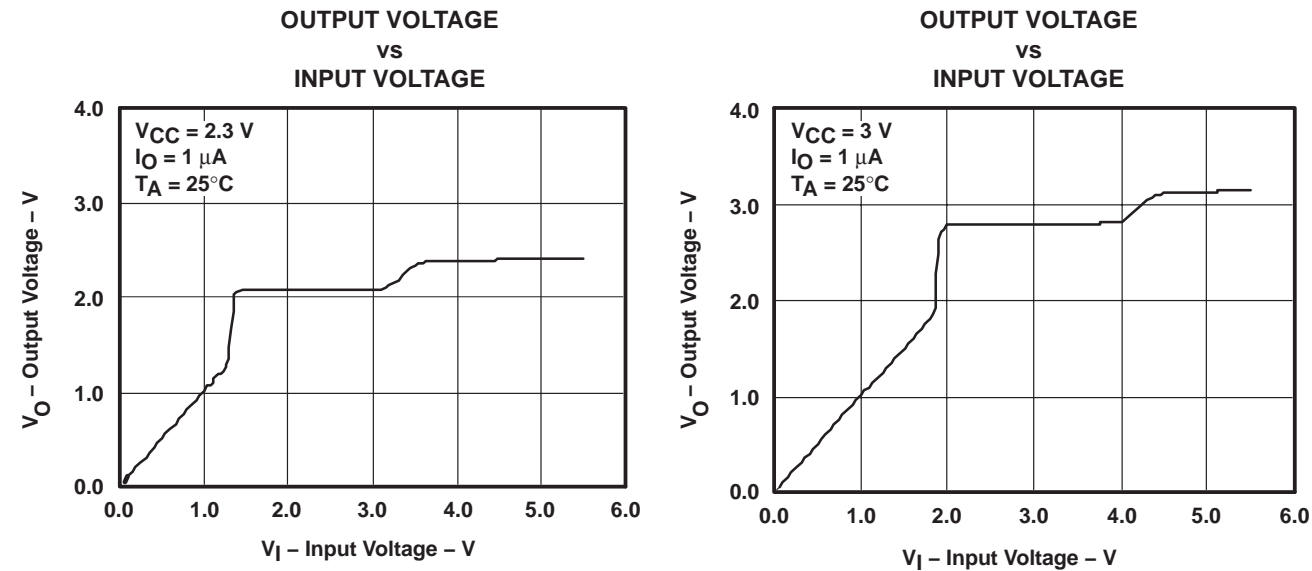


Figure 3. Data Output Voltage vs Data Input Voltage



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**TYPICAL CHARACTERISTICS (continued)**

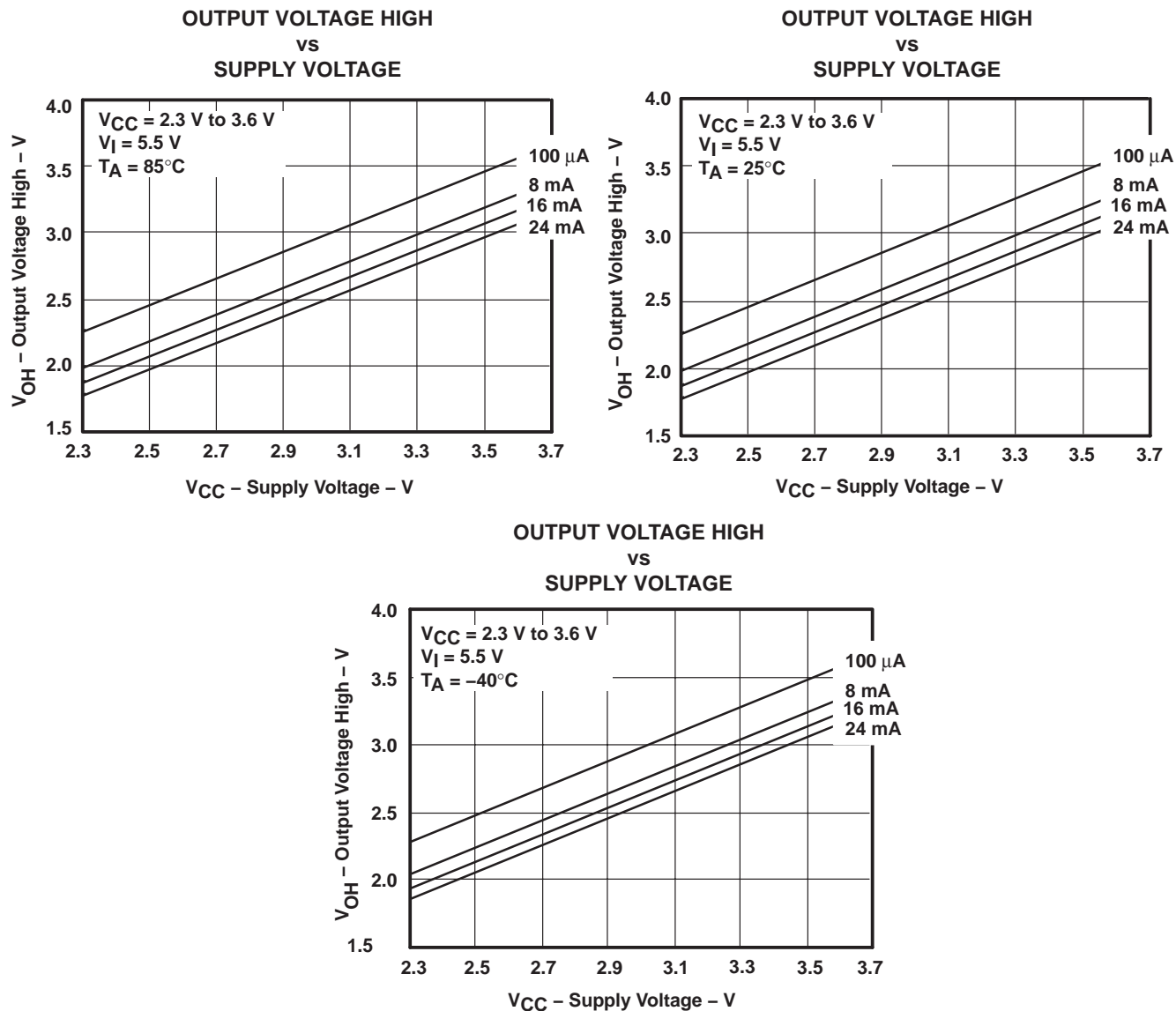


Figure 4.  $V_{OH}$  Values

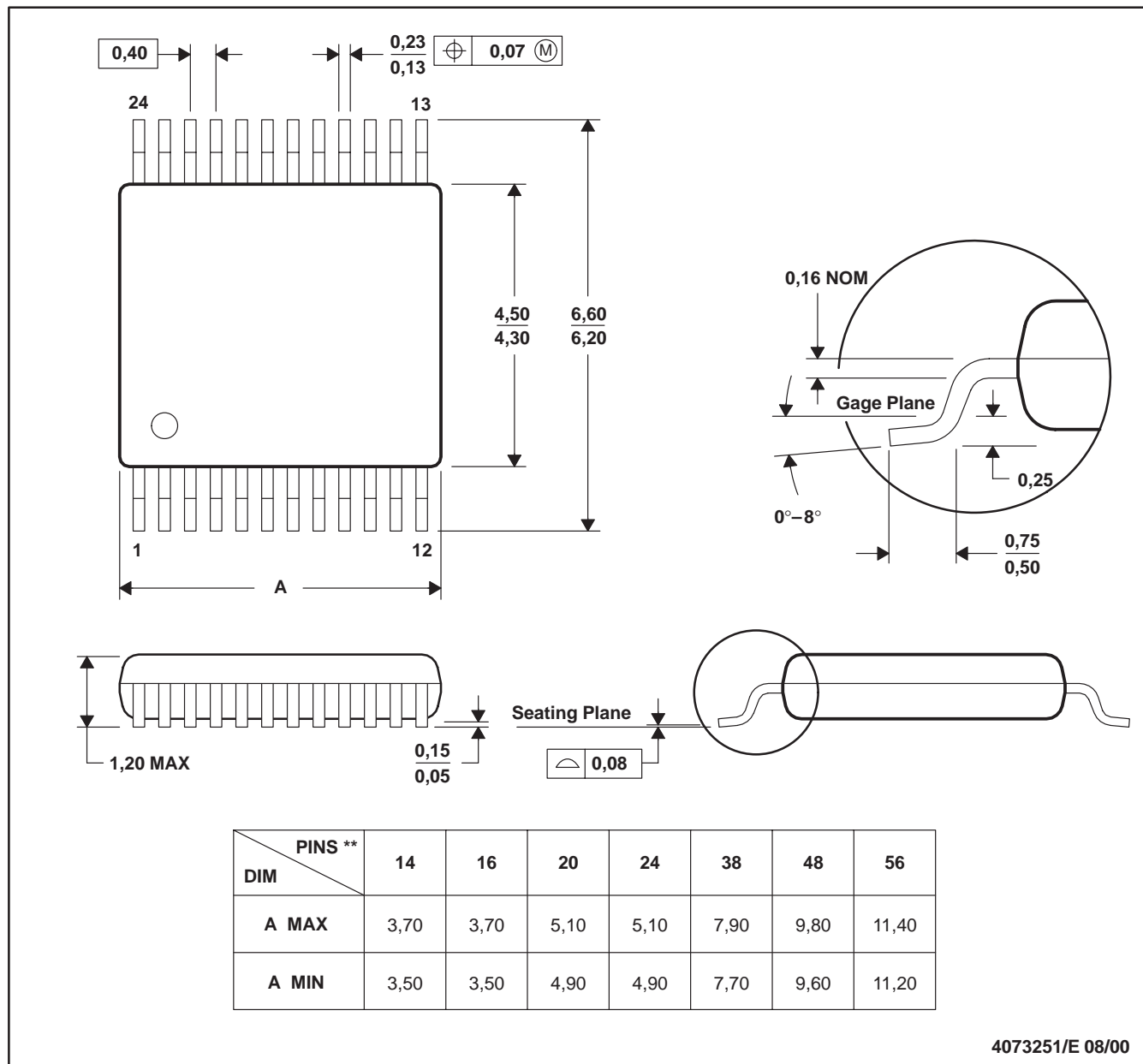
# MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

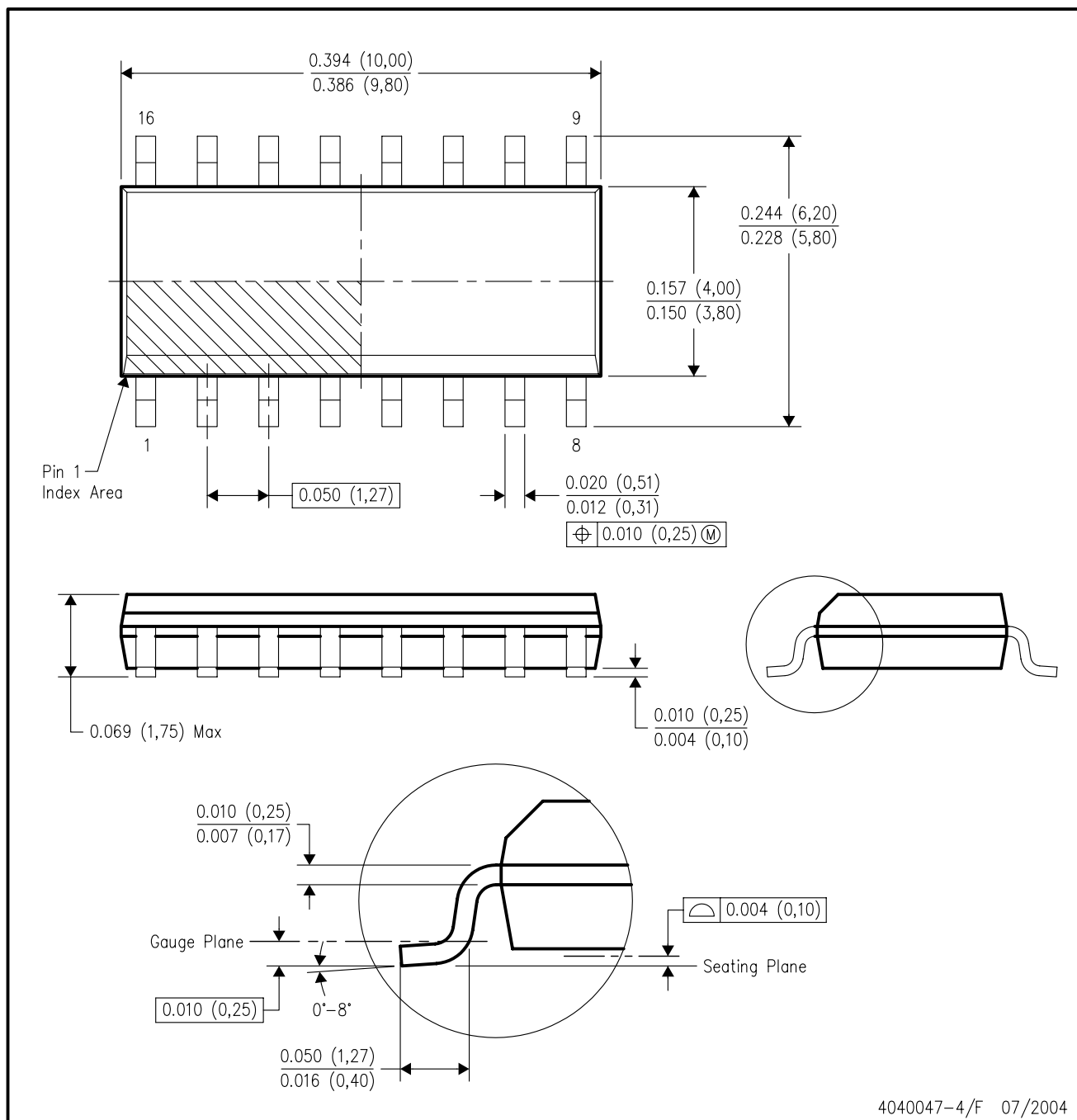


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# MECHANICAL DATA

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

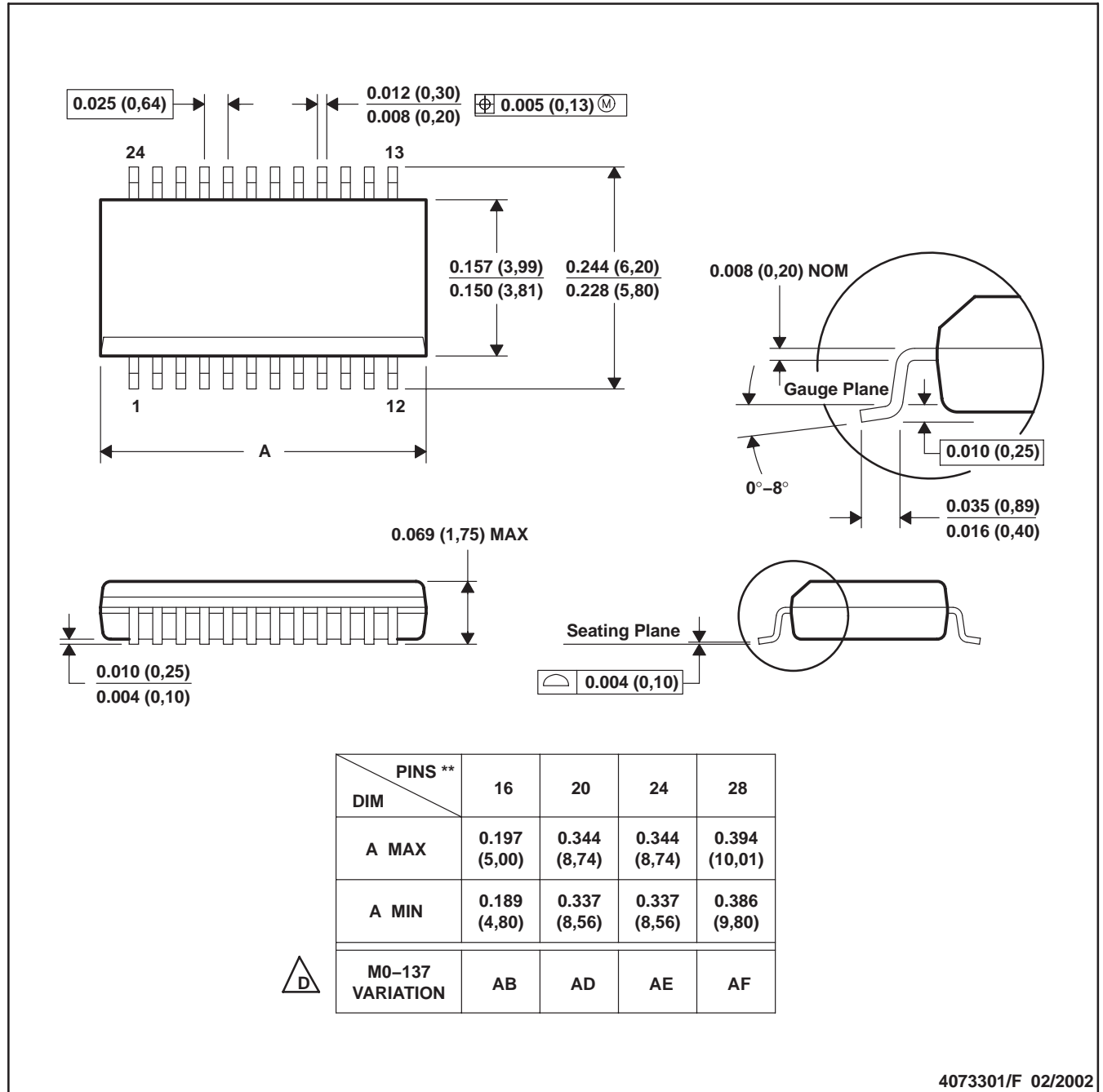
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

# MECHANICAL DATA

MSOI004E JANUARY 1995 – REVISED MAY 2002

DBQ (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-137.

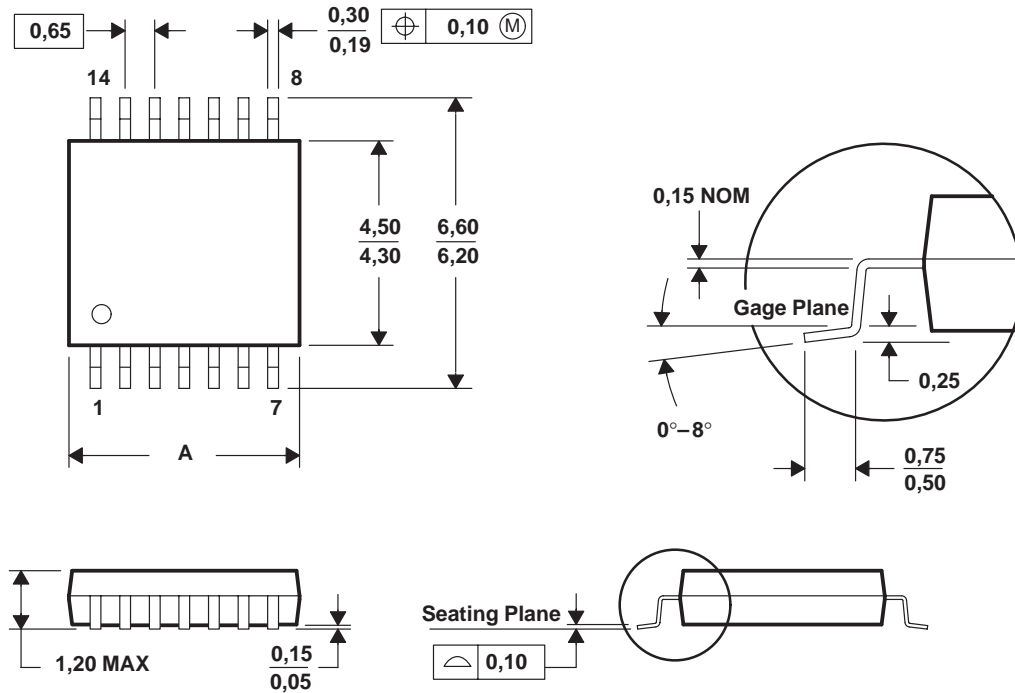
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

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