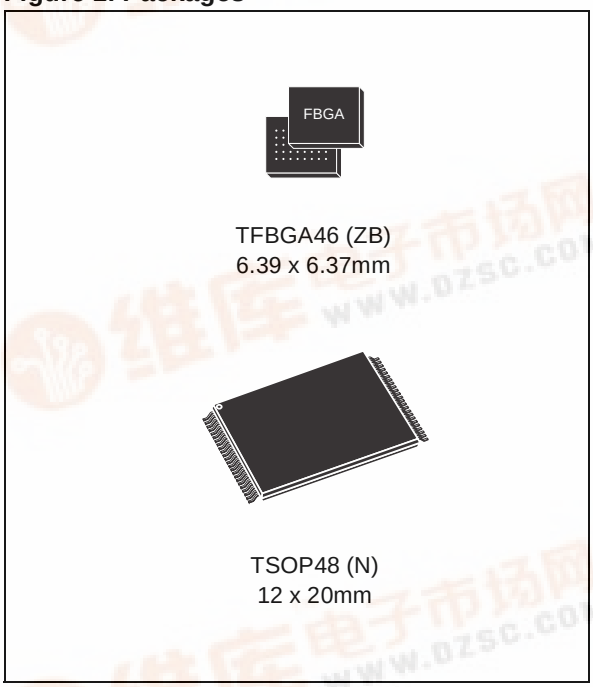
M28W800BT
M28W800BB

8 Mbit (512Kb x16, Boot Block) 3V Supply Flash Memory

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 2.7V to 3.6V Core Power Supply
  - V_{DDQ}= 1.65V to 3.6V for Input/Output
  - V_{PP} = 12V for fast Program (optional)
- ACCESS TIME: 70, 85, 90,100ns
- PROGRAMMING TIME
  - 10µs typical
  - Double Word Programming Option
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- MEMORY BLOCKS
  - Parameter Blocks (Top or Bottom location)
  - Main Blocks
- BLOCK PROTECTION on TWO PARAMETER BLOCKS
  - $\overline{WP}$ for Block Protection
- AUTOMATIC STAND-BY MODE
- PROGRAM and ERASE SUSPEND
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M28W800BT: 8892h
  - Bottom Device Code, M28W800BB: 8893h

Figure 1. Packages



TFBGA46 (ZB)
6.39 x 6.37mm

TSOP48 (N)
12 x 20mm

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SUMMARY DESCRIPTION

The M28W800B is a 8 Mbit (512Kbit x 16) non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a Word-by-Word basis. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. V_{DDQ} allows to drive the I/O pin down to 1.65V. An optional 12V V_{PP} power supply is provided to speed up customer programming.

The device features an asymmetrical blocked architecture. The M28W800B has an array of 23 blocks: 8 Parameter Blocks of 4 KWord and 15 Main Blocks of 32 KWord. M28W800BT has the Parameter Blocks at the top of the memory address space while the M28W800BB locates the Parameter Blocks starting from the bottom. The memory maps are shown in Figure 5, Block Addresses.

Parameter blocks 0 and 1 can be protected from accidental programming or erasure. Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The memory is offered in TSOP48 (10 X 20mm), and TFBGA46 (6.39 x 6.37mm, 0.75mm pitch) packages and is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

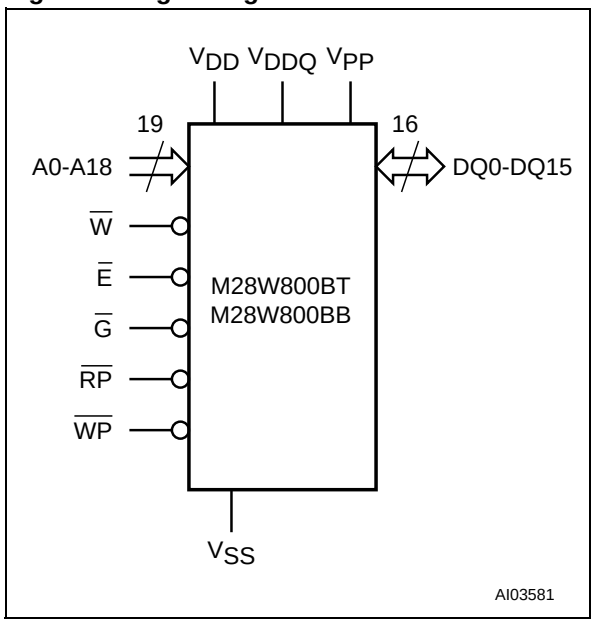


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
$\overline{WP}$	Write Protect
V_{DD}	Core Power Supply
V_{DDQ}	Power Supply for Input/Output
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

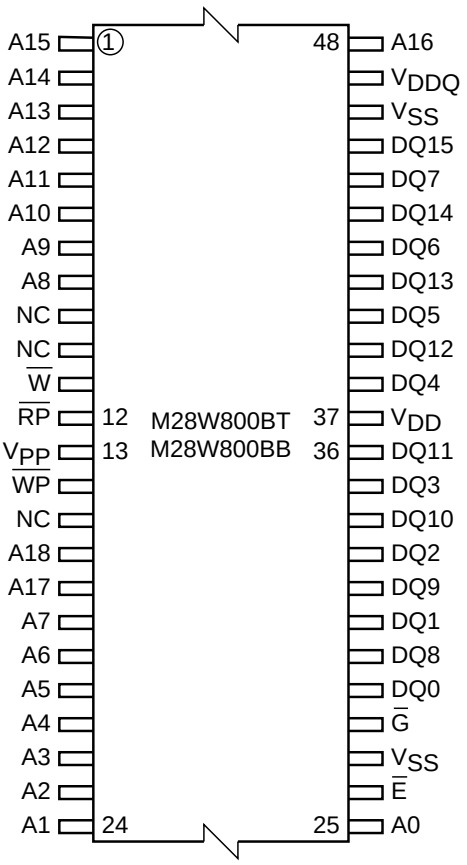


Figure 4. TFBGA Connections (Top view through package)

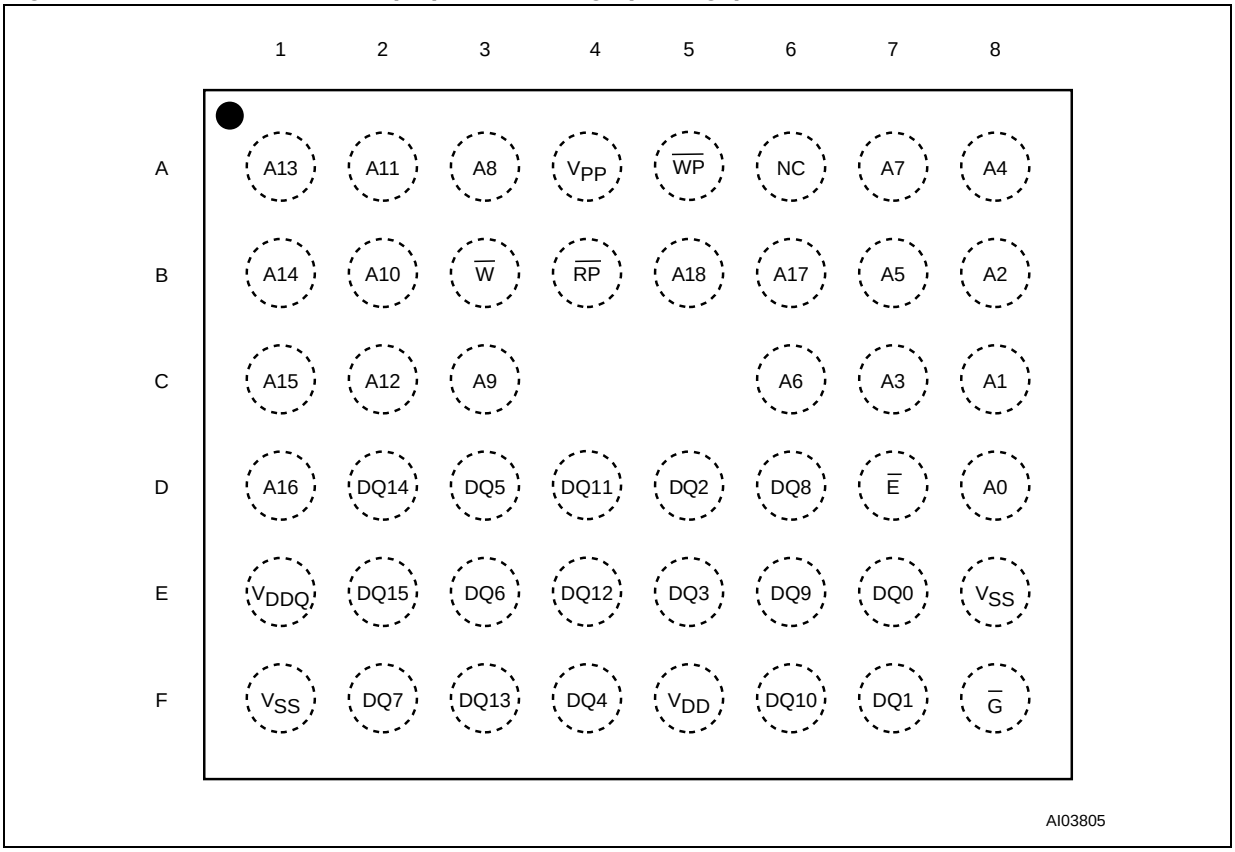
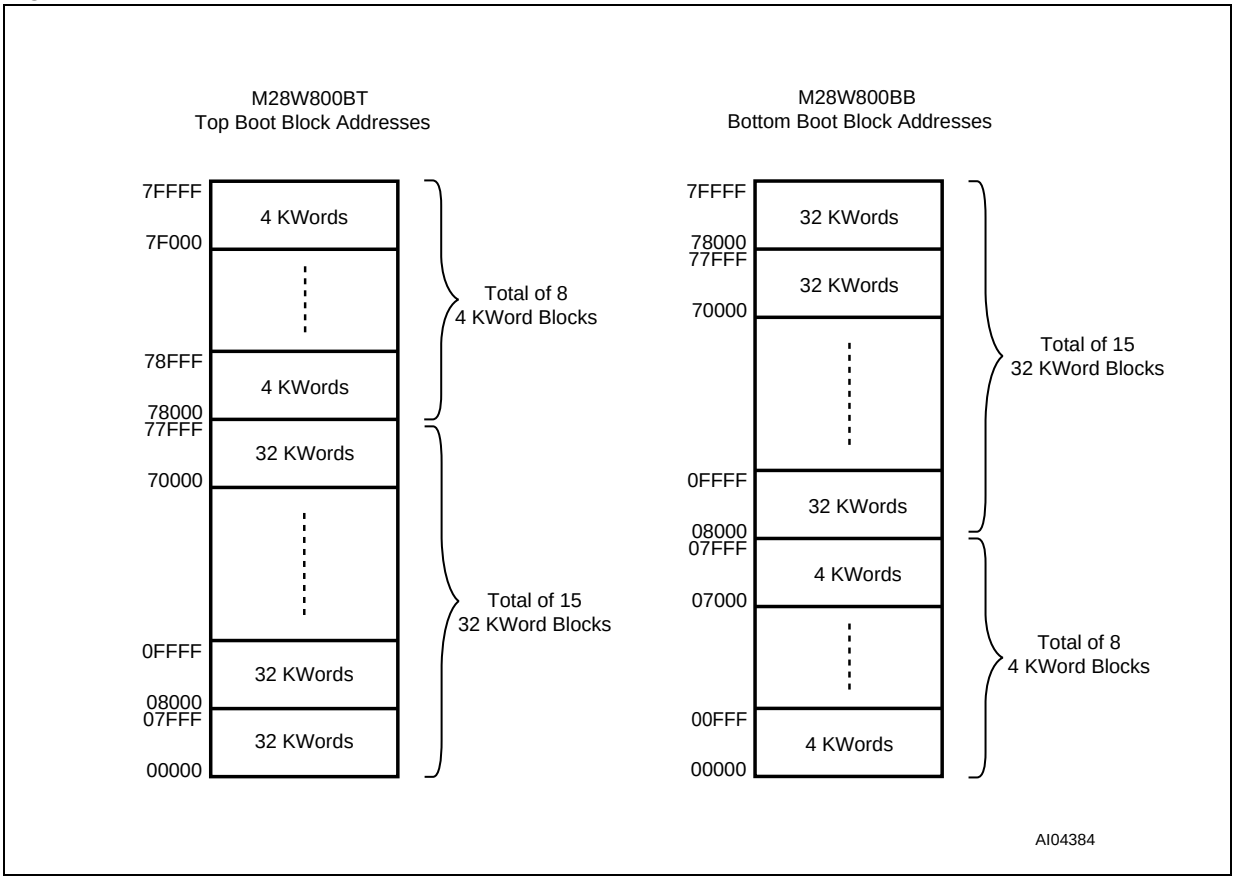


Figure 5. Block Addresses



Note: Also see Appendix A, Tables 21 and 22 for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram and Table 1,Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A18). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or data to be programmed during a Write Bus operation.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

Output Enable ($\overline{G}$). The Output Enable controls data outputs during the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable, E, or Write Enable, W, whichever occurs first.

Write Protect ($\overline{WP}$). Write Protect is an input to protect or unprotect the two lockable parameter blocks. When Write Protect is at V_{IL}, the lockable blocks are protected and Program or Erase operations are not possible. When Write Protect is at V_{IH}, the lockable blocks are unprotected and can be programmed or erased (refer to Table 4, Memory Blocks Protection Truth).

Reset ($\overline{RP}$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is minimized. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters read array mode, but a negative transition of Chip Enable or a change of the address is required to ensure valid data outputs.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

V_{PP} Program Supply Voltage. V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. The Supply Voltage V_{DD} and the Program Supply Voltage V_{PP} can be applied in any order.

If V_{PP} is kept in a low voltage range (0V to 3.6V) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see Table 11, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range 11.4V to 12.6V it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed (see Table 13 and 14).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Note: Each device in a system should have V_{DD},V_{DDQ} and V_{PP} decoupled with a 0.1µF capacitor close to the pin. See Figure 7, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required V_{PP} Program and Erase currents.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Reset. See Table 2, Bus Operations, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Read. Read Bus operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figure 8, Read Mode AC Waveforms, and Table 12, Read AC Characteristics, for details of when the output becomes valid.

Read mode is the default state of the device when exiting Reset or after power-up.

Write. Bus Write operations write Commands to the memory or latch Input Data to be programmed. A write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

See Figures 9 and 10, Write AC Waveforms, and Tables 13 and 14, Write AC Characteristics, for details of the timing requirements.

Output Disable. The data outputs are high impedance when the Output Enable is at V_{IH}.

Standby. Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable is at V_{IH} and the device is in read mode. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Automatic Standby. Automatic Standby provides a low power consumption state during Read mode. Following a read operation, the device enters Automatic Standby after 150ns of bus inactivity, even if Chip Enable is low, V_{IL}, and the supply current is reduced to I_{DD1}. The data Inputs/Outputs will still output data.

Reset. During Reset mode, when Output Enable is low, V_{IL}, the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL}. The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Table 2. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{WP}$	V_{PP}	DQ0-DQ15
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Don't Care	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	V_{DD} or V_{PPH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Don't Care	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	X	Don't Care	Hi-Z
Reset	X	X	X	V_{IL}	X	Don't Care	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PPH} = 12V ± 5%.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time, to monitor the progress of an operation, or the Program/Erase states. See Appendix D, Table 29, Write State Machine Current/Next, for a summary of the Command Interface.

The Command Interface is reset to Read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode. Refer to Table 3, Commands, in conjunction with the text descriptions below.

Read Memory Array command

The Read command returns the memory to its Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent read operations will read the addressed location and output the data. When a device Reset occurs, the memory defaults to Read mode.

Read Status Register Command

The Status Register indicates when a program or erase operation is complete and the success or failure of the operation itself. Issue a Read Status Register command to read the Status Register's contents. Subsequent Bus Read operations read the Status Register, at any address, until another command is issued. See Table 7, Status Register Bits, for details on the definitions of the bits.

The Read Status Register command may be issued at any time, even during a Program/Erase operation. Any Read attempt during a Program/Erase operation will automatically output the content of the Status Register.

Read Electronic Signature Command

The Read Electronic Signature command reads the Manufacturer and Device Codes.

The Read Electronic Signature command consists of one write cycle, a subsequent read will output the Manufacturer or the Device Code depending on the levels of A0. The Manufacturer Code is output when the address line A0 is at V_{IL}, the Device Code is output when A0 is at V_{IH}. Addresses A1-A7 must be kept to V_{IL}, other addresses are ignored. The codes are output on DQ0-DQ7 with DQ8-DQ15 at 00h. (see Table 4)

Read CFI Query Command

The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area, allowing programming equipment or applications to automatically match their interface to the characteristics of the device.

One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Common Flash Interface, Tables 23, 24, 25, 26, 27 and 28 for details on the information contained in the Common Flash Interface memory area.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts.

Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

During Erase operations the memory will only accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 6, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix C, Figure 19, Erase Flowchart and Pseudo Code, for the flowchart for using the Erase command.

Program Command

The memory array can be programmed word-by-word. Two bus write cycles are required to issue the Program command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

During Program operations the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other

commands will be ignored. Typical Program times are given in Table 6, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 16, Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

Double Word Program Command

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel.The two words must differ only for the address A0. Programming should not be attempted when V_{PP} is not at V_{PPH}. The command can be executed if V_{PP} is below V_{PPH} but the result is not guaranteed.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See Appendix C, Figure 17, Double Word Program Flowchart and Pseudo Code, for the flowchart for using the Double Word Program command.

Clear Status Register Command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One bus write cycle is required to issue the Clear Status Register command.

The bits in the Status Register do not automatically return to '0' when a new Program or Erase command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Program or Erase operation. One bus write cycle is required to issue the Program/Erase command and pause the Program/Erase controller.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array, Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Program command will also be accepted. Only the blocks not being erased may be read or programmed correctly.

During a Program/Erase Suspend, the device can be placed in a pseudo-standby mode by taking Chip Enable to V_{IH}. Program/Erase is aborted if Reset turns to V_{IL}.

See Appendix C, Figure 18, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 20, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the command. Once the command is issued subsequent Bus Read operations read the Status Register.

See Appendix C, Figure 18, Program or Double Word Program Suspend & Resume Flowchart and Pseudo Code, and Figure 20, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Resume command.

Block Protection

Two parameter/lockable blocks (blocks #0 and #1) can be protected against Program or Erase operations. Unprotected blocks can be programmed or erased.

To protect the two lockable blocks set Write Protect to V_{IL}. When V_{PP} is below V_{PPLK} all blocks are protected. Any attempt to Program or Erase protected blocks will abort, the data in the block will not be changed and the Status Register outputs the error.

Table 5, Memory Blocks Protection Truth Table**,** defines the protection methods.

Table 3. Commands

Commands	No. of Cycles	Bus Write Operations								
		1st Cycle			2nd Cycle			3nd Cycle		
		Bus Op.	Addr	Data	Bus Op.	Addr	Data	Bus Op.	Addr	Data
Read Memory Array	1+	Write	X	FFh	Read	Read Addr	Data			
Read Status Register	1+	Write	X	70h	Read	X	Status Register			
Read Electronic Signature	1+	Write	X	90h	Read	Signature Addr (2)	Signature			
Read CFI Query	1+	Write	X	98h	Read	CFI Addr	Query			
Erase	2	Write	X	20h	Write	Block Addr	D0h			
Program	2	Write	X	40h or 10h	Write	Addr	Data Input			
Double Word Program(3)	3	Write	X	30h	Write	Addr 1	Data Input	Write	Addr 2	Data Input
Clear Status Register	1	Write	X	50h						
Program/Erase Suspend	1	Write	X	B0h						
Program/Erase Resume	1	Write	X	D0h						

Note: 1. X = Don't Care.
2. A0=V_{IL} outputs Manufacturer code, A0=V_{IH} outputs Device code. Address A7-A1 must be V_{IL}.
3. Addr 1 and Addr 2 must be consecutive Addresses differing only for A0.

Table 4. Read Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1-A7	A8-A18	DQ0-DQ7	DQ8-DQ15
Manufact. Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Don't Care	20h	00h
Device Code	M28W800BT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	92h	88h
	M28W800BB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	93h	88h

Note: $\overline{RP}$ = V_{IH}.

Table 5. Memory Blocks Protection Truth Table

V_{PP} (1)	$\overline{RP}$	$\overline{WP}$ (1)	Lockable Blocks (blocks #0 and #1)	Other Blocks
X	V_{IL}	X	Protected	Protected
V_{IL}	V_{IH}	X	Protected	Protected
V_{DD} or V_{PPH} (2)	V_{IH}	V_{IL}	Protected	Unprotected
V_{DD} or V_{PPH} (2)	V_{IH}	V_{IH}	Unprotected	Unprotected

Note: 1. X = Don't Care
2. V_{PP} must also be greater than the Program Voltage Lock Out V_{PPLK}.

Table 6. Program, Erase Times and Program/Erase Endurance Cycles

Parameter	Test Conditions	M28W800B			Unit
		Min	Typ	Max	
Word Program	$V_{PP} = V_{DD}$		10	200	µs
Double Word Program	V_{PP} = 12V ±5%		10	200	µs
Main Block Program	V_{PP} = 12V ±5%		0.16	5	s
	$V_{PP} = V_{DD}$		0.32	5	s
Parameter Block Program	V_{PP} = 12V ±5%		0.02	4	s
	$V_{PP} = V_{DD}$		0.04	4	s
Main Block Erase	V_{PP} = 12V ±5%		1	10	s
	$V_{PP} = V_{DD}$		1	10	s
Parameter Block Erase	V_{PP} = 12V ±5%		0.8	10	s
	$V_{PP} = V_{DD}$		0.8	10	s
Program/Erase Cycles (per Block)		100,000			cycles

STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operation. The various bits convey information and errors on the operation. To read the Status register the Read Status Register command can be issued, refer to the Read Status Register Command section. To output the contents, the Status Register is latched on the falling edge of the Chip Enable or Output Enable signals, and can be read until Chip Enable or Output Enable returns to V_{IH}. Either Chip Enable or Output Enable must be toggled to update the latched data.

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 7, Status Register Bits. Refer to Table 7 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low (set to '0'), the Program/Erase Controller is active; when the bit is High (set to '1'), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High .

During Program, Erase, operations the Program/Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit (set to '1') indicates that an Erase operation has been suspended or is going to be suspended.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 7 is set within 30µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. When the Erase Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program failure. When the Program Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to '0'), the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High (set to '1'), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit (set to '1') indicates that a Program operation has been suspended or is going to be suspended.

The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 2 is set within 5µs of the Program/Erase Suspend command being issued therefore the

memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is High (set to '1'), a Program or Erase operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value must be masked.

Note: Refer to Appendix C, Flowcharts and Pseudo Codes, for using the Status Register.

Table 7. Status Register Bits

Bit	Name	Logic Level	Definition
7	P/E.C. Status	'1'	Ready
		'0'	Busy
6	Erase Suspend Status	'1'	Suspended
		'0'	In progress or Completed
5	Erase Status	'1'	Erase Error
		'0'	Erase Success
4	Program Status	'1'	Program Error
		'0'	Program Success
3	V_{PP} Status	'1'	V_{PP} Invalid, Abort
		'0'	V_{PP} OK
2	Program Suspend Status	'1'	Suspended
		'0'	In Progress or Completed
1	Block Protection Status	'1'	Program/Erase on protected Block, Abort
		'0'	No operation to protected blocks
0	Reserved		

Note: Logic level '1' is High, '0' is Low.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature (1)	–40	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	155	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ}+0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6	4.1	V
V_{PP}	Program Voltage	–0.6	13	V

Note: 1. Depends on range.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 9, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 9. Operating and AC Measurement Conditions

Parameter	M28W800BT, M28W800BB								
	70		85		90		100		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{DD} Supply Voltage	2.7	3.6	2.7	3.6	2.7	3.6	2.7	3.6	V
V_{DDQ} Supply Voltage ($V_{DDQ} \leq V_{DD}$)	2.7	3.6	2.7	3.6	2.7	3.6	1.65	3.6	V
Ambient Operating Temperature	– 40	85	– 40	85	– 40	85	– 40	85	°C
Load Capacitance (C_L)	50		50		50		50		pF
Input Rise and Fall Times		5		5		5		5	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDQ}		0 to V_{DDQ}		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		$V_{DDQ}/2$		$V_{DDQ}/2$		V

Figure 6. AC Measurement I/O Waveform

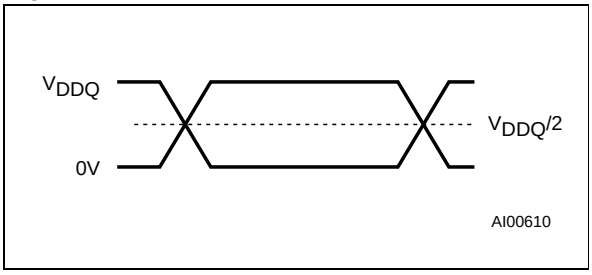


Figure 7. AC Measurement Load Circuit

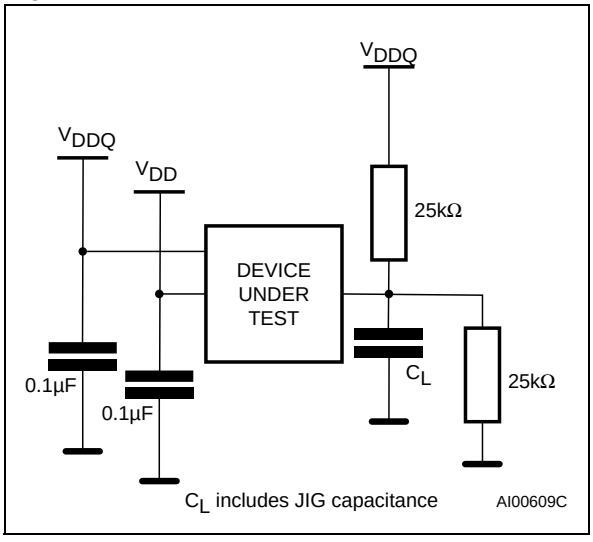


Table 10. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 11. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±10	µA
I_{DD}	Supply Current (Read)	$\overline{E} = V_{SS}$, $\overline{G} = V_{IH}$, f = 5MHz		10	20	mA
I_{DD1}	Supply Current (Stand-by or Automatic Stand-by)	$\overline{E} = V_{DDQ} \pm 0.2V$, $\overline{RP} = V_{DDQ} \pm 0.2V$		15	50	µA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		15	50	µA
I_{DD3}	Supply Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$		10	20	mA
		Program in progress $V_{PP} = V_{DD}$		10	20	mA
I_{DD4}	Supply Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$		5	20	mA
		Erase in progress $V_{PP} = V_{DD}$		5	20	mA
I_{DD5}	Supply Current (Program/Erase Suspend)	$\overline{E} = V_{DDQ} \pm 0.2V$, Erase suspended			50	µA
I_{PP}	Program Current (Read or Stand-by)	$V_{PP} > V_{DD}$			400	µA
I_{PP1}	Program Current (Read or Stand-by)	$V_{PP} \le V_{DD}$			5	µA
I_{PP2}	Program Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$			5	µA
I_{PP3}	Program Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$			10	mA
		Program in progress $V_{PP} = V_{DD}$			5	µA
I_{PP4}	Program Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$			10	mA
		Erase in progress $V_{PP} = V_{DD}$			5	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
		$V_{DDQ} \ge 2.7V$	–0.5		0.8	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} +0.4	V
		$V_{DDQ} \ge 2.7V$	0.7 V_{DDQ}		V_{DDQ} +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min	V_{DDQ} –0.1			V
V_{PP1}	Program Voltage (Program or Erase operations)		1.65		3.6	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)				1	V
V_{LKO}	V_{DD} Supply Voltage (Program and Erase lock-out)				2	V

Figure 8. Read AC Waveforms

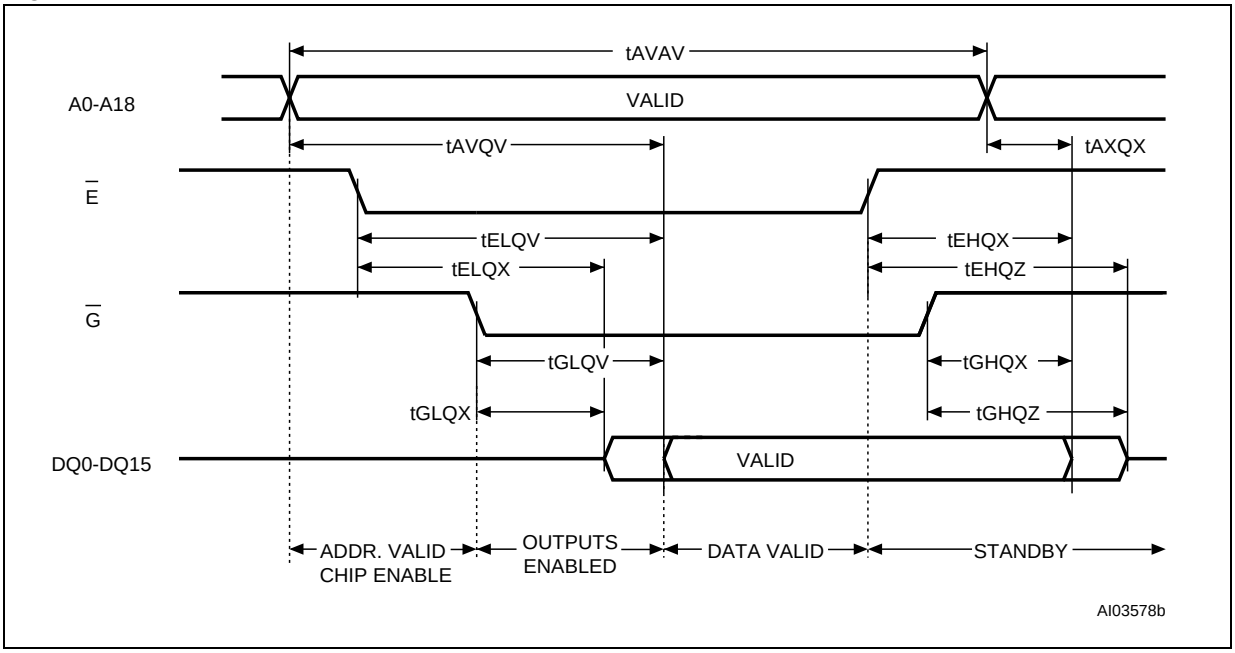


Table 12. Read AC Characteristics

Symbol	Alt	Parameter		M28W800B				Unit
				70	85	90	100	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	70	85	90	100	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	Max	70	85	90	100	ns
t_{AXQX} (1)	t_{OH}	Address Transition to Output Transition	Min	0	0	0	0	ns
t_{EHQX} (1)	t_{OH}	Chip Enable High to Output Transition	Min	0	0	0	0	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	20	20	25	30	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	Max	70	85	90	100	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	0	0	ns
t_{GHQX} (1)	t_{OH}	Output Enable High to Output Transition	Min	0	0	0	0	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	Max	20	20	25	30	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	20	20	30	35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	0	0	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 9. Write AC Waveforms, Write Enable Controlled

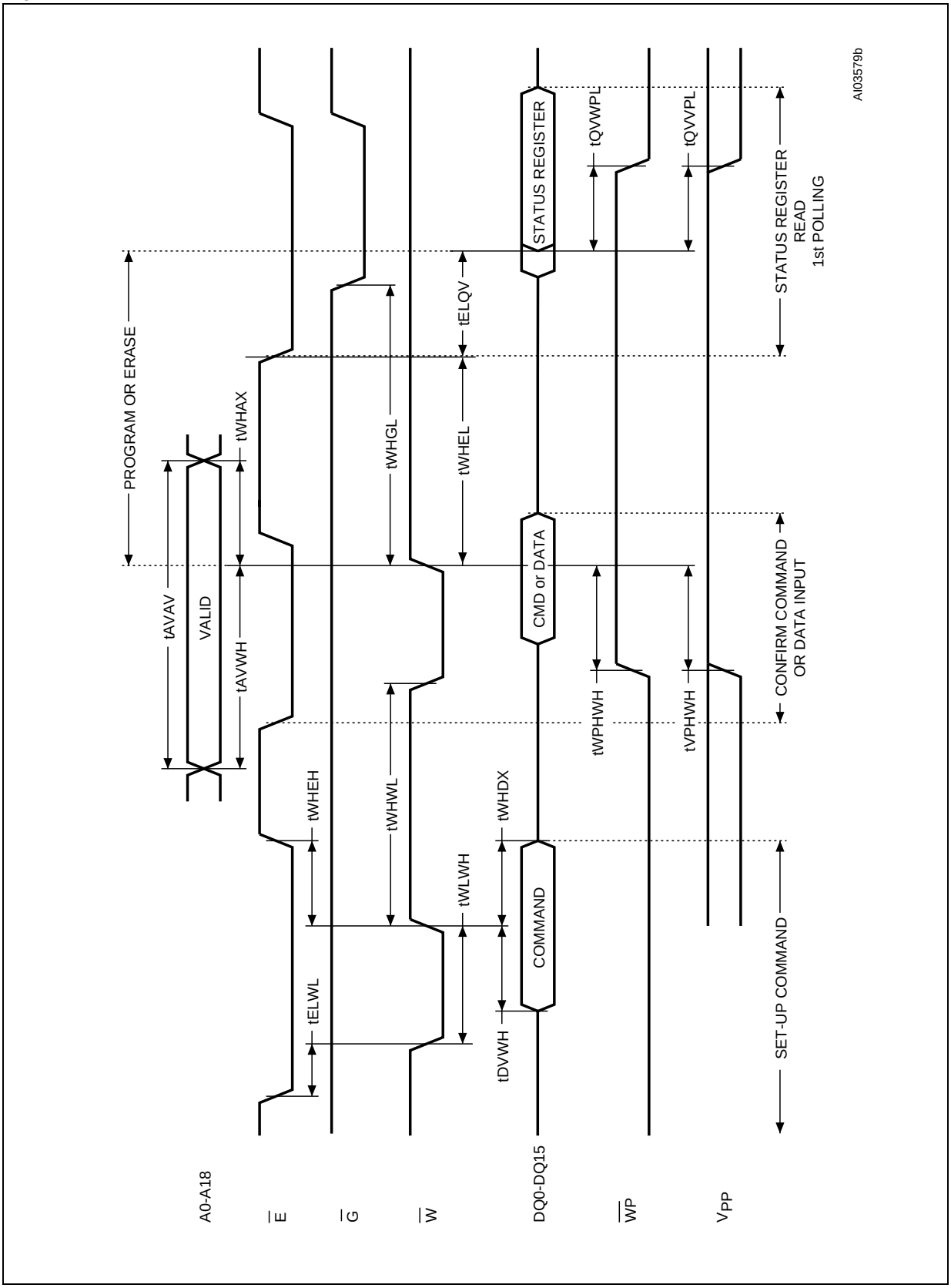


Table 13. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M28W800B				Unit
				70	85	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	85	90	100	ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Min	45	45	50	50	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	0	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70	85	90	100	ns
t_{QVVPL} (1,2)		Output Valid to V_{PP} Low	Min	0	0	0	0	ns
t_{QVWPL}		Output Valid to Write Protect Low	Min	0	0	0	0	ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	Min	200	200	200	200	ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	Min	0	0	0	0	ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	0	ns
t_{WHEL}		Write Enable High to Chip Enable Low	Min	25	25	30	30	ns
t_{WHGL}		Write Enable High to Output Enable Low	Min	20	20	30	30	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	25	25	30	30	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	50	50	ns
t_{WPHWH}		Write Protect High to Write Enable High	Min	45	45	50	50	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 10. Write AC Waveforms, Chip Enable Controlled

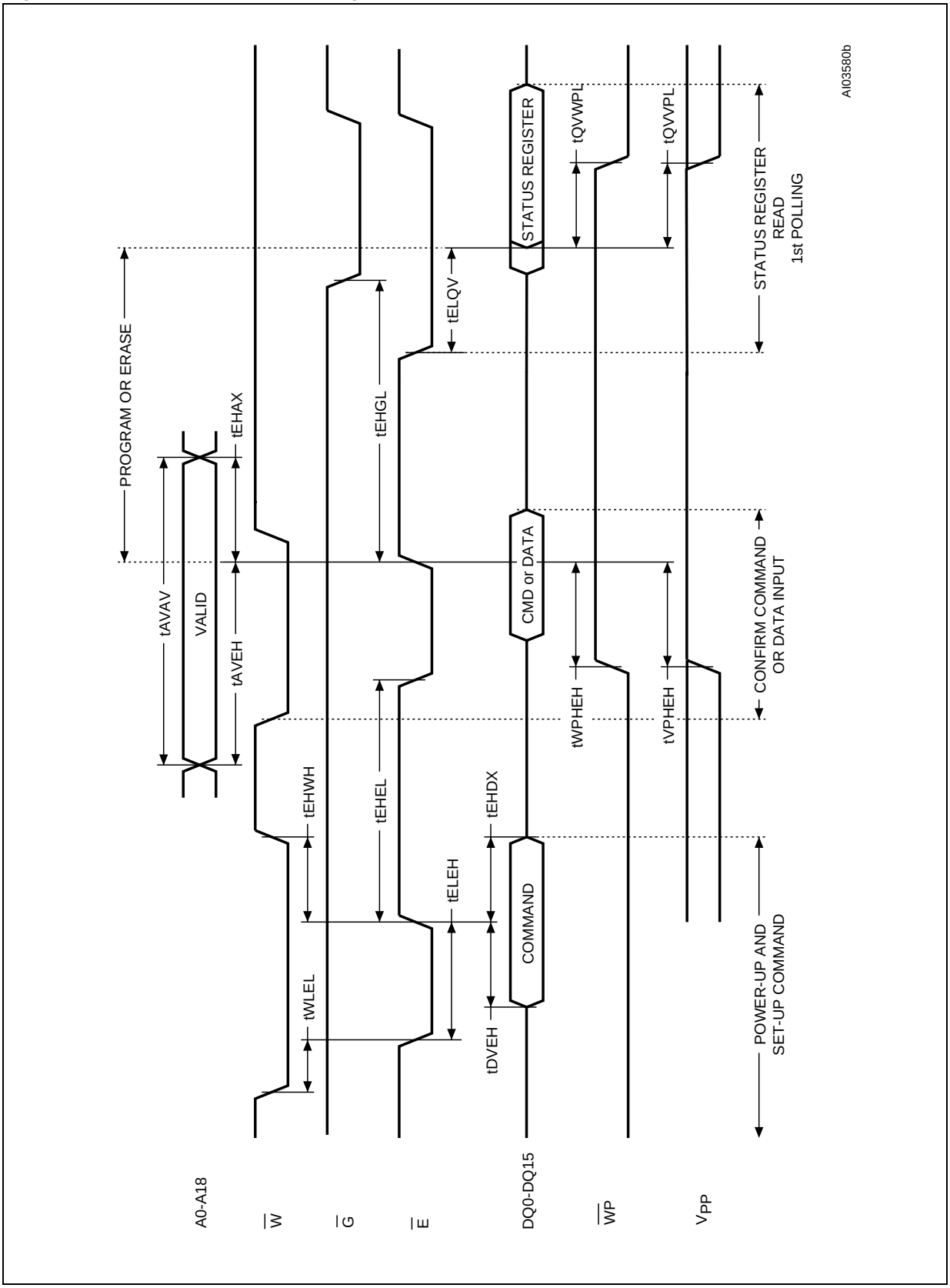


Table 14. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M28W800B				Unit
				70	85	90	100	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	85	90	100	ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	Min	45	45	50	50	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	Min	0	0	0	0	ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	Min	0	0	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	25	25	30	30	ns
t_{EHGL}		Chip Enable High to Output Enable Low	Min	25	25	30	30	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	50	50	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70	85	90	100	ns
t_{QVVPL} (1,2)		Output Valid to V_{PP} Low	Min	0	0	0	0	ns
t_{QVWPL}		Data Valid to Write Protect Low	Min	0	0	0	0	ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	Min	200	200	200	200	ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	Min	0	0	0	0	ns
t_{WPHEH}		Write Protect High to Chip Enable High	Min	45	45	50	50	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 11. Power-Up and Reset AC Waveforms

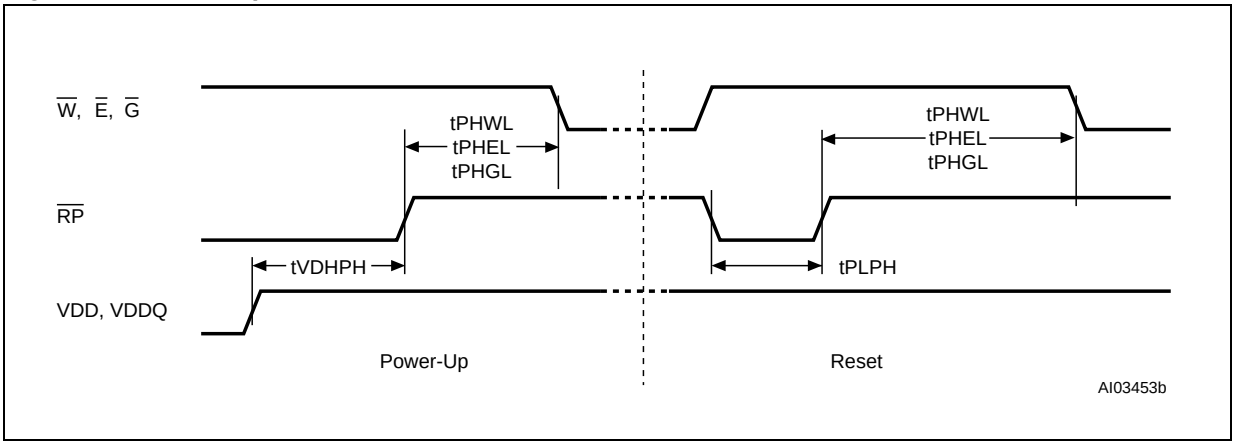


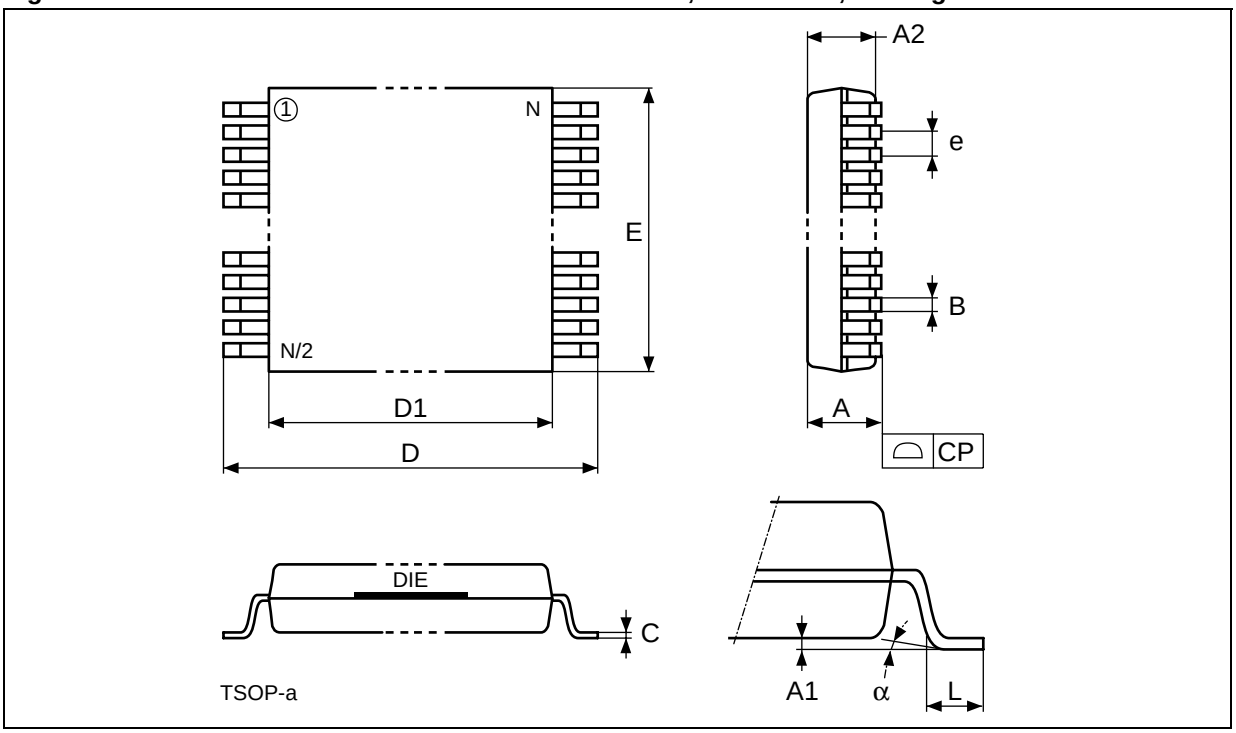
Table 15. Power-Up and Reset AC Characteristics

Symbol	Parameter	Test Condition		M28W800B				Unit
				70	85	90	100	
t_{PHWL} t_{PHEL} t_{PHGL}	Reset High to Write Enable Low, Chip Enable Low, Output Enable Low	During Program and Erase	Min	50	50	50	50	µs
		others	Min	30	30	30	30	ns
t_{PLPH}(1,2)	Reset Low to Reset High		Min	100	100	100	100	ns
t_{VDHPH}(3)	Supply Voltages High to Reset High		Min	50	50	50	50	µs

Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
2. Sampled only, not 100% tested.
3. It is important to assert $\overline{RP}$ in order to allow proper CPU initialization during power up or reset.

PACKAGE MECHANICAL

Figure 12. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

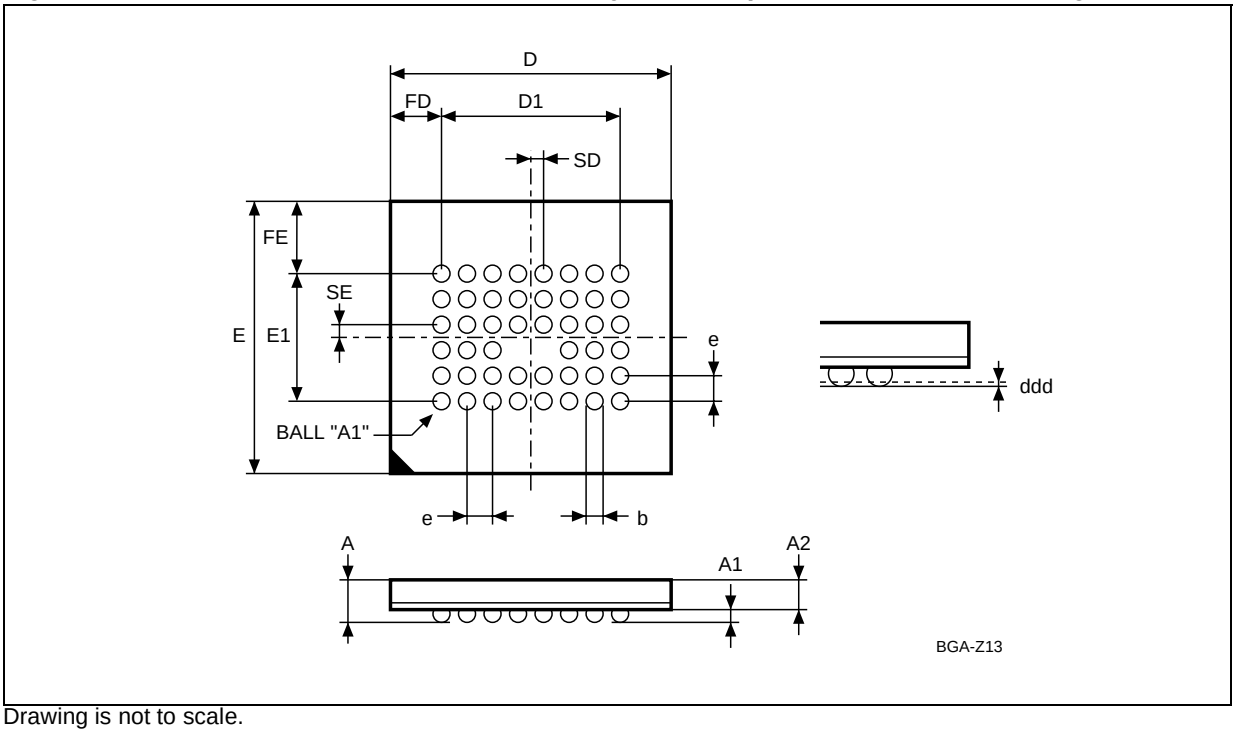


Note: Drawing is not to scale.

Table 16. TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0279
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

Figure 13. TFBGA46 6.39x6.37mm - 8x6 ball array, 0.75mm pitch, Bottom View Package Outline



Drawing is not to scale.

Table 17. TFBGA46 6.39x6.37mm - 8x6 ball array, 0.75mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2			1.000			0.0394
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	6.390	6.290	6.490	0.2516	0.2476	0.2555
D1	5.250	–	–	0.2067	–	–
ddd			0.100			0.0039
E	6.370	6.270	6.470	0.2508	0.2469	0.2547
e	0.750	–	–	0.0295	–	–
E1	3.750	–	–	0.1476	–	–
FD	0.570	–	–	0.0224	–	–
FE	1.310	–	–	0.0516	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

Figure 14. TFBGA46 Daisy Chain - Package Connections (Top view through package)

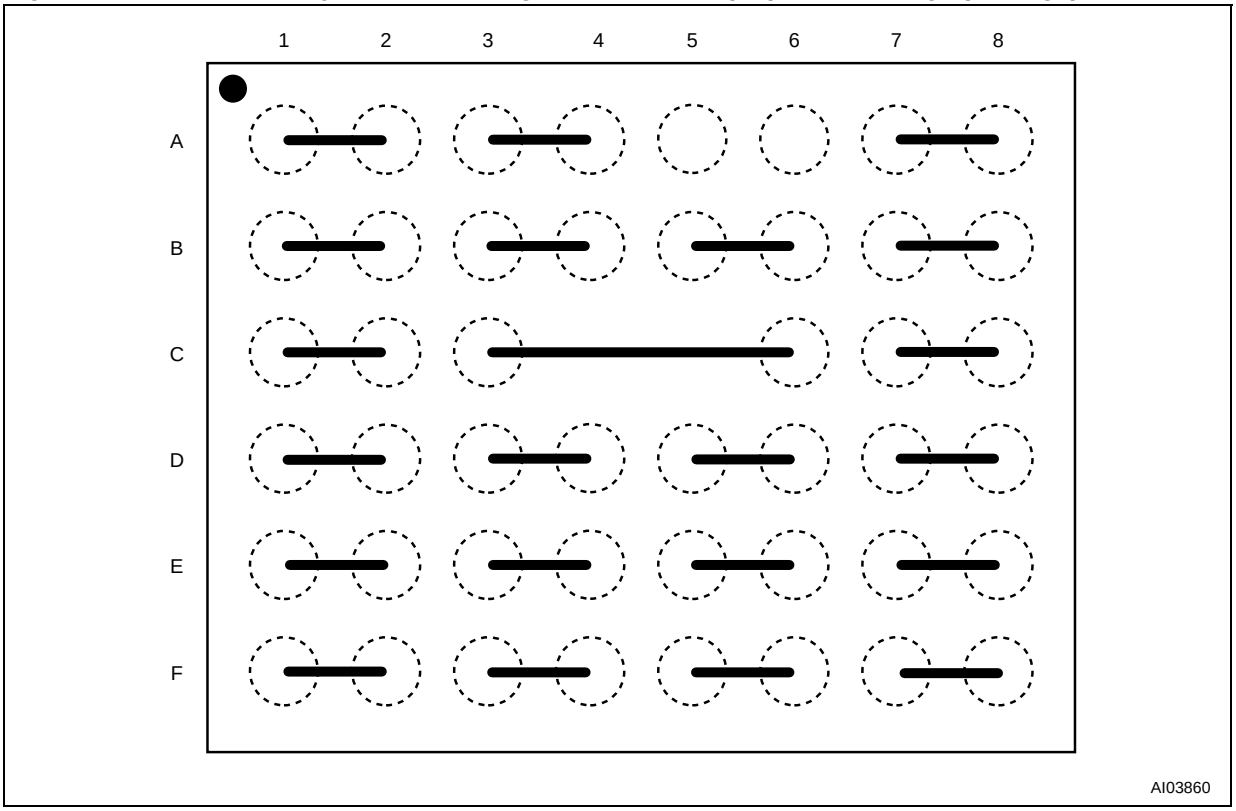
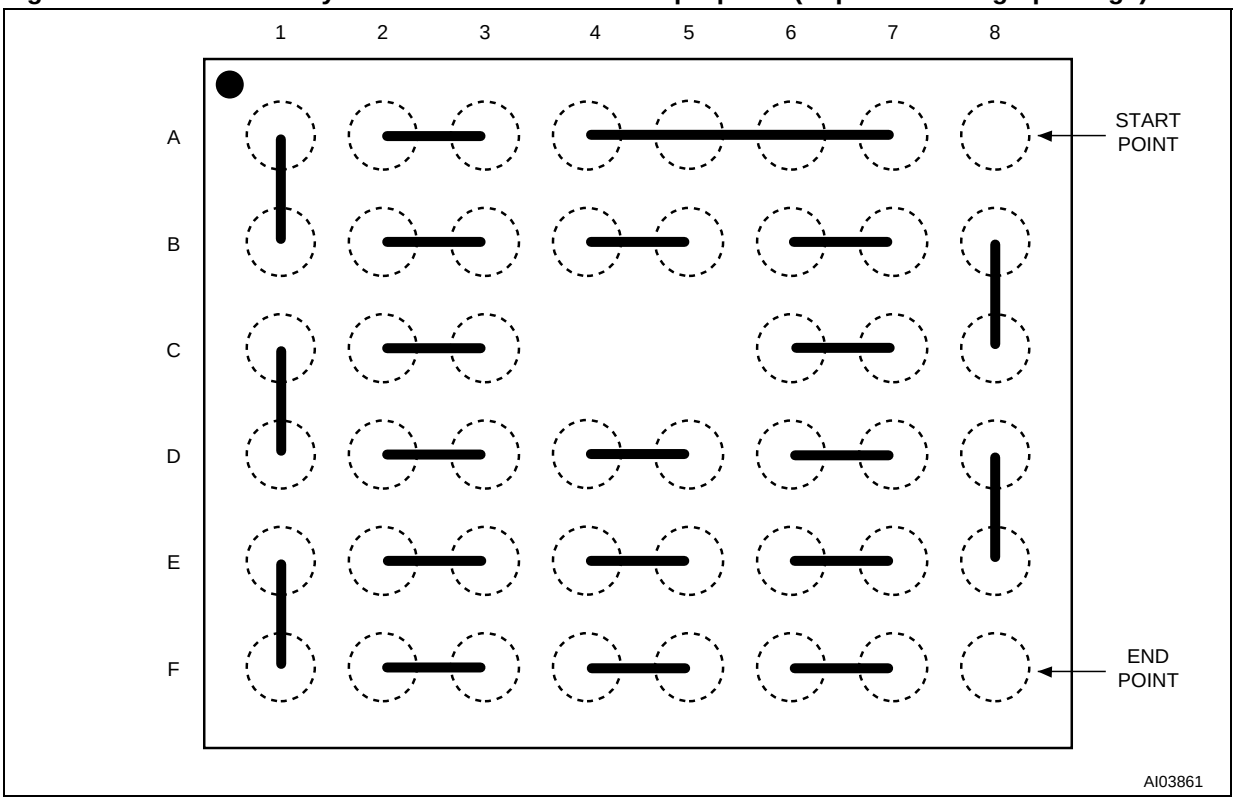


Figure 15. TFBGA46 Daisy Chain - PCB Connections proposal (Top view through package)



PART NUMBERING

Table 18. Ordering Information Scheme

Example: M28W800BT 90 N 6 T

Device Type
M28

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 1.65V to 3.6V

Device Function
800B = 8 Mbit (512Kb x16), Boot Block

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
70 = 70 ns
85 = 85 ns
90 = 90 ns
100 = 100 ns

Package
N = TSOP48: 12 x 20 mm
ZB = TFBGA46: 6.39 x 6.37mm, 0.75 mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Table 19. Daisy Chain Ordering Scheme

Example: M28W800B -GB T

Device Type
M28W800B

Daisy Chain
-ZB = TFBGA46: 6.39 x 6.37mm, 0.75 mm pitch

Option
T = Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 20. Document Revision History

Date	Version	Revision Details
July 1999	-01	First Issue
10-May-2001	-02	Completely rewritten and restructured, 70ns and 85ns speed class added.
29-May-2001	-03	Corrections to CFI data and Block Address Table.
31-May-2001	-04	Package changes - TFBGA45 replaced by TFBGA46.
31-Oct-2001	-05	Document status changed from Preliminary Data to Datasheet V_{DDQ} Maximum changed to 3.3V Commands Table, Read CFI Query Address on 1st cycle changed to 'X' (Table 3) t_{WHEL} description clarified (Table 13)
16-May-2002	-06	V_{DDQ} Maximum changed to 3.6V, TFBGA package dimensions added to description.

APPENDIX A. BLOCK ADDRESS TABLES

Table 21. Top Boot Block Addresses, M28W800BT

#	Size (KWord)	Address Range
0	4	7F000-7FFFF
1	4	7E000-7EFFF
2	4	7D000-7DFFF
3	4	7C000-7CFFF
4	4	7B000-7BFFF
5	4	7A000-7AFFF
6	4	79000-79FFF
7	4	78000-78FFF
8	32	70000-77FFF
9	32	68000-6FFFF
10	32	60000-67FFF
11	32	58000-5FFFF
12	32	50000-57FFF
13	32	48000-4FFFF
14	32	40000-47FFF
15	32	38000-3FFFF
16	32	30000-37FFF
17	32	28000-2FFFF
18	32	20000-27FFF
19	32	18000-1FFFF
20	32	10000-17FFF
21	32	08000-0FFFF
22	32	00000-07FFF

Table 22. Bottom Boot Block Addresses, M28W800BB

#	Size (KWord)	Address Range
22	32	78000-7FFFF
21	32	70000-77FFF
20	32	68000-6FFFF
19	32	60000-67FFF
18	32	58000-5FFFF
17	32	50000-57FFF
16	32	48000-4FFFF
15	32	40000-47FFF
14	32	38000-3FFFF
13	32	30000-37FFF
12	32	28000-2FFFF
11	32	20000-27FFF
10	32	18000-1FFFF
9	32	10000-17FFF
8	32	08000-0FFFF
7	4	07000-07FFF
6	4	06000-06FFF
5	4	05000-05FFF
4	4	04000-04FFF
3	4	03000-03FFF
2	4	02000-02FFF
1	4	01000-01FFF
0	4	00000-00FFF

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 23, 24, 25, 26, 27 and 28 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 28, Security Code area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 23. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: Query data are always presented on the lowest order data outputs.

Table 24. CFI Query Identification String

Offset	Data	Description	Value
00h	0020h	Manufacturer Code	ST
01h	8892h 8893h	Device Code	Top Bottom
02h-0Fh	reserved	Reserved	
10h	0051h	Query Unique ASCII String "QRY"	“Q”
11h	0052h	Query Unique ASCII String "QRY"	“R”
12h	0059h	Query Unique ASCII String "QRY"	“Y”
13h 14h	0003h 0000h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	Intel Compatible
15h 16h	offset = P = 0035h 0000h	Address for Primary Algorithm extended Query table	P=35h
17h 18h	0000h 0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)	NA
19h 1Ah	value = A = 0000h 0000h	Address for Alternate Algorithm extended Query table note: 0000h means none exists	NA

Note: Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 25. CFI Query System Interface Information

Offset	Data	Description	Value
1Bh	0027h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	2.7V
1Ch	0036h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	3.6V
1Dh	00B4h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.4V
1Eh	00C6h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.6V
1Fh	0004h	Typical timeout per single word program = 2^n µs	16µs
20h	0004h	Typical timeout for Double Word Program = 2^n µs	16µs
21h	000Ah	Typical timeout per individual block erase = 2^n ms	1 s
22h	0000h	Typical timeout for full chip erase = 2^n ms	NA
23h	0005h	Maximum timeout for word program = 2^n times typical	512µs
24h	0005h	Maximum timeout for Double Word Program = 2^n times typical	512µs
25h	0003h	Maximum timeout per individual block erase = 2^n times typical	8 s
26h	0000h	Maximum timeout for chip erase = 2^n times typical	NA

Table 26. Device Geometry Definition

Offset Word Mode		Data	Description	Value
27h		0014h	Device Size = 2^n in number of bytes	1MByte
28h 29h		0001h 0000h	Flash Device Interface Code description	x16 Async
2Ah 2Bh		0002h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	4
2Ch		0002h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	2
M28W800BT	2Dh 2Eh	000Eh 0000h	Region 1 Information Number of identical-size erase block = 000Eh+1	15
	2Fh 30h	0000h 0001h	Region 1 Information Block size in Region 1 = 0100h * 256 byte	64KByte
	31h 32h	0007h 0000h	Region 2 Information Number of identical-size erase block = 0007h+1	8
	33h 34h	0020h 0000h	Region 2 Information Block size in Region 2 = 0020h * 256 byte	8KByte
M28W800BB	2Dh 2Eh	0007h 0000h	Region 1 Information Number of identical-size erase block = 0007h+1	8
	2Fh 30h	0020h 0000h	Region 1 Information Block size in Region 1 = 0020h * 256 byte	8KByte
	31h 32h	000Eh 0000h	Region 2 Information Number of identical-size erase block = 000Eh+1	15
	33h 34h	0000h 0001h	Region 2 Information Block size in Region 2 = 0100h * 256 byte	64KByte

Table 27. Primary Algorithm-Specific Extended Query Table

Offset P = 35h (1)	Data	Description	Value
(P+0)h = 35h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
(P+1)h = 36h	0052h		"R"
(P+2)h = 37h	0049h		"I"
(P+3)h = 38h	0031h	Major version number, ASCII	"1"
(P+4)h = 39h	0030h	Minor version number, ASCII	"0"
(P+5)h = 3Ah	0006h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte.	
(P+6)h = 3Bh	0000h		
(P+7)h = 3Ch	0000h	bit 0 Chip Erase supported (1 = Yes, 0 = No)	No
		bit 1 Erase Suspend supported (1 = Yes, 0 = No)	Yes
(P+8)h = 3Dh	0000h	bit 2 Program Suspend (1 = Yes, 0 = No)	Yes
		bit 3 Lock/Unlock supported (1 = Yes, 0 = No)	No
		bit 4 Queued Erase supported (1 = Yes, 0 = No)	No
		bit 31 to 5 Reserved; undefined bits are ‘0’	
(P+9)h = 3Eh	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query are always supported during Erase or Program operation	
		bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No)	Yes
		bit 7 to 1 Reserved; undefined bits are ‘0’	
(P+A)h = 3Fh	0000h	Block Lock Status Defines which bits in the Block Status Register section of the Query are implemented.	NA
(P+B)h = 40h	0000h		
		bit 0 Block Lock Status Register Lock/Unlock bit active (1 = Yes, 0 = No)	
		bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No)	
		bit 15 to 2 Reserved for future use; undefined bits are ‘0’	
(P+C)h = 41h	0030h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance)	3V
		bit 7 to 4 HEX value in volts	
		bit 3 to 0 BCD value in 100 mV	
(P+D)h = 42h	00C0h	V_{PP} Supply Optimum Program/Erase voltage	12V
		bit 7 to 4 HEX value in volts	
		bit 3 to 0 BCD value in 100 mV	
(P+E)h	0000h	Reserved	

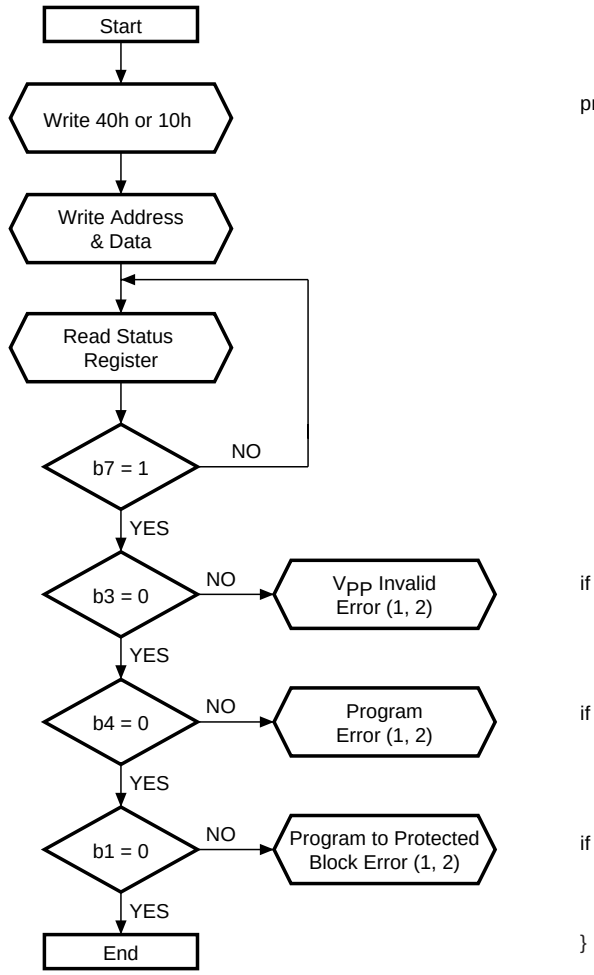
Note: 1. See Table 24, offset 15h for P pointer definition.

Table 28. Security Code Area

Offset	Data	Description
81h	XXXX	64 bits unique device number.
82h	XXXX	
83h	XXXX	
84h	XXXX	

APPENDIX C. FLOWCHARTS AND PSEUDO CODES

Figure 16. Program Flowchart and Pseudo Code




```
program_command (addressToProgram, dataToProgram) {:
        writeToFlash (any_address, 0x40) ;
        /*or writeToFlash (any_address, 0x10) ; */

         writeToFlash (addressToProgram, dataToProgram) ;
         /*Memory enters read status state after
         the Program Command*/

      do {
          status_register=readFlash (any_address) ;
          /* E or G must be toggled*/

         } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

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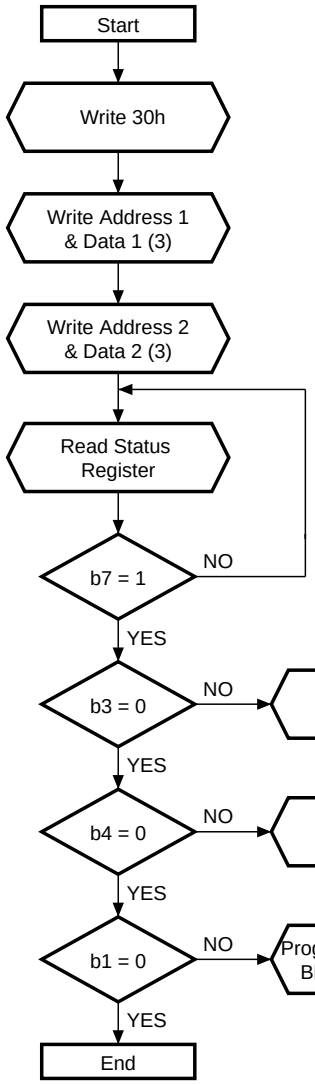
Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 17. Double Word Program Flowchart and Pseudo Code




```
double_word_program_command (addressToProgram1, dataToProgram1,
                                        addressToProgram2, dataToProgram2)
{
        writeToFlash (any_address, 0x30) ;
        writeToFlash (addressToProgram1, dataToProgram1) ;
                                        /*see note (3) */
        writeToFlash (addressToProgram2, dataToProgram2) ;
                                        /*see note (3) */
         /*Memory enters read status state after
        the Program command*/

      do {
        status_register=readFlash (any_address) ;
        /* E or G must be toggled*/

        } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

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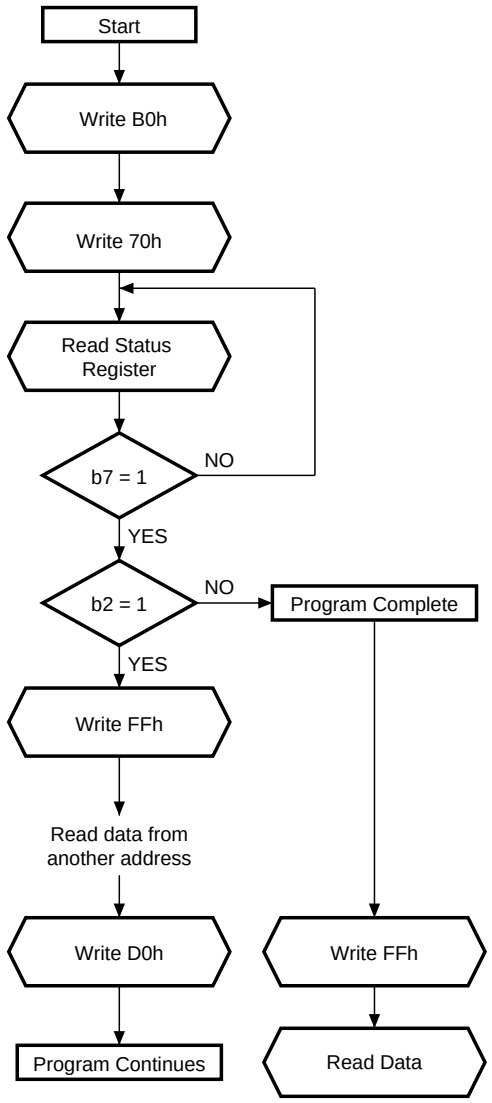
Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.

Figure 18. Program Suspend & Resume Flowchart and Pseudo Code




```
program_suspend_command   ( ) {
      writeToFlash (any_address, 0xB0) ;

      writeToFlash (any_address, 0x70) ;
      /* read status register to check if
      program has already completed */


  do {
      status_register=readFlash (any_address) ;
      /* E or G must be toggled*/




      } while (status_register.b7== 0) ;




if  (status_register.b2==0)  /*program completed */
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ) ; /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/


       }
else
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ); /*read data from another address*/
        writeToFlash (any_address, 0xD0) ;
        /*write 0xD0 to resume program*/
       }
}
```

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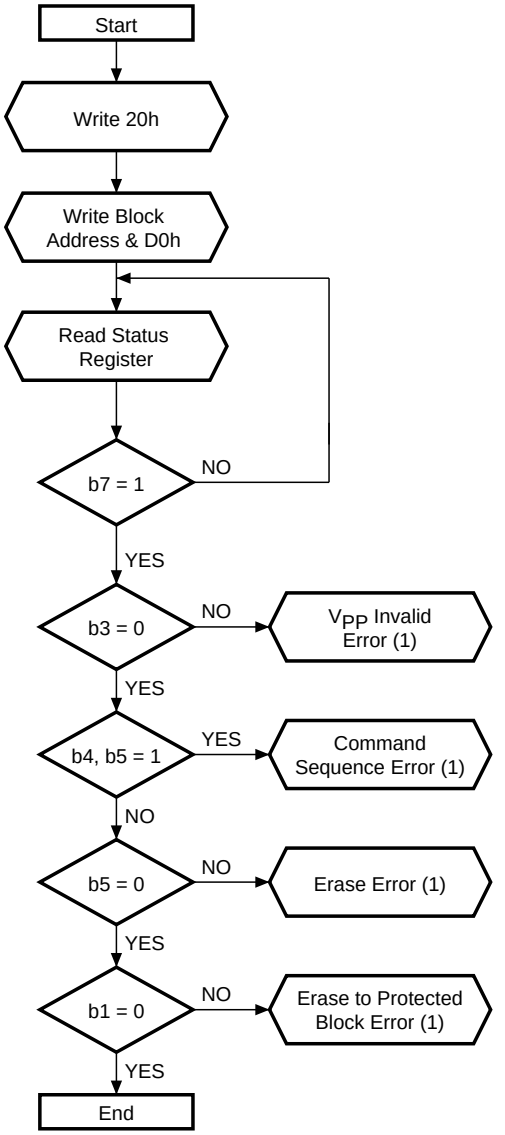
Figure 19. Erase Flowchart and Pseudo Code




```
erase_command   ( blockToErase )  {
        writeToFlash (any_address, 0x20) ;

        writeToFlash (blockToErase, 0xD0) ;
        /* only A12-A20 are significannt */
        /* Memory enters read status state after
        the Erase Command */


    do {
         status_register=readFlash (any_address) ;
          /* E or G must be toggled*/




        }  while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
        error_handler ( ) ;

if  ( (status_register.b4==1) && (status_register.b5==1) )
/* command sequence error */
        error_handler ( ) ;

if  ( (status_register.b5==1) )
/* erase error */
        error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
        error_handler ( ) ;


}
```

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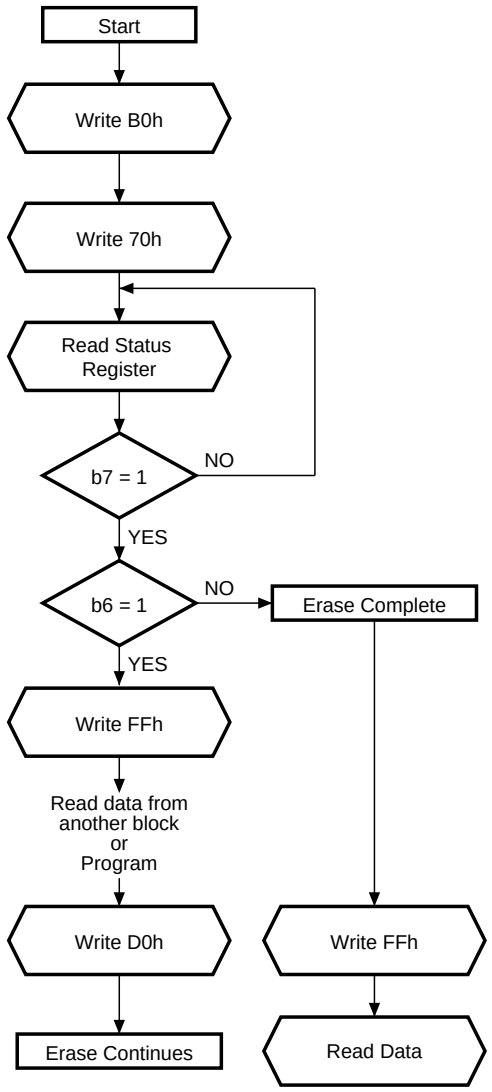
Note: If an error is found, the Status Register must be cleared before further Program/Erase operations.

Figure 20. Erase Suspend & Resume Flowchart and Pseudo Code




```
erase_suspend_command   ( ) {
        writeToFlash (any_address, 0xB0) ;

        writeToFlash (any_address, 0x70) ;
        /* read status register to check if
        erase has already completed */



    do {
        status_register=readFlash (any_address) ;
        /* E or G must be toggled*/



        } while (status_register.b7== 0) ;

if  (status_register.b6==0)  /*erase completed */
        {  writeToFlash (any_address, 0xFF)  ;


          read_data ( ) ;
          /*read data from another block*/
          /*The device returns to Read Array
          (as if program/erase suspend was not issued).*/


        }
else
        {  writeToFlash (any_address, 0xFF)  ;
          read_program_data ( );
          /*read or program data from another address*/
          writeToFlash (any_address, 0xD0) ;
          /*write 0xD0 to resume erase*/
        }
}
```

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APPENDIX D. COMMAND INTERFACE AND PROGRAM/ERASE CONTROLLER STATE

Table 29. Write State Machine Current/Next

Current State	SR bit 7	Data When Read	Command Input (and Next State)								
			Read Array (FFh)	Program Setup (10/40h)	Erase Setup (20h)	Erase Confirm (D0h)	Program/ Erase Suspend (B0h)	Program/ Erase Resume (D0h)	Read Status (70h)	Clear Status (50h)	Read Elect.Sg. (90h)
Read Array	“1”	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.
Read Status	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.
Read Elect.Sg.	“1”	Electronic Signature	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.
Program Setup	“1”	Status	Program (Command input = Data to be Programmed)								
Program (continue)	“0”	Status	Program (continue)				Program Suspend to Read Status	Program (continue)			
Program Suspend to Read Status	“1”	Status	Program Suspend to Read Array	Program Suspend to Read Array		Program (continue)	Program Suspend to Read Array	Program (continue)	Program Suspend to Read Status	Program Suspend to Read Array	Program Suspend to Read Elect.Sg.
Program Suspend to Read Array	“1”	Array	Program Suspend to Read Array	Program Suspend to Read Array		Program (continue)	Program Suspend to Read Array	Program (continue)	Program Suspend to Read Status	Program Suspend to Read Array	Program Suspend to Read Elect.Sg.
Program Suspend to Read Elect.Sg.	“1”	Electronic Signature	Program Suspend to Read Array	Program Suspend to Read Array		Program (continue)	Program Suspend to Read Array	Program (continue)	Program Suspend to Read Status	Program Suspend to Read Array	Program Suspend to Read Elect.Sg.
Program (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.
Erase Setup	“1”	Status	Erase Command Error			Erase (continue)	Erase Command Error	Erase (continue)	Erase Command Error		
Erase Cmd. Error	“0”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.
Erase (continue)	“1”	Status	Erase (continue)				Erase Suspend to Read Status	Erase (continue)			
Erase Suspend to Read Status	“1”	Status	Erase Suspend to Read Array	Program Setup	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Status	Erase Suspend to Read Array	Erase Suspend to Read Elect.Sg.
Erase Suspend to Read Array	“1”	Array	Erase Suspend to Read Array	Program Setup	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Status	Erase Suspend to Read Array	Erase Suspend to Read Elect.Sg.
Erase Suspend to Read Elect.Sg.	“1”	Electronic Signature	Erase Suspend to Read Array	Program Setup	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Array	Erase (continue)	Erase Suspend to Read Status	Erase Suspend to Read Array	Erase Suspend to Read Elect.Sg.
Erase (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Elect.Sg.

Note: Elect.Sg. = Electronic Signature.